ICmic™
IC MICROSYSTEMS

Preliminary Information

256K X25256 32K x 8 Bit

5MHz SPI Serial E 2PROM with Block Lock ™ Protection

FEATURES

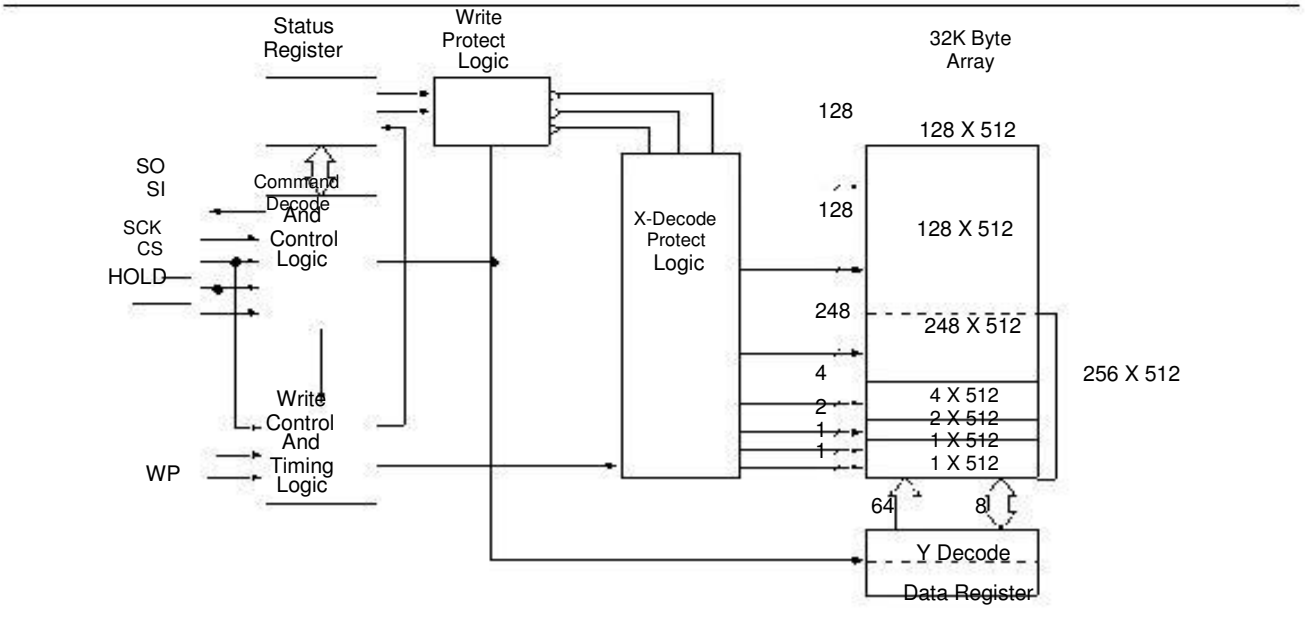
- 5MHz Clock Rate
- Low Power CMOS
  - —<1µA standby current
  - —<5mA active current
- 2.5V To 5.5V Power Supply
- SPI Modes (0,0 & 1,1)
- 32K X 8 Bits
  - —64 byte page mode
- Block Lock ™ Protection
  - —Protect first page, first 2 pages, first 4 pages, first 8 pages, 1/4, 1/2 or all of E^2PROM array
- Programmable Hardware Write Protection
  - —In-circuit programmable ROM mode
- Built-In Inadvertent Write Protection
  - —Power-up/down protection circuitry
  - —Write enable latch
  - —Write protect pin
- Self-Timed Write Cycle
  - —5ms write cycle time (typical)
- High Reliability
  - —Endurance: 100,000 cycles
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- Packages —8-lead XBGA
  - —8-lead SOIC (JEDEC, EIAJ)
  - —20-lead TSSOP

DESCRIPTION

The X25256 is a CMOS 256K-bit serial E^2PROM, internally organized as 32K x 8. The X25256 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select (CS) input, allowing any number of devices to share the same bus.

The X25256 also features two additional inputs that provide the end user with added flexibility. By asserting the HOLD input, the X25256 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The WP input can be used as a hardwire input to the X25256 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering first page, first 2 pages, 4 pages, 8 pages, 0, 1/4, 1/2 or all of the memory.

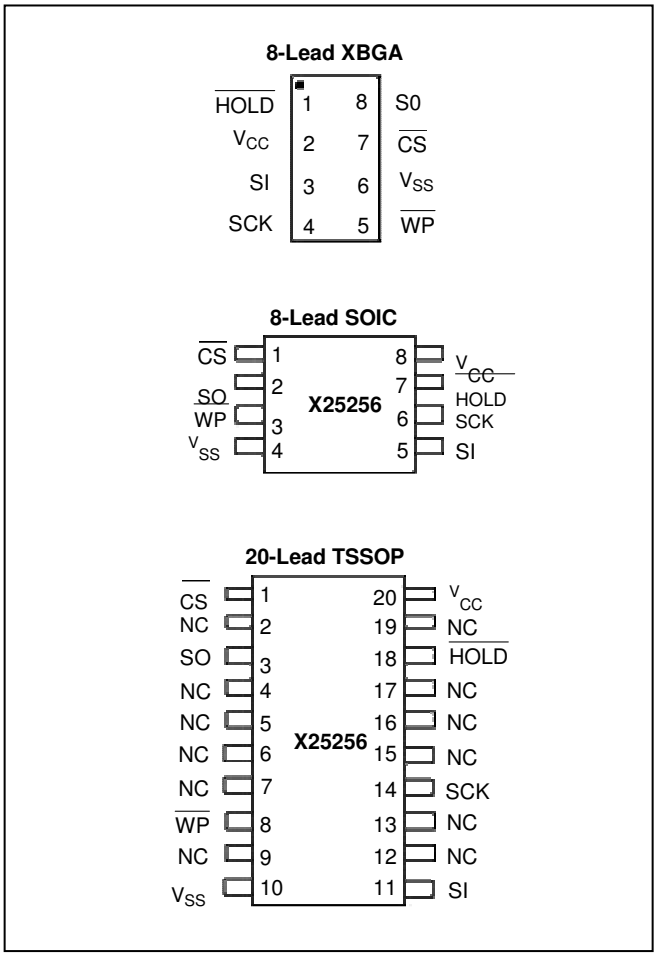
FUNCTIONAL DIAGRAM



™ and Block Lock™ Protection is a trademark of Xicor, Inc.

The X25256 utilizes Xicor's proprietary Direct Write ™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25256 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25256 will be in the standby power mode. $\overline{CS}$ LOW enables the X25256, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is "1", nonvolatile writes to the X25256 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25256 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is "0". This allows the user to install the X25256 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set "1".

Hold (HOLD)

HOLD is used in conjunction with the CS pin to pause the device. Once the part is selected and a serial sequence is underway, HOLD may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, HOLD must be brought LOW while SCK is LOW. To resume communication, HOLD is brought HIGH, again while SCK is LOW. If the pause feature is not used, HOLD should be held HIGH at all times.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 64 Bytes)

Notes: *Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

PRINCIPLES OF OPERATION

The X25256 is a 32K x 8 E^{2}PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25256 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. CS must be LOW and the HOLD and WP inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after CS goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input to place the X25256 into a "PAUSE" condition. After releasing HOLD, the X25256 will resume operation from the point when HOLD was first asserted.

Write Enable Latch

The X25256 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is format- ted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	BL2	BL1	BL0	WEL	WIP

WPEN, BL0 and BL1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

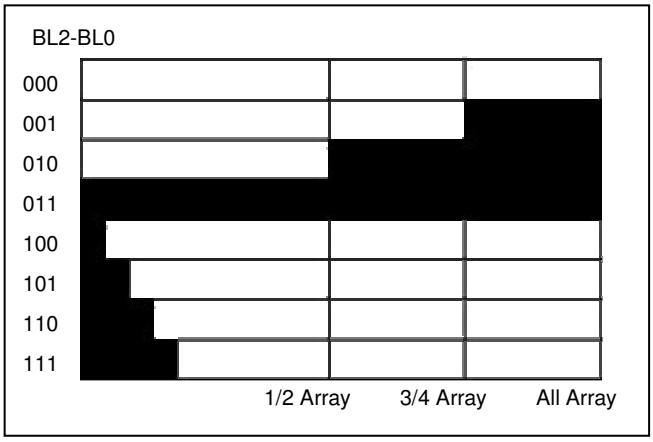
The Write-In-Process (WIP) bit indicates whether the X25256 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. This bit is set and reset by hardware, it cannot be controlled by the WRSR instruction. When reading the Status Register while an internal nonvolatile write is in progress, all bits output will be '1'. This allows the programmer to use the WIP bit to determine an early end of write condition. It also allows the programmer to check for "FF" or "not FF" to determine end of write. The programmer can also use the first one or two bits received from the Status Register (if they were known to be zero) to determine end of write. Each of these techniques can simplify or speed the end of nonvolatile write detection.

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset. This bit is controlled by hardware and cannot be written by the WRSR instruction.

The Block Lock (BL0, BL1, and BL2) bits are nonvola- tile and allow the user to select one of eight levels of protection. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated in the following table.

Status Register Bits			Array Addresses Protected	Array Lock
BL2	BL1	BL0		
0	0	0	None	None
0	0	1	$6000–$7FFF (8K bytes)	Upper 1/4 (Q4)
0	1	0	$4000–$7FFF (16K bytes)	Upper 1/2 (Q3, Q4)
0	1	1	$0000–$7FFF (32K bytes)	Full Array (All)
1	0	0	$000–$03F (64 bytes)	First Page (P1)
1	0	1	$000–$07F (128 bytes)	First 2 Pages (P2)
1	1	0	$000–$0FF (256 bytes)	First 4 Pages (P4)
1	1	1	$000–$1FF (512 bytes)	First 8Pages (P8)

Figure 1. Block Lock Configurations



The Write-Protect-Enable (WPEN) bit is available for the X25256 as a nonvolatile enable bit for the WP pin.

Programmable Hardware Write Protection

The Write Protect (WP) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the Programmable Hardware Write Protect feature. Hardware Write Protection is enabled when WP pin is LOW, and the WPEN bit is "1". Hardware Write Protection is disabled when either the WP pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Lock bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

In Circuit Programmable ROM Mode

Note that since the WPEN bit is write protected, it can- not be changed back to a LOW state; so write protection is enabled as long as the WP pin is held LOW. Thus an In Circuit Programmable ROM function can be implemented by hardwiring the WP pin to Vss, writing to and Block Locking the desired portion of the array to be ROM, and then programming the WPEN bit HIGH. The table above defines the program protect status for each combination of WPEN and WP.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the ^{2}E PROM memory array, CS is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25256, followed by the 16-bit address of which the last 15 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address

can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($7FFF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking CS HIGH. Refer to the read E^{2}PROM array operation sequence illustrated in Figure 2.

To read the status register the CS line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. Figure 3 illustrates the read status register sequence.

WP	WPEN	Memory Array Not Block Protected	Memory Array Block Protected	Block Lock Bits	WPEN Bit	Protection
HIGH	X	Writable	Blocked	Writable	Writable	Software
LOW	0	Writable	Blocked	Writable	Writable	Software
LOW	1	Writable	Blocked	Writes Blocked	Writes Blocked	Hardware

Write Sequence

Prior to any attempt to write data into the X25256, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 4). CS is first taken LOW, then the WREN instruction is clocked into the X25256. After all eight bits of the instruction are transmitted, CS must then be taken HIGH. If the user continues the write operation without taking CS HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^{2}PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. CS must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 64 bytes of data to the X25256. The only restriction is the 64 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, CS can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 5 and 6 below for a detailed illustration of the write sequences and time frames in which CS going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 5, and 6 are "don't care". Figure 7 illustrates this sequence.

While the write is in progress following a status register or E^{2}PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted HOLD can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when HOLD is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25256 powers-up in the following state:

– The device is in the low power standby state.
– A HIGH to LOW transition on CS is required to enter an active state and receive an instruction. –
SO pin is high impedance.
– The "write enable" latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

– The "write enable" latch is reset upon power-up.
– A WREN instruction must be issued to set the "write enable" latch.
– CS must come HIGH at the proper clock count in order to start a write cycle.

Figure 2. Read E²PROM Array Operation Sequence

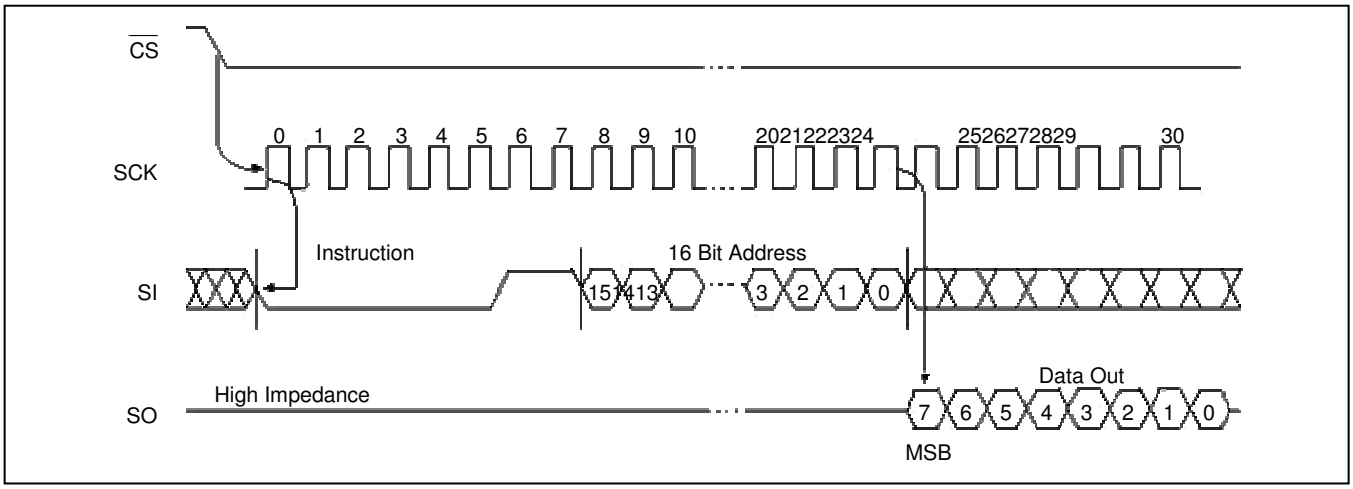


Figure 3. Read Status Register Operation Sequence

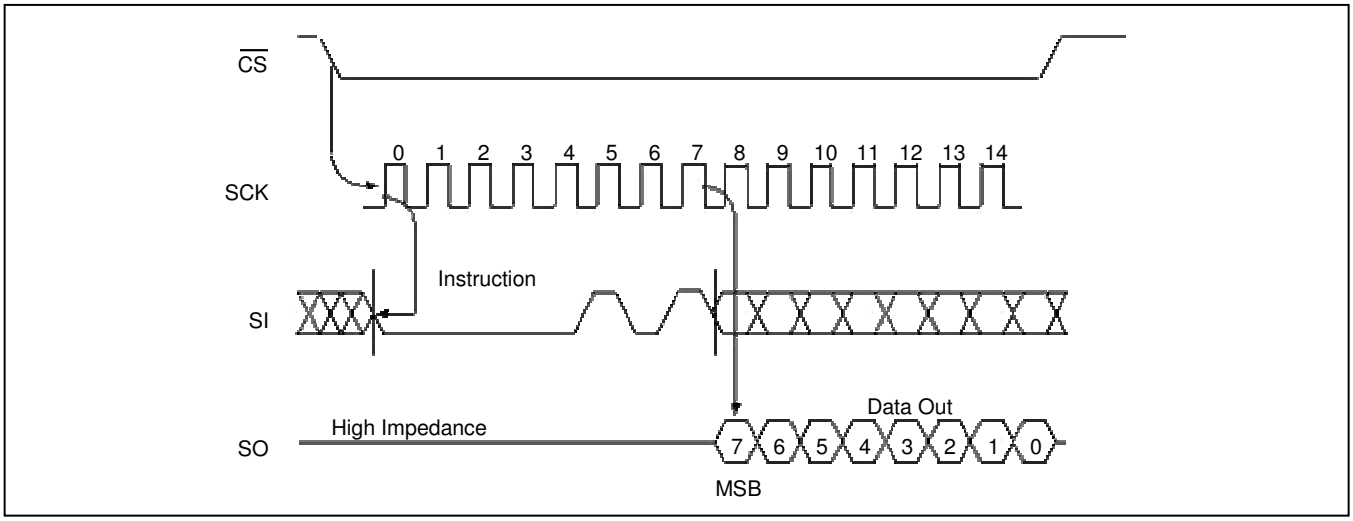


Figure 4. Write Enable Latch Sequence

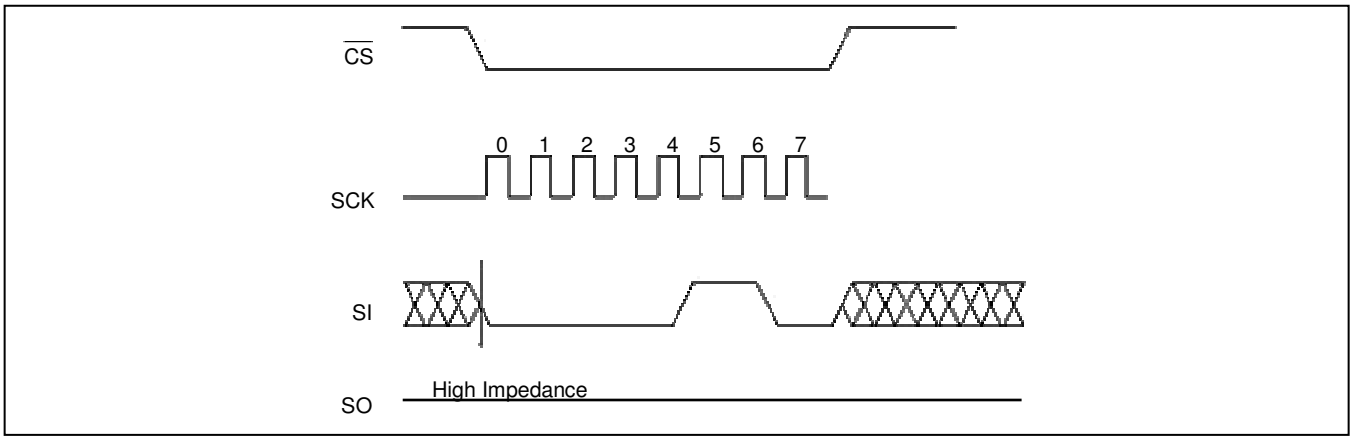


Figure 5. Byte Write Operation Sequence

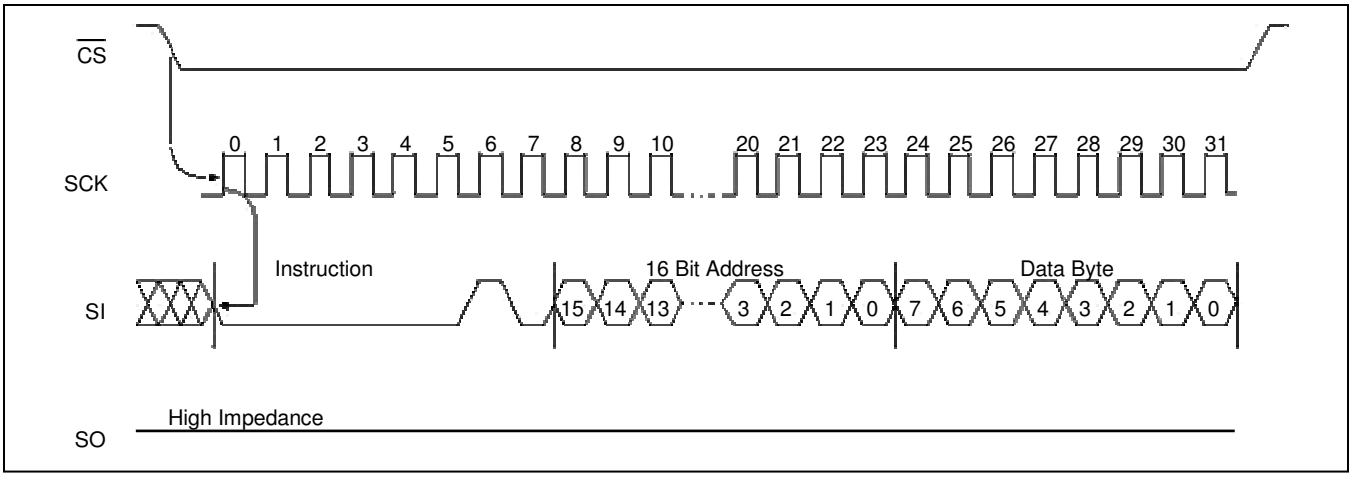


Figure 6. Page Write Operation Sequence

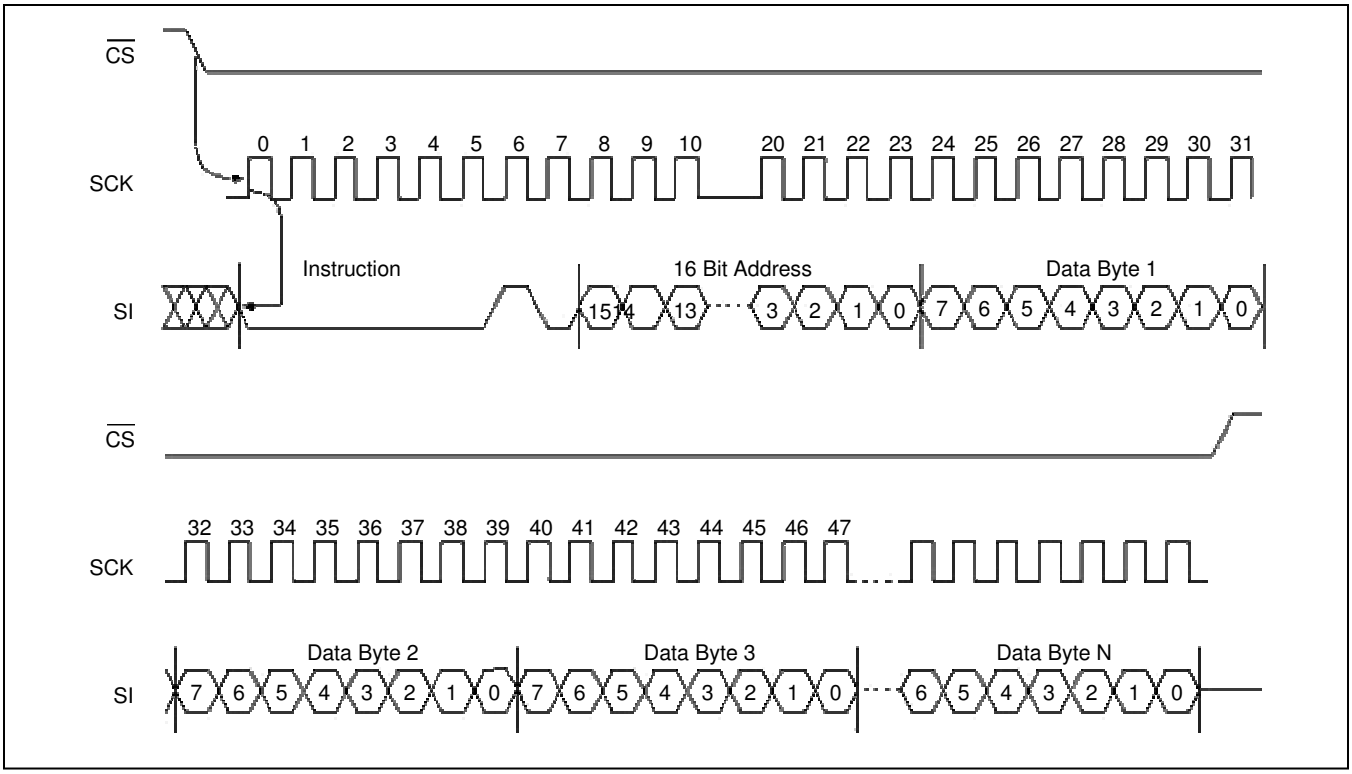
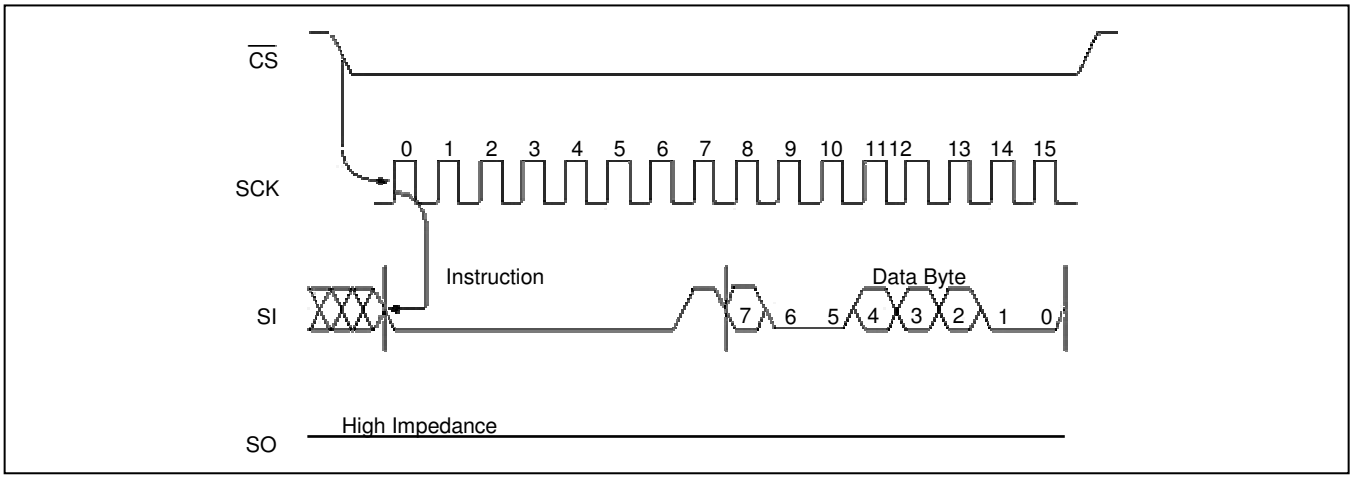


Figure 7. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....–65 to +135°C
Storage temperature .....–65 to +150°C
Voltage on any pin with
respect to V_{SS} .....–1V to +7V
D.C. output current
5mA (soldering, 10 seconds) ..... 300°C

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only; and the functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limit
X25256-2.5	2.5V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz, SO = Open, CS = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V, T_A = 25°C
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 5V
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1.0mA, V_{CC} = 5V
V_{OL2}	Output LOW Voltage		0.4	V	I_{OL} = 1.0mA, V_{CC} = 3V
V_{OH2}	Output HIGH Voltage	V_{CC}–0.4		V	I_{OH} = –0.4mA, V_{CC} = 3V

POWER-UP TIMING

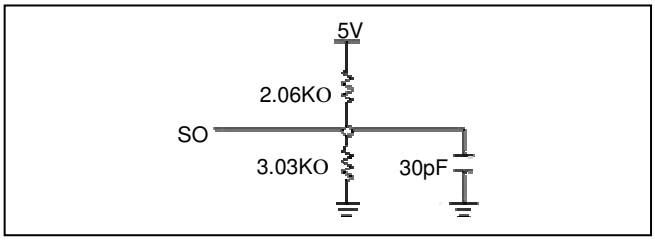
Symbol	Parameter	Min.	Max.	Unit
T_{PUR}(3)	Power-up to Read Operation		1	ms
T_{PUW}(3)	Power-up to Write Operation		5	ms

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Test Conditions
$C_{I/O}$(3)	Output Capacitance (SO)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Notes: (1)V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2)This parameter is periodically sampled and not 100% tested.
(3)t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} X 0.5

A.C. OPERATING CHARACTERISTICS

Data Input Timing

Symbol	Parameter	V_{CC} = 2.5V–5.5V		Unit
		Min.	Max.	
f_{SCK}	Clock Frequency	0	5.0	MHz
t_{CYC}	Cycle Time	200		ns
t_{LEAD}	$\overline{CS}$ Lead Time	100		ns
t_{LAG}	$\overline{CS}$ Lag Time	100		ns
t_{WH}	Clock HIGH Time	80		ns
t_{WL}	Clock LOW Time	80		ns
t_{SU}	Data Setup Time	20		ns
t_H	Data Hold Time	20		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	40		ns
t_{CD}	$\overline{HOLD}$ Hold Time	40		ns
t_{CS}	$\overline{CS}$ Deselect Time	100		ns
t_{WC}(5)	Write Cycle Time		10	ms

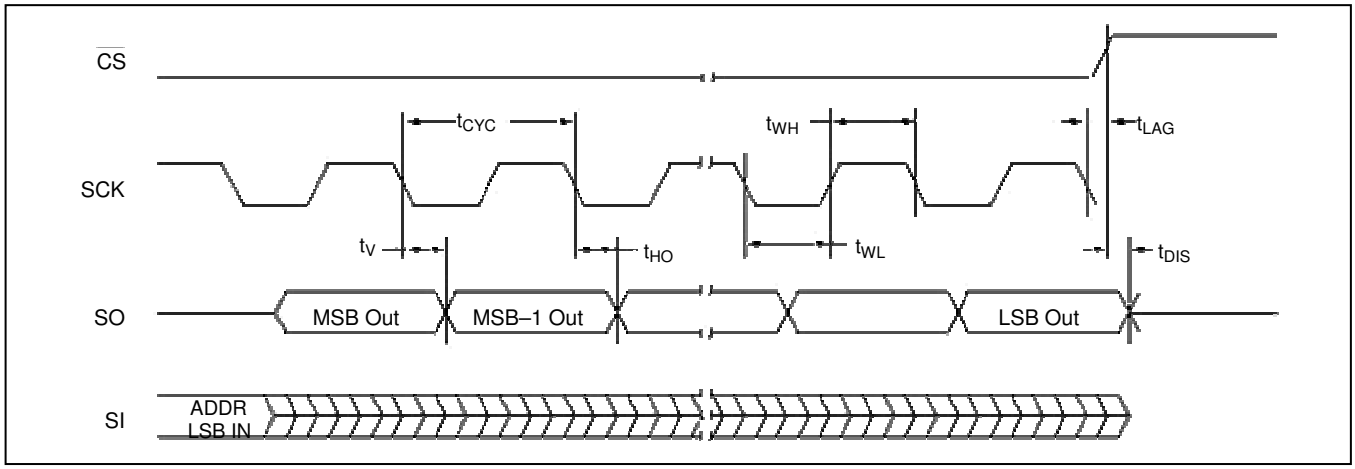
Data Output Timing

Symbol	Parameter	V_{CC} = 2.5V–5.5V		Unit
		Min.	Max.	
f_{SCK}	Clock Frequency	0	5.0	MHz
t_{DIS}	Output Disable Time		100	ns
t_V	Output Valid from Clock LOW		80	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		50	ns
t_{FO}(4)	Output Fall Time		50	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	50		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	50		ns

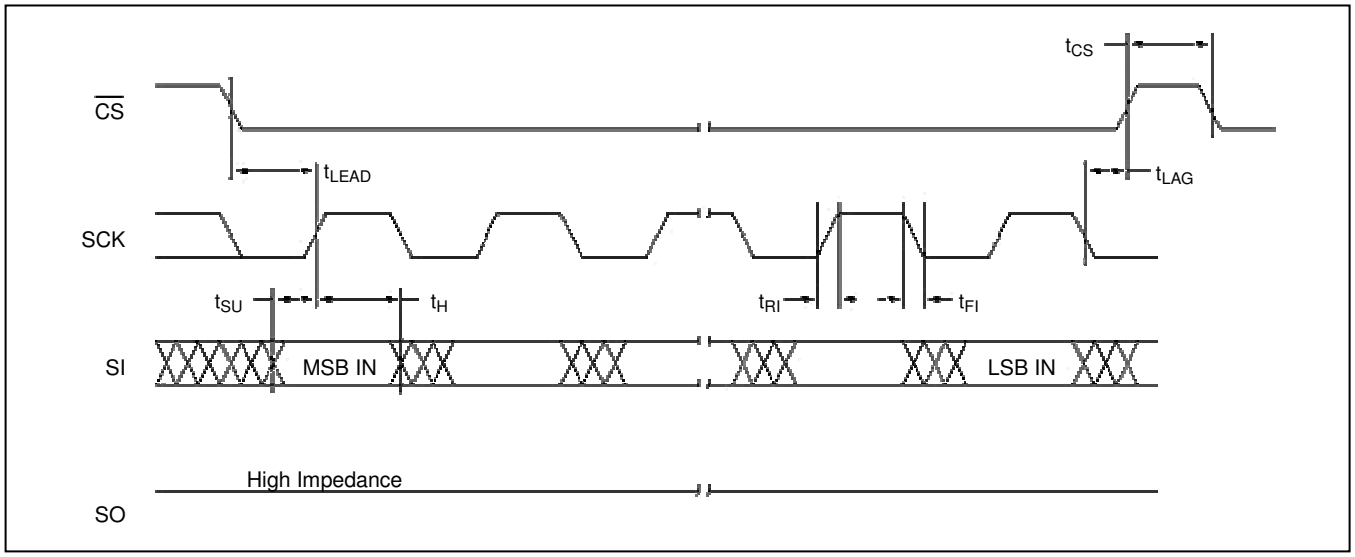
Notes: (4)This parameter is periodically sampled and not 100% tested.

(5)t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle

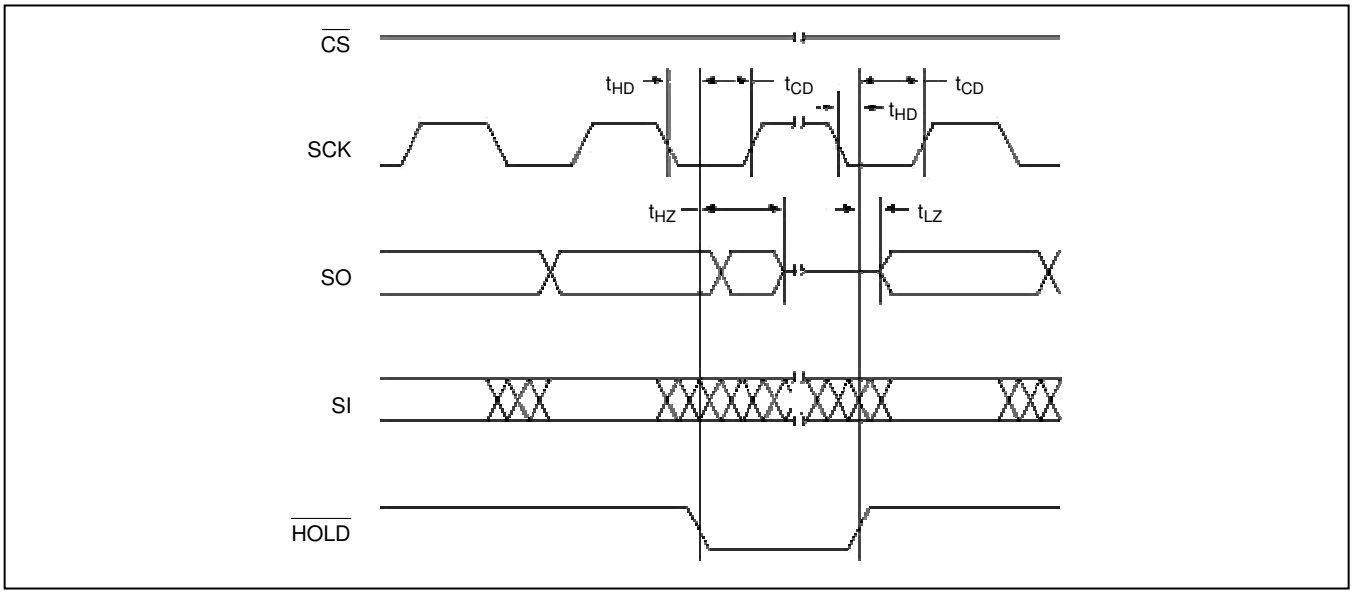
Serial Output Timing



Serial Input Timing

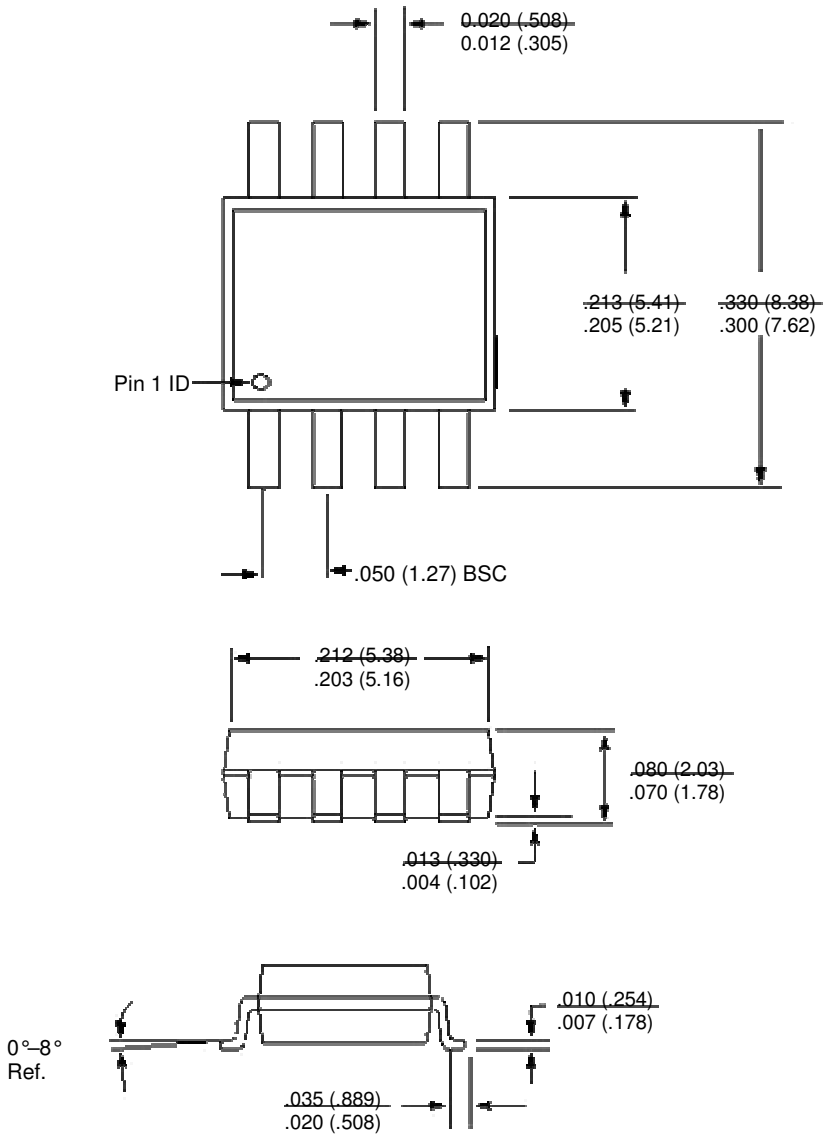


Hold Timing



PACKAGE INFORMATION

8-Lead Plastic, 0.200” Wide Small Outline Gullwing Package Typ “A” (EIAJ SOIC)

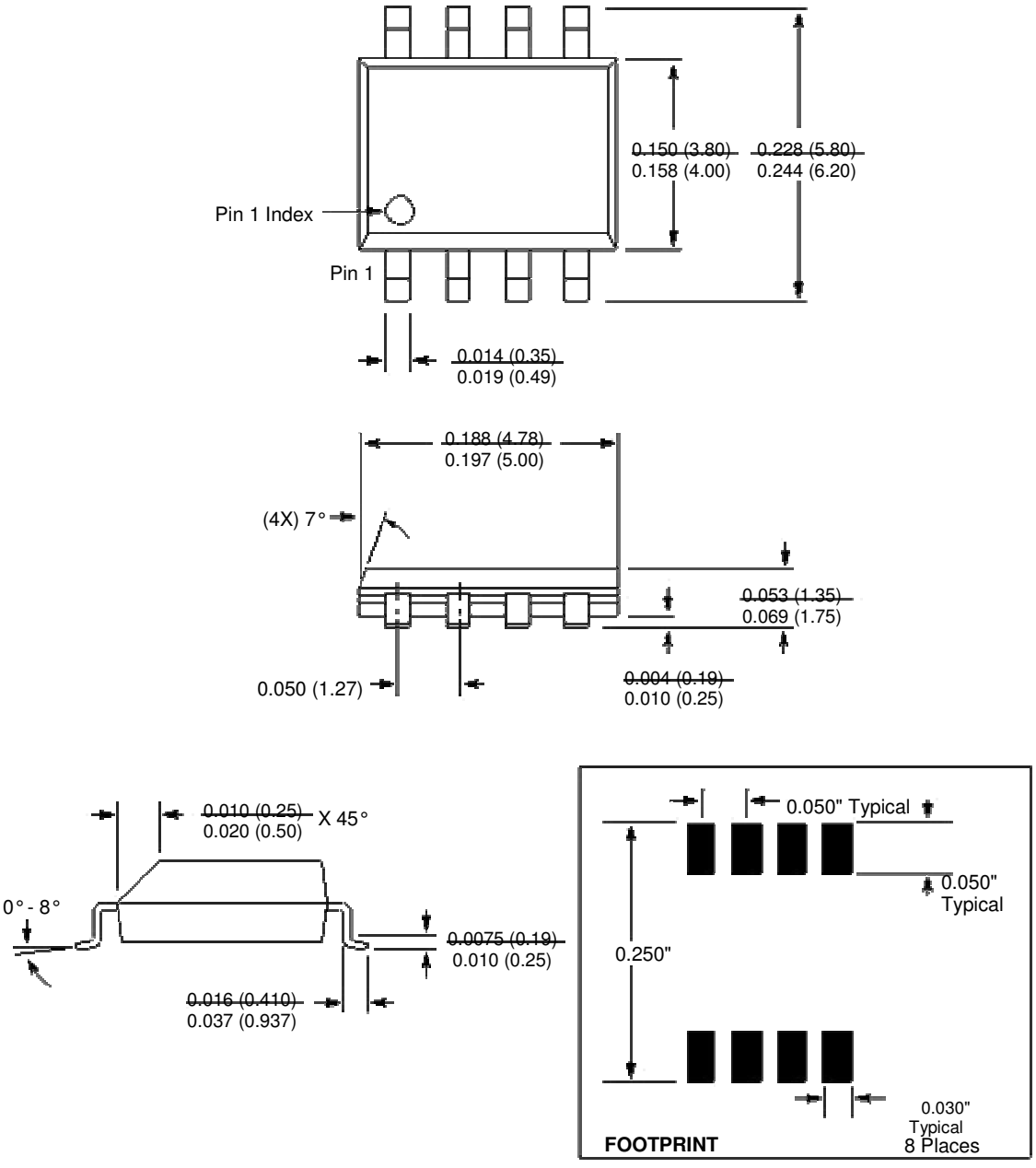


NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS) 2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

PACKAGING INFORMATION

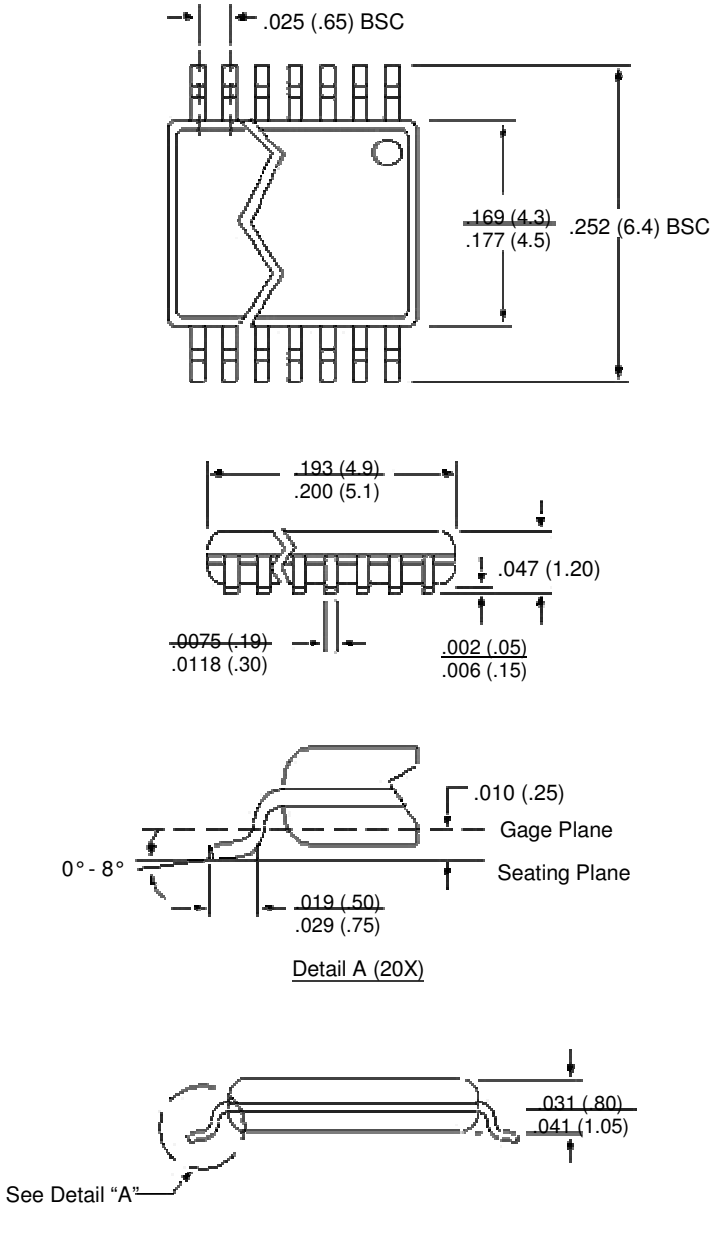
8-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

20-Lead Plastic, TSSOP, Package Type V



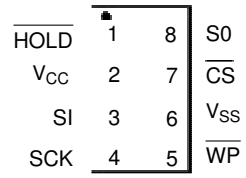
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

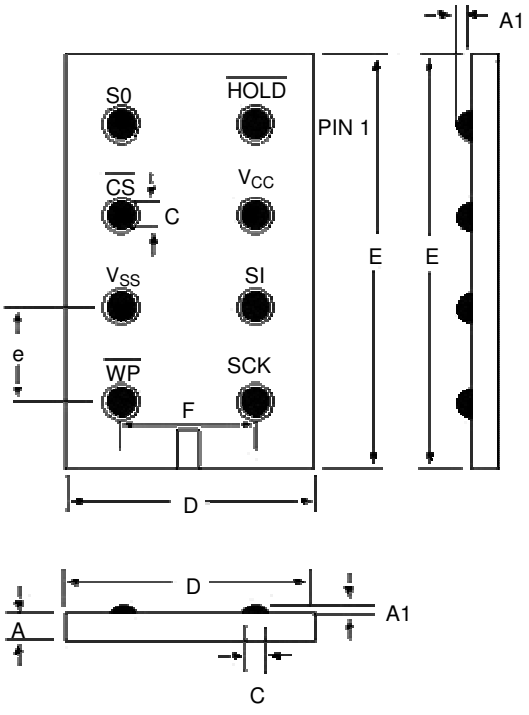
8-Lead XBGA

Complete Part Number	Top Mark
X25256B-2.5	XAAD
X25256BI-2.5	XACR

8-Lead XBGA: Top View



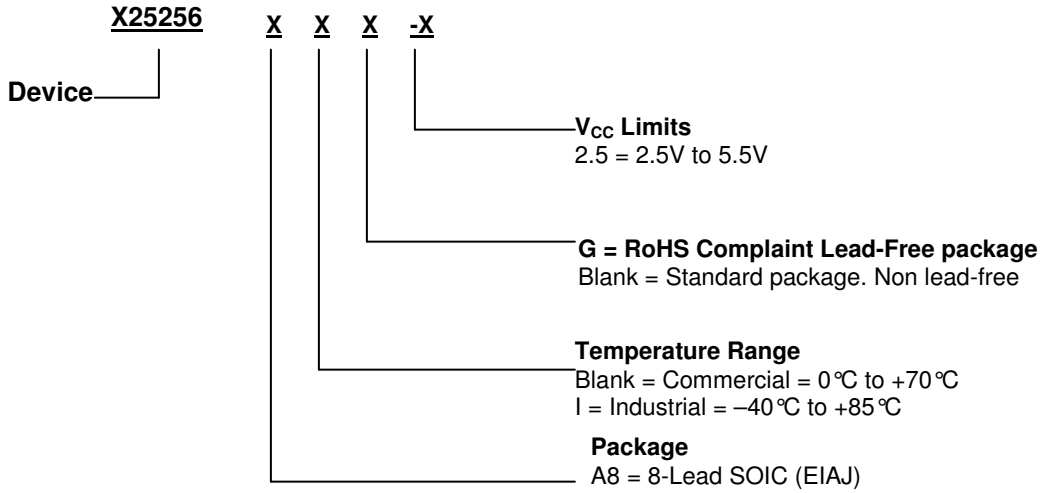
X25256: Bottom View



Dwg Symbol	8-Lead XBGA B Package Min.	8-Lead XBGA B Package Max.
A	0.445	0.470
A1	0.253	0.293
C	0.360	0.388
D	1.940	2.000
E	3.770	3.830
e	1.0 nominal	
F	1.2 nominal	

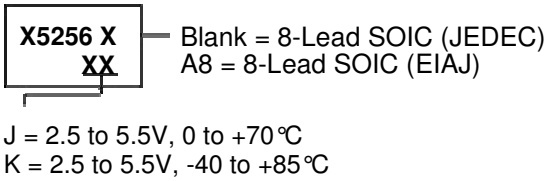
NOTE:ALL DIMENSION IN MM
ALL DIMENSIONS ARE TYPICAL VALUES

Ordering Information



Park Mark Convention

8-Lead SOIC



8-Lead XBGA Complete Part Number	Top Mark
X25256B-2.5	XAAK
X25256BI-2.5	XAAL

20-Lead TSSOP