High-Speed CMOS Bus Interface 8-Bit Latches

QS54/74FCT373T
QS54/74FCT533T

QS54/74FCT2373T
QS54/74FCT2533T

FEATURES/BENEFITS

- Pin and function compatible to the 74F373/533 74FCT373/533 and 74FCT373T/533T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 373T, 533T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std. , A , C, and D speed grades with 4.2ns for D
- Iol = 48 mA Com., 32 mA Mil.

FCT-T 2373T, 2533T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. , A , C, & D speed grades with 4.2ns for D
- Iol = 12mA Com.

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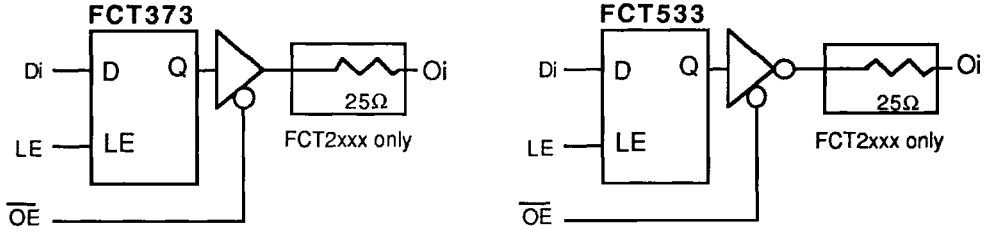
DESCRIPTION

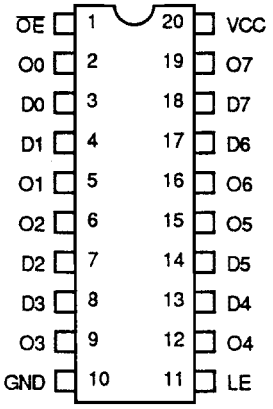
The QSFCT373T and QSFCT533T are 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2373/533 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2373 and 2533 series parts can replace the 373 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

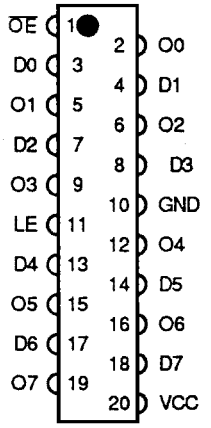


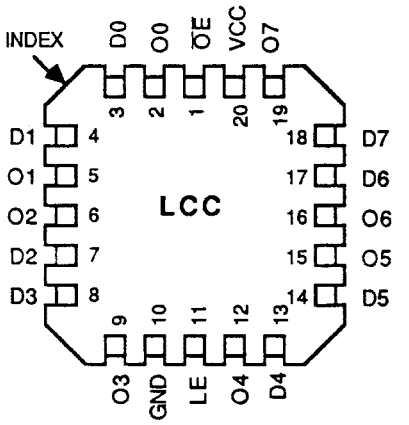
PINOUTS

PDIP, SOIC, QSOP



ZIP





ALL PINS TOP VIEW

PIN DESCRIPTION AND FUNCTION TABLE

FCT373, 2373

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
LE	I/O	Latch Enable
$\overline{OE}$	I/O	Output Enable

Inputs			Internal Q Value	Outputs		Function
				373	533	
$\overline{OE}$	LE	Di		Oi	$\overline{Oi}$	
H	X	X	X	Z	Z	Disable Outputs
L	L	X	H	H	L	Enable Outputs
L	L	X	L	L	H	
L	H	L	L	L	H	Pass Input Data
L	H	H	H	H	L	
L	L	X	Q	Q	$\overline{Q}$	Hold Prior Data

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to 7.0V
DC Input Voltage V_I ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
Maximum Power Dissipation..... 0.5 watts
T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3,4,7,8,11,13,14,17,18	4	4	5	7	pF
2,5,6,9,12,15,16,19	6	6	7	9	pF
———	8	8	9	10	pF

Note: Capacitance is characterized but not tested

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysterisis	Vtlh - Vthl for All Inputs		-	0.2	-	
| Iih | | Iil |	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	µA
| Ioz |	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-225	mA
Ior	Current Drive FCT2XXX	Vcc = Min, Vo =2.0V (3)		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 32 mA (MIL)	-	-	0.50	
			Iol = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	25	-	Ω
			Iol = 12 mA (COM)	20	28	40	

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin =3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description		Notes	373 2373 533 2533		373A 2373A 533A 2533A		373C, 2373C 533C 2533C		373D 2373D		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
t PHL t PLH	Propagation Delay Data to Oi, 373	COM	1	1.5	8	1.5	5.2	1.5	4.2	1.5	3.7	ns
		MIL	1	2	8.5	1.5	5.6					
	Propagation Delay Data to Oi, 2373	COM	1	1.5	8	1.5	5.2	1.5	4.2	1.5	3.7	
		MIL	1	2	8.5	1.5	5.6					
t PHL t PLH	Propagation Delay LE to Oi, 373	COM	1	2	13	2	8.5	2	5.5	1.5	4.9	
		MIL	1	2	14	2	9.8					
	Propagation Delay LE to Oi, 2373	COM	1	2	13	2	8.5	2	5.5	1.5	4.9	
		MIL	1	2	14	2	9.8					
t PZH t PZL	Output Enable Time $\overline{OE}$ to Yi, 373	COM	1	1.5	11	1.5	6.5	1.5	5.5	1.5	5.5	
		MIL	1	1.5	12.5	1.5	7.5					
	Output Enable Time $\overline{OE}$ to Yi, 2373	COM	1	1.5	11	1.5	6.5	1.5	6.2	1.5	6.2	
		MIL	1	1.5	12.5	1.5	7.5					
t PHZ t PLZ	Output Disable Time $\overline{OE}$ to Yi	COM	2	1.5	7	1.5	5.5	1.5	5.0	1.5	5.0	
		MIL	2	1.5	8.5	1.5	6.5					
t S	Data Setup Time Di to LE hi to low	COM		2		2		2		2		
		MIL		2		2						
t H	Data Hold Time Di to LE hi to low	COM		1.5		1.5		1.5		1.5		
		MIL		1.5		1.5						
t W	LE Pulse Width HIGH or LOW	COM	2	6		5		4		4		
		MIL	2	6		6						

Notes:
1) Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) See Test Circuit and Waveforms.