PRELIMINARY **CY2254**

Pentium™ Processor Compatible Clock Synthesizer/Driver

Features

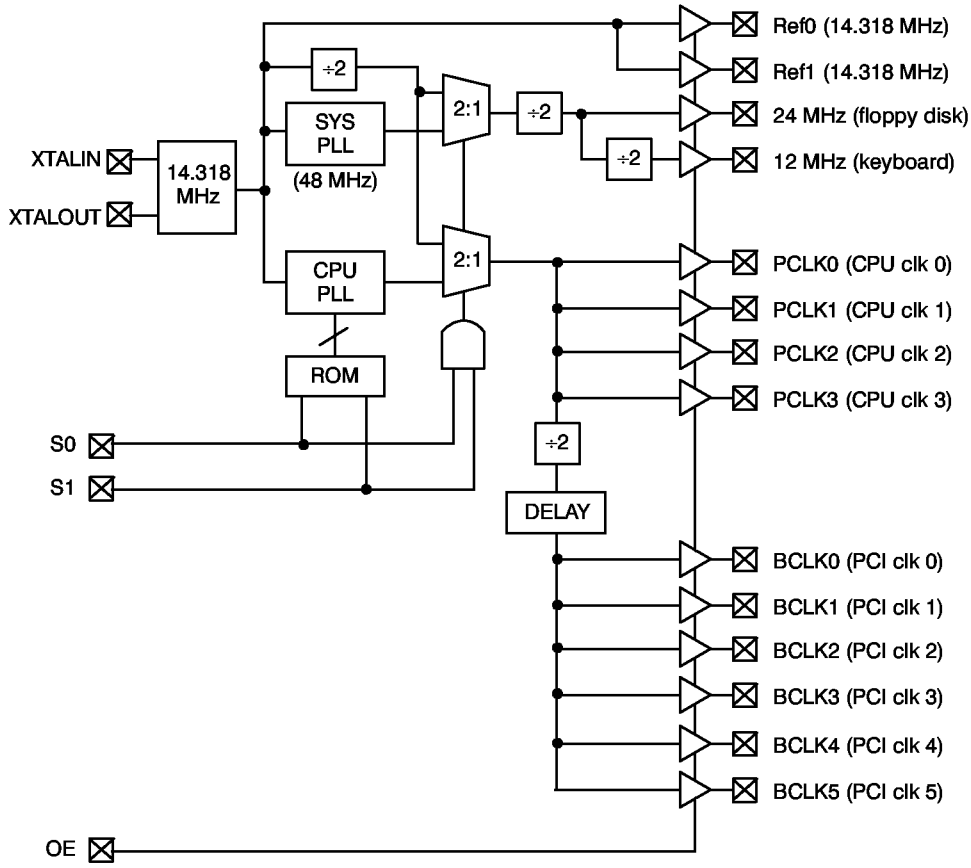
- **Compatible with Intel Triton™ chipset requirements**
- **Multiple clock outputs to meet requirements of most motherboards using Pentium™ processors**
  - **— Four CPU clocks @ 66.66 MHz, 60 MHz, and 50 MHz, pin selectable**
  - **— Six PCI clocks (CPUCLK/2)**
  - **— One Floppy clock @ 24 MHz**
  - **— One Keyboard Controller clock @ 12 MHz**
  - **— Two Ref. clocks @ 14.318 MHz**
  - **— Ref. 14.318 MHz Xtal oscillator input**
- **CPU clock jitter ≤ 200 ps cycle-to-cycle**
- **Low skew outputs**
  - **— ≤ 250 ps between CPU clocks (PCLK)**
  - **— ≤ 500 ps between PCI clocks (BCLK)**
  - **— +1 ns min. to +5 ns max. skew between CPU and PCI Clocks (CPU leads PCI)**
- **Freq. stability = 0.01 % (max.)**
- **Output duty cycle 40% min. to 60% max.**
- **Test mode support**
- **3.3V operation**

Functional Description

The CY2254 is a Clock Synthesizer/Driver chip for the Intel® Pentium processor based PC. The part outputs multiple clocks, to serve the requirements of most motherboards. The CY2254 has low-skew outputs (≤ 250 ps between the CPU Clocks, ≤ 500 ps between the PCI Clocks). In addition, the CY2254 CPU clock outputs have less than 200 ps cycle-to-cycle RMS jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of the Pentium-based system.

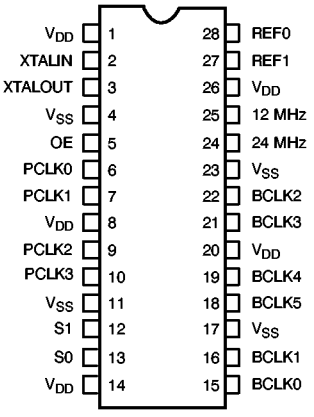
The CY2254 accepts a 14.318 MHz reference signal as its input. The CY2254 has 2 PLLs, one of which generates the CPU and PCI clocks, and the other generates the Floppy Disk and Keyboard Controller clocks. The CY2254 runs off a 3.3V supply.

Logic Block Diagram



Pin Configuration

Top View
SOIC



Note:
PCLK = CPU Clock
BCLK = PCI Bus Clock

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Pin Summary

Name	Number	Description
V_{DD}	1	Digital voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
OE	5	Output Enable, Active HIGH
PCLK0	6	CPU output clock
PCLK1	7	CPU output clock
V_{DD}	8	Digital voltage supply
PCLK2	9	CPU output clock
PCLK3	10	CPU output clock
V_{SS}	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V_{DD}	14	Digital voltage supply
BCLK0	15	PCI output clock
BCLK1	16	PCI output clock
V_{SS}	17	Ground
BCLK5	18	PCI output clock
BCLK4	19	PCI output clock
V_{DD}	20	Digital voltage supply
BCLK3	21	PCI output clock
BCLK2	22	PCI output clock
V_{SS}	23	Ground
24 MHz	24	Floppy disk output clock (24 MHz)
12 MHz	25	Keyboard controller clock (12 MHz)
V_{DD}	26	Digital voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Function Table

OE	S0	S1	XTALIN Input	PCLK	BCLK	Ref. Clock Output	24 MHz	12 MHz
0	X	X	14.31818 MHz	High-Z	High-Z	High-Z	High-Z	High-Z
1	0	0	14.31818 MHz	50 MHz	PCLK/2	14.31818 MHz	24 MHz	12 MHz
1	0	1	14.31818 MHz	60 MHz	PCLK/2	14.31818 MHz	24 MHz	12 MHz
1	1	0	14.31818 MHz	66 MHz	PCLK/2	14.31818 MHz	24 MHz	12 MHz
1	1	1	TCLK[2]	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

PCI Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

CPU Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... −65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_C	Temperature of Case	0	70	°C
C_L	Max. Capacitive Load on PCLK BCLK 24 MHz 12 MHz REF0 REF1		 20 30 20 20 30 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Notes:
2. TCLK is a test clock on the XTAL1 input during test mode.
3. Electrical parameters are guaranteed with these operating conditions.

Electrical Characteristics V_{DD} = 3.3V ±5%, T_C = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = 6 mA	PCLK	2.4		V
			I_{OH} = 12 mA	BCLK, REF0			
			I_{OH} = 4 mA	24, 12 MHz			
			I_{OH} = 8 mA	REF1			
V_{OL}	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 6 mA	PCLK		0.4	V
			I_{OL} = 12 mA	BCLK, REF0			
			I_{OL} = 4 mA	24, 12 MHz			
			I_{OL} = 8 mA	REF1			
I_{IH}	Input High Current	V_{IH} = V_{DD} − 0.5V			−5	+5	µA
I_{IL}	Input Low Current	V_{IL} = 0.5V			−5	+5	µA
I_{OZ}	Output Leakage Current	Three-state			−10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.465, V_{IN} = 0 or V_{DD}				90	mA

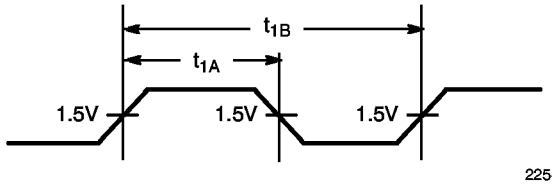
Switching Characteristics[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle[5]	t_1 = t_{1A} ÷ t_{1B}	40%	60%	
t_2	PCLK, BCLK	Output Slew Rate	0.4−2.4V	1		V/ns
t_3	REF, 24, 12 MHz	Rise Time	0.4−2.4V		4	ns
t_4	REF, 24, 12 MHz	Fall Time	2.4−0.4V		4	ns
t_5	PCLK	CPU Skew	CPU-CPU clock skew		250	ps
t_6	BCLK	PCI Skew	PCI-PCI clock skew		500	ps
t_7	PCLK, BCLK	CPU-PCI Skew	CPU to PCI clock skew (CPU leads)	1	5	ns
t_8	PCLK	Cycle-Cycle Clock Jitter	Clock jitter		200	ps

Notes:
4. All parameters specified with outputs fully loaded.
5. Duty cycle is measured at 1.5V.

Switching Waveforms

Duty Cycle Timing



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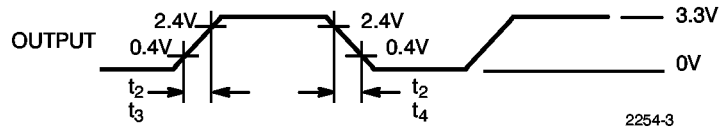
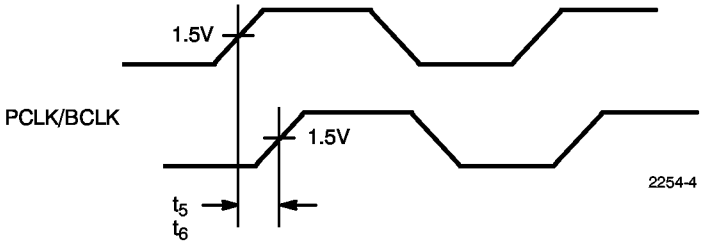
Switching Waveforms (continued)

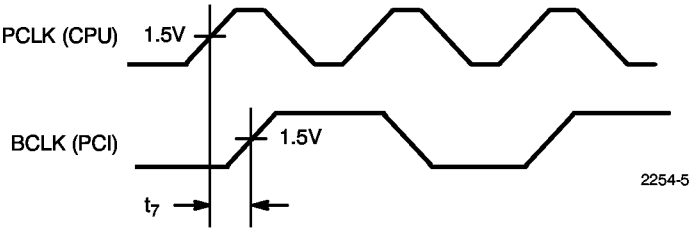
All Outputs Rise/Fall Time



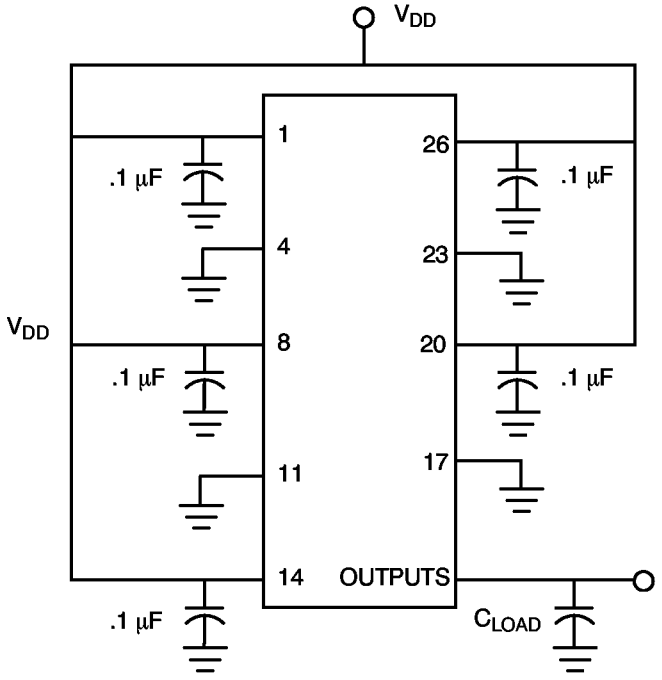
Clock Skew



CPU-PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2254	S	28-Pin SOIC	Commercial

Document #: 38−00426

Package Diagram

28-Lead (300-Mil) Molded SOIC S21