AMERICAN MICROSYSTEMS, INC.

FS71429-01

Programmable 1-PLL LVPECL Clock Generator IC

November 2000

Preliminary Information

1.0 Features

- Single Phase Lock Loop with programmable Feedback and Post Dividers
- Differential 3.3V LVPECL output drive
- Serial three-wire programming interface
- Parallel programming interface for power-on
- Internal crystal reference oscillator and integrated loop filter require no external components
- Output enable provides tristate control of LVPECL clock driver
- Accepts 5MHz to 27MHz crystal resonators
- CMOS version of industry standard x429 device
- Available in 28-pin (0.300") SOIC

2.0 Description

The FS71429 is a general purpose programmable CMOS clock generator IC designed to minimize cost and component count in a variety of high speed electronic systems. Both serial and parallel programming interfaces are provided.

Figure 1: Pin Configuration

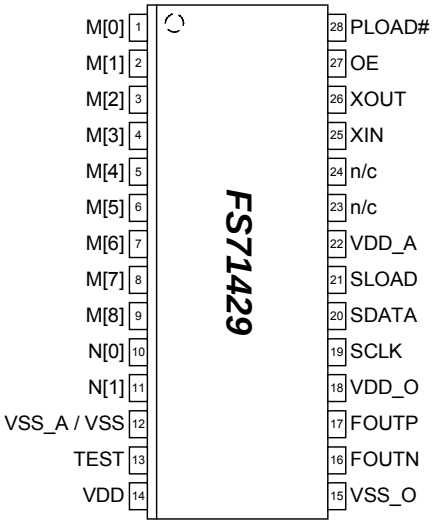
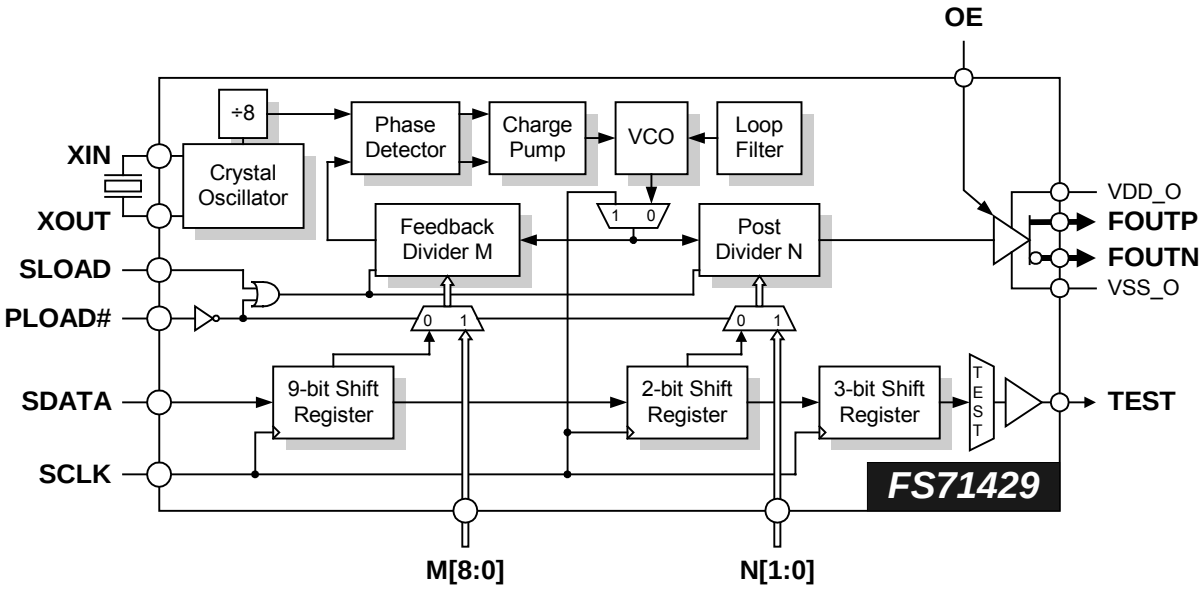


Figure 2: Block Diagram



ISO9001
QS9000

Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	DI^U	M[0]	Feedback Divider modulus 0
2	DI^U	M[1]	Feedback Divider modulus 1
3	DI^U	M[2]	Feedback Divider modulus 2
4	DI^U	M[3]	Feedback Divider modulus 3
5	DI^U	M[4]	Feedback Divider modulus 4
6	DI^U	M[5]	Feedback Divider modulus 5
7	DI^U	M[6]	Feedback Divider modulus 6
8	DI^U	M[7]	Feedback Divider modulus 7
9	DI^U	M[8]	Feedback Divider modulus 8
10	DI^U	N[0]	Post Divider modulus 0
11	DI^U	N[1]	Post Divider modulus 1
			The logic levels on these pins: 1) are sampled and latched on the *low-to-high* transition of PLOAD#, or 2) directly control the Feedback and Post Dividers if PLOAD# is *low*, or 3) are ignored if PLOAD# is *high*.
12	P	VSS / VSS_A	Ground for internal logic and PLL core
13	DO	TEST	LVTTL Test mode output. The function of this pin is controlled by Test Logic enabled through the serial bits T_0:2, as given in Table 3.
14	P	VDD	3.3V power supply for internal logic
15	P	VSS_O	Ground for LVPECL output pins and pre-drivers
16	AO	FOUTN	Low-voltage positive-referenced ECL (LVPECL) output (*complementary*)
17	AO	FOUTP	Low-voltage positive-referenced ECL (LVPECL) output (*true*)
18	P	VDD_O	3.3V power supply for the LVPECL output pins and pre-drivers
19	DI_D	SCLK	LVTTL serial interface clock for data I/O. Data present on SDATA is clocked into the internal serial shift registers on the rising edges (low-to-high transitions) on this pin.
20	DI_D	SDATA	LVTTL serial interface data input into the internal shift registers
21	DI_D	SLOAD	Active-high LVTTL serial load signal latches the contents of the internal serial shift registers into the Feedback and Post Dividers, and Test Logic. The data in the shift registers are: 1) latched into the dividers and test logic on the *high-to-low* transition of SLOAD, or 2) directly control the dividers and test logic if SLOAD is *high*, or 3) are ignored if SLOAD is *low*.
22	P	VDD_A	3.3V power supply for PLL core
23, 24	-	n/c	No connection
25	AI	XIN	Crystal oscillator input
26	AO	XOUT	Crystal oscillator feedback. This pin may be overdriven with an external reference clock if XIN is left floating.
27	DI^U	OE	Active-high LVTTL output enable input
28	DI^U	PLOAD#	Active-low parallel load signal. When this pin is low, the parallel load latches are transparent. Logic levels on pins 1-11 are latched into the device on the low-to-high transition of the PLOAD# pin.

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Preliminary Information

3.0 Device Operation

The phase-locked loop (PLL) is a standard phase- and frequency-locked loop architecture that multiplies a crystal reference frequency to a desired output frequency by a ratio of integers. This frequency multiplication is exact.

As shown in Figure 3, the PLL consists of a fixed divide-by-8 circuit, a Phase-Frequency Detector (PFD), a charge pump, an internal loop filter, a Voltage-Controlled Oscillator (VCO), a Feedback Divider, and a Post Divider.

During operation the crystal frequency (f_{XIN}), generated by the on-board crystal oscillator, is divided by eight and fed into the PFD.

The PFD controls the frequency of the VCO (f_{VCO}) through the charge pump and loop filter. The VCO provides a high-speed, low noise, continuously variable frequency clock source for the PLL. The output of the VCO is fed back to the PFD through the Feedback Divider (the modulus is denoted by M) to close the loop.

The PFD will drive the VCO up or down in frequency until the divided crystal frequency and the divided VCO frequency appearing at the PFD inputs are equal.

The input/output relationship between the crystal frequency and the VCO frequency is

$$f_{VCO} = f_{XIN}\left(\frac{M}{8}\right) \qquad \text{Equation 1}$$

The Post Divider (the modulus is denoted by N) allows the VCO to be operated in a narrower range of frequencies compared to the variety of output clock frequencies that the device is required to generate. The function can be expressed as:

$$f_{OUT} = \left(\frac{f_{VCO}}{N}\right) \qquad \text{Equation 2}$$

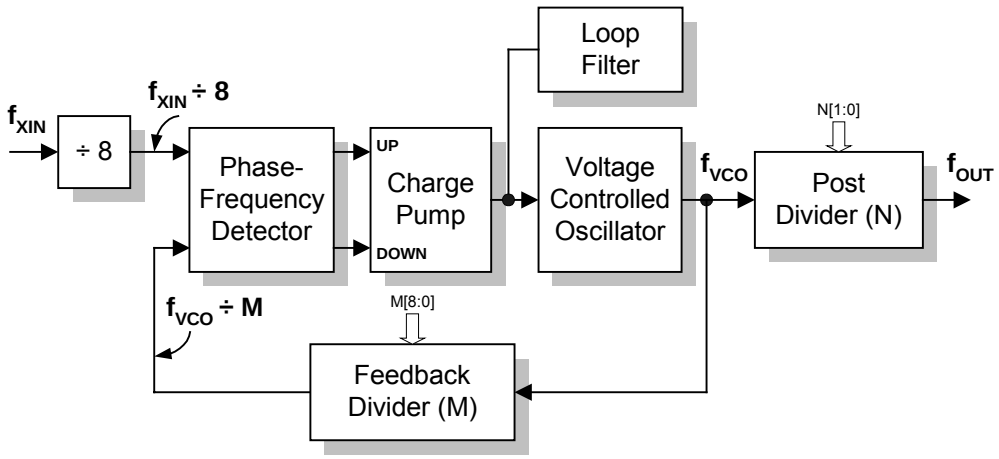
where f_{VCO} is determined in Equation 1.

Taking Equation 1 and 2 together, the basic PLL equation changes to

$$f_{OUT} = f_{XIN}\left(\frac{M}{8}\right)\left(\frac{1}{N}\right) \qquad \text{Equation 3}$$

where *M* and *N* are the Feedback and Post Divider moduli respectively, and f_{OUT} and f_{XIN} are the output and crystal oscillator frequencies.

Figure 3: PLL Diagram



4.0 Register Programming

4.1 Feedback Divider

The Feedback Divider is a straightforward 9-bit divider whose value is directly controlled by the bits M[8:0]. These bits may be programmed in a serial fashion, via SLOAD, SCLK, and SDATA, or in a parallel fashion, via M[8] through M[0], and PLOAD#.

4.2 Post Divider

The Post Divider is controlled by bits N[0] and N[1]. These bits may be programmed serially, through SLOAD, SCLK, and SDATA, or in a parallel fashion, through N[0], N[1], and PLOAD#.

Table 2: Post Divider Function

N[1]	N[0]	POST DIVIDER
0	0	÷ 2
0	1	÷ 4
1	0	÷ 8
1	1	÷ 16

4.3 Test Mode

The Test Mode is accessible only through the serial programming bits T[2:0]. The Mode cannot be programmed through the parallel interface. T[2:0] are cleared to 000 when PLOAD# is low.

When T[2:0] is set to 100, the device is placed in a PLL bypass mode. The clock signal present at SCLK is fed directly into the Feedback (M) and Post (N) dividers, and the Post Divider drives the FOUTP/FOUTN pins, while the Feedback Divider drives the TEST output.

Table 3: Test Mode Function

SERIAL DATA			OUTPUT PIN FUNCTION	
T[2]	T[1]	T[0]	TEST	FOUTP, FOUTN
0	0	0	Shift register data out	f_{VCO} ÷ N
0	0	1	High (1)	f_{VCO} ÷ N
0	1	0	f_{XIN} ÷ 8	f_{VCO} ÷ N
0	1	1	f_{VCO} ÷ M (feedback out)	f_{VCO} ÷ N
1	0	0	f_{VCO} ÷ N	f_{VCO} ÷ N
1	0	1	Low (0)	f_{VCO} ÷ N
1	1	0	SCLK ÷ M	SCLK ÷ N
1	1	1	f_{VCO} ÷ 4N	f_{VCO} ÷ N

Table 4: Feedback Divider Function

M[8]	M[7]	M[6]	M[5]	M[4]	M[3]	M[2]	M[1]	M[0]	FEEDBACK DIVIDER	VCO FREQUENCY (f_{VCO})
256	128	64	32	16	8	4	2	1		
0	1	1	0	0	1	0	0	0	**200**	25.000 x f_{XIN}
0	1	1	0	0	1	0	0	1	**201**	25.125 x f_{XIN}
0	1	1	0	0	1	0	1	0	**202**	25.250 x f_{XIN}
0	1	1	0	0	1	0	1	1	**203**	25.375 x f_{XIN}
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •		
1	1	0	0	0	1	1	0	1	**397**	49.625 x f_{XIN}
1	1	0	0	0	1	1	1	0	**398**	49.750 x f_{XIN}
1	1	0	0	0	1	1	1	1	**399**	49.875 x f_{XIN}
1	1	0	0	1	0	0	0	0	**400**	50.000 x f_{XIN}

NOTE: f_{XIN} is the crystal reference frequency, and f_{VCO} is the VCO frequency, per Figure 3.

5.0 Device Operation

M[8:0] and N[1:0] are expected to be configured on power-up through the parallel programming interface. Once powered up, the M and N dividers can be reprogrammed through the serial interface. In this fashion the device can be powered up with a default output frequency, and then fine-tuned by the user for an alternate output frequency.

As noted in Section 3.0, the output frequency is determined by configuring the Feedback (M) and Post (N) dividers based on the crystal frequency.

$$f_{OUT} = \frac{f_{XTAL}}{8} \times \frac{M}{N}$$

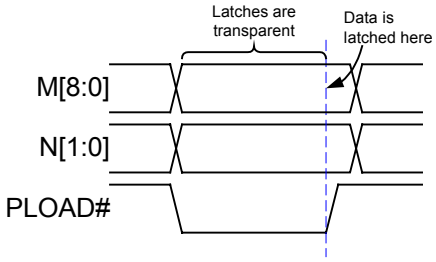
Note that the VCO has a maximum frequency, as given in Table 8. It is possible to program a value of M with a given crystal frequency that may exceed the maximum VCO frequency, so care must be taken to avoid this. The equation for the VCO is given in Equation 1.

5.1 Programming Interface

Both the serial and/or parallel interface can be used to load the Feedback (M) and Post (N) dividers. When using the parallel interface, the logic values present on the M[8:0] and N[1:0] pins determine the divider modulus. A low-to-high transition on PLOAD# latches the information on the M[8:0] and N[1:0] pins into the respective dividers.

When PLOAD# is low, the latches are transparent to the M[8:0] and N[1:0] pins. Therefore, any changes on the M and N pins immediately change the Feedback and Post dividers and directly affect the output frequency present on FOUTP/FOUTN. If the serial interface will be used, PLOAD# should be held high so that the logic levels on the M and N pins will be ignored.

Figure 4: Parallel Programming



To use the serial interface, the SLOAD pin must be held low. The SCLK signal is used to sample data present on SDATA and to load the data into the shift register. For each register the most significant bit is shifted in first (T[2] for the Test Register, N[1] for the Post Divider, and M[8] for the Feedback Divider).

A pulse on the SLOAD pin transfers the shifted data into the Test Register, Post, and Feedback Dividers. A high-to-low transition on SLOAD latches the shifted data.

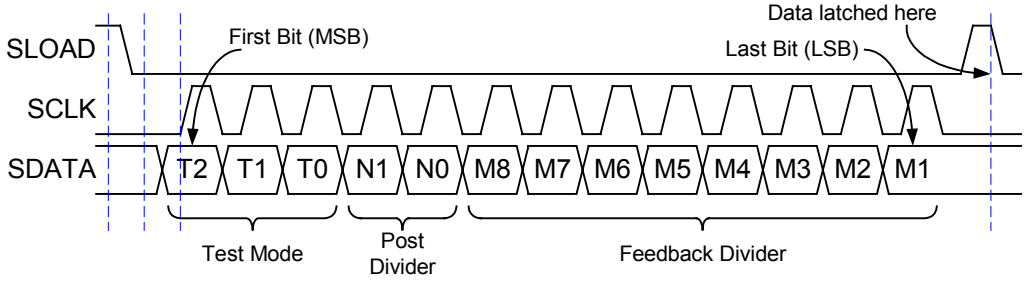
5.2 Oscillator Overdrive

For applications where an external reference clock is provided (and the crystal oscillator is not required), the reference clock should be connected to XOUT and XIN should be left unconnected (float).

For best results, make sure the reference clock signal is as jitter-free as possible, can drive a 40pF load with fast rise and fall times, and can swing rail-to-rail.

If the reference clock is not a rail-to-rail signal, the reference must be AC coupled to XOUT through a 0.01µF or 0.1µF capacitor. A minimum 1V peak-to-peak signal is required to drive the internal differential oscillator buffer.

Figure 5: Serial Programming



6.0 Electrical Specifications

Table 5: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	4.0	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 6: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}, V_{DD_A}	3.3V ± 10%	3	3.3	3.6	V
	V_{DD_O}	3.3V ± 10%	3	3.3	3.6	
Ambient Operating Temperature Range	T_A	Commercial	0		70	°C
Crystal Resonator Frequency	f_{XIN}		5		27	MHz
Crystal Resonator Loading Capacitance	C_{XL}	As seen by an external crystal between XIN and XOUT		18		pF

Table 7: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 3.3V, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σfrom typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic	I_{DD}	f_{XIN} = 16.667MHz, f_O = 200MHz		56		mA
Supply Current, Static	I_{DDL}	f_{XIN} = 16.667MHz, outputs disabled (OE low)		50		mA
Parallel Interface Inputs (M[8:0], N[1:0], PLOAD#), Output Enable Input (OE)						
High-Level Input Voltage	V_{IH}	V_{DD} = 3.6V	2.0		V_{DD} + 0.3	V
Low-Level Input Voltage	V_{IL}	V_{DD} = 3.6V	V_{SS} – 0.3		0.8	V
High-Level Input Current	I_{IH}				1	µA
Low-Level Input Current (pull-up)	I_{IL}	V_I = 0V		-26		µA
Serial Interface Inputs (SLOAD, SCLK, SDATA)						
High-Level Input Voltage	V_{IH}	V_{DD} = 3.6V	2.0		V_{DD} + 0.3	V
Low-Level Input Voltage	V_{IL}	V_{DD} = 3.6V	V_{SS} – 0.3		0.8	V
High-Level Input Current (pull-down)	I_{IH}	V_I = 3.6V		26		µA
Low-Level Input Current	I_{IL}		-1			µA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}	V_{DD} = 3.6V		1.7		V
High-Level Input Current	I_{IH}			42		µA
Low-Level Input Current	I_{IL}	V_{DD} = 3.6V		-42		µA
Crystal Oscillator Drive (XOUT)						
High-Level Output Source Current	I_{OH}	V_{DD} = V(XIN) = 3.6V, V_O = 0V		-13		mA
Low-Level Output Sink Current	I_{OL}	V_{DD} = V_O = 3.6V, V(XIN) = 0V		10		mA
Input Loading Capacitance *	$C_{L(XOUT)}$	As seen by an external clock driver on XOUT; XIN unconnected		36		pF
Test Output (TEST)						
High-Level Output Source Current	I_{OH}	V_O = 2.4V		-2.0		mA
Low-Level Output Sink Current	I_{OL}	V_O = 0.4V		2.0		mA
LVPECL Clock Outputs (FOUTP, FOUTN)						
High-Level Output Voltage	V_{OH}	50Ω to V_{DD_O} – 2.0V, V_{DD_O} = 3.3V	V_{DD_O} – 1.075		V_{DD_O} – 0.830	V
Low-Level Output Voltage	V_{OL}	50Ω to V_{DD_O} – 2.0V, V_{DD_O} = 3.3V	V_{DD_O} – 1.860		V_{DD_O} – 1.570	V
Crossover Voltage	V_X	50Ω to V_{DD_O} – 2.0V, V_{DD_O} = 3.3V		1.92		V
Common Mode Voltage (peak-peak)	V_{CM}	50Ω to V_{DD_O} – 2.0V, V_{DD_O} = 3.3V		250		mV
Differential Swing	V_{PP}	50Ω to V_{DD_O} – 2.0V, V_{DD_O} = 3.3V				
Low-Level Output Sink Current	I_{OL}	V_O = 1.44V				mA
Tristate Output Current	I_Z		-10		10	µA
Short Circuit Sink Current *	I_{SCL}	V_{DD} = V_O = 3.6V, shorted for 30s, max.		32		mA

Table 8: AC Timing Specifications

Unless otherwise stated, V_{DD} = 3.3V, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σfrom typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Overall							
Output Frequency *	f_O					500	MHz
VCO Frequency *	f_{VCO}					1000	MHz
Tristate Enable Delay *	t_{PZL}, t_{PZH}			1		8	ns
Tristate Disable Delay *	t_{PLZ}, t_{PHZ}			1		8	ns
Clock Stabilization Time *	t_{STB}					3	ms
Divider Modulus							
Feedback Divider	M			1		511	
Post Divider	N			2		16	
Interface Timing Specifications							
SCLK Frequency						10	MHz
Setup Time	t_{SU}	SDATA to SCLK		20			ns
		SCLK to SLOAD		20			
		M, N to PLOAD#		20			
Hold Time	t_{HD}	SDATA to SCLK		20			ns
		M, N to PLOAD#		20			
Pulse Width	t_{pw}	SLOAD		50			ns
		PLOAD#		50			
LVPECL Clock Outputs (FOUTP, FOUTN)							
Duty Cycle *	d_C	Ratio of high pulse width to one clock period, measured at V_X	200.0	45	49	55	%
Jitter, Cycle-to-Cycle (peak-peak)*	$t_{j(CC)}$	From rising edge to the next rising edge at V_X over 10k cycles, f_{XIN}=16.667MHz, M=24, N=2	200.0	-50		+50	ps
Rise Time *	t_r	20% to 80%, 50Ω to V_{DD_O} – 2.0V			420		ps
Fall Time *	t_f	80% to 20%, 50Ω to V_{DD_O} – 2.0V			440		ps

Figure 6: Serial Timing

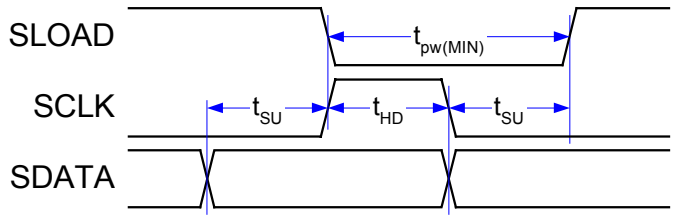
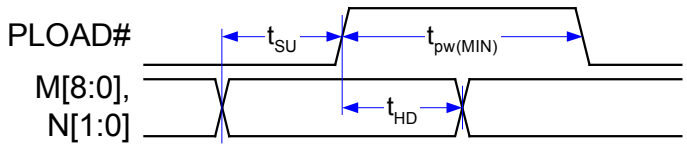


Figure 7: Parallel Timing



7.0 Package Information

Table 9: 28-pin SOIC (0.300") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.0926	0.1043	2.35	2.65
A1	0.0040	0.0118	0.10	0.30
b	0.0130	0.0200	0.33	0.51
C	0.0091	0.0125	0.23	0.32
D	0.6969	0.7125	17.70	18.10
E	0.2914	0.2992	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.029	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

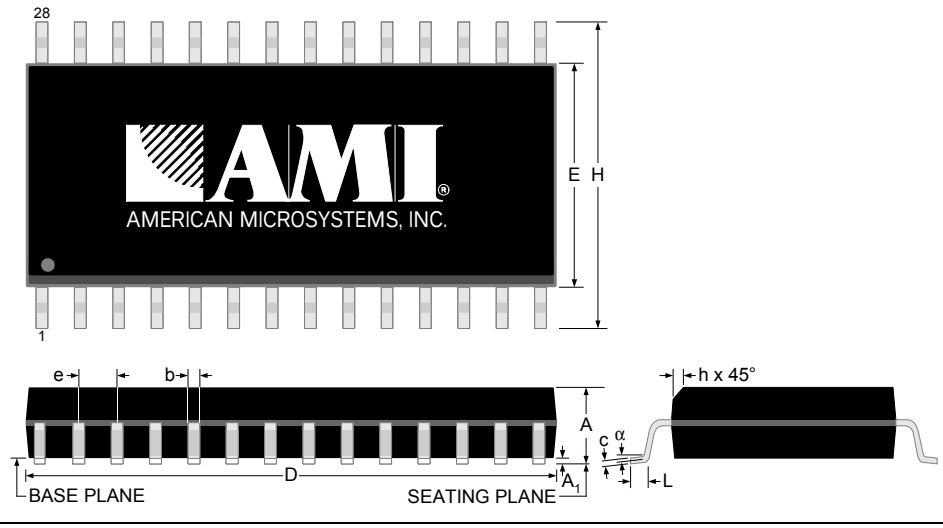


Table 10: 28-pin SOIC (0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s, single-layer PCB	77	°C/W
Lead Inductance, Self	L_{11}	Corner lead, plus wire	5.914	nH
		Center lead, plus wire	2.187	
Lead Inductance, Mutual	L_{12}	Corner lead plus wire, to first adjacent lead	2.240	nH
		Center lead plus wire, to first adjacent lead	0.647	
	L_{13}	Corner lead plus wire, to next adjacent lead	1.108	
		Center lead plus wire, to next adjacent lead	0.366	
Lead Capacitance, Bulk	C_{11}	Any corner lead plus wire to V_{SS}	1.173	pF
		Any center lead plus wire to V_{SS}	0.419	
Lead Capacitance, Mutual	C_{12}	Any corner lead plus wire to first adjacent lead	0.463	pF
		Any center lead plus wire to first adjacent lead	0.084	
	C_{13}	Any corner lead plus wire to next adjacent lead	0.045	
		Any center lead plus wire to next adjacent lead	0.013	

8.0 Ordering Information

8.1 Device Ordering Codes

DEVICE NUMBER	FONT	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS71429	-01	13715-801	28-pin (0.300") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tape-and-Reel

American Microsystems, Inc., 2300 Buckskin Rd., Pocatello, ID 83201, (208) 233-4690, FAX (208) 234-6796, WWW Address: http://www.amis.com E-mail: tgp@amis.com