IC WORKS

W42C07A

PRELIMINARY, APRIL 1994

CPU Frequency Generator

FEATURES

- **Small 8 Pin SOIC/DIP package**
- **Synthesizes 4 programmable frequencies from 2MHz to 120MHz**
- **Supports 3.3V and 5.0V operation**
- **Smooth, glitch-free frequency transitions**
- **Advanced PLL design with low phase jitter**
- **Reference and synthesized clocks**
- **High performance, low power CMOS design with on chip loop filter**
- **TTL or CMOS input level compatible**
- **Ideal replacement for crystal oscillators**
- **W42C07A-01 is pin and functional compatible with AV9107-05**

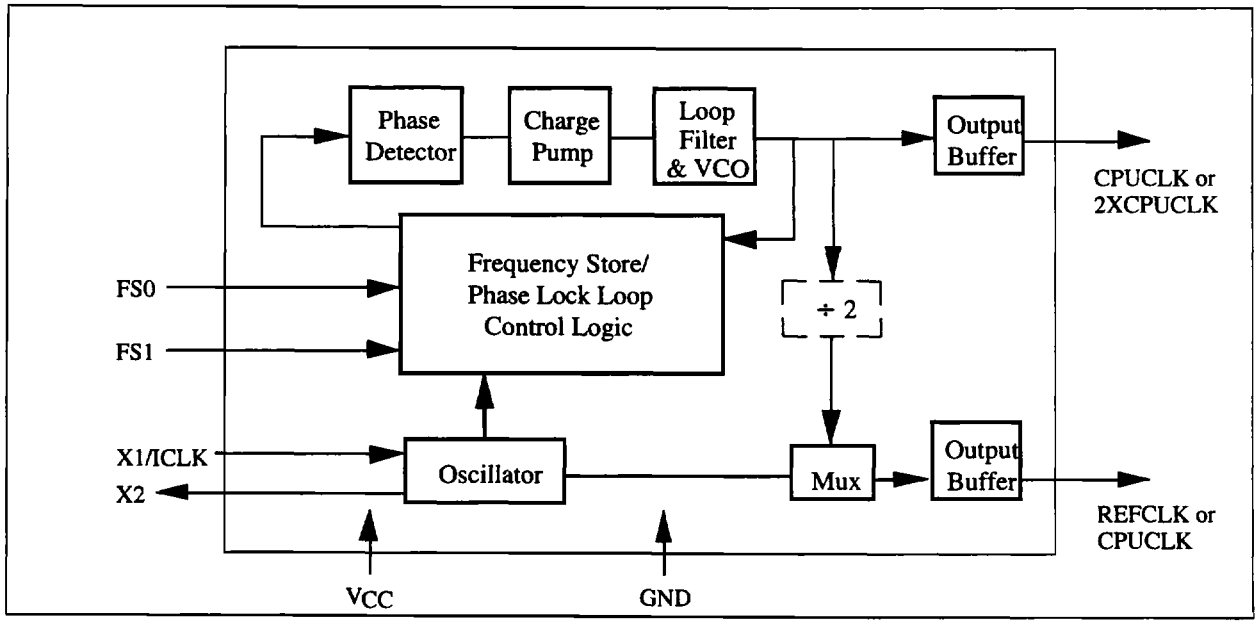
FUNCTIONAL DESCRIPTION

The W42C07A is a solution for generating two simultaneous clocks while using minimum board space. One clock (REFCLK) is a fixed output frequency which is the same as the input reference crystal (or clock). The other clock (CPUCLK) can vary between 2 and 120MHz with up to 4 selectable programmed frequencies stored in internal ROM.

Included in the W42C07A's advanced feature set is an on-chip loop filter, providing jitter free operation with only two decoupling capacitors. The W42C07A offers smooth and glitch-free transitions when switching from one frequency to another. This feature can be utilized in power management systems such as "green" PCs, notebooks and palmtop computers where it is frequently necessary to slow down the clock to preserve power. The device is designed to be compatible with the Intel cycle to cycle timing specifications for the 80486 processors.

The W42C07A (see Table 1) is an ideal solution for replacing high speed oscillators in computers for CPU clock generation.

FUNCTIONAL BLOCK DIAGRAM: W42C07A



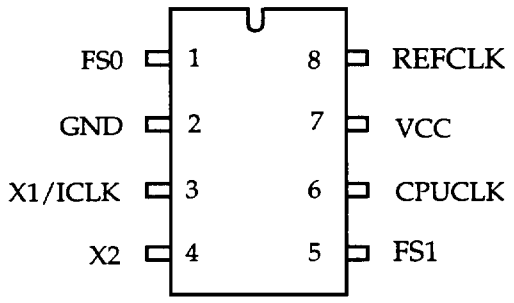
PIN DESCRIPTIONS

Pin Name	Input/ Output	Pin Description
2XCPUCLK	O	Clock output (refer to Frequency Selection Table)
CPUCLK	O	Clock output (refer to Frequency Selection Table)
FS0	I	Frequency selection input, LSB (Note 1)
FS1	I	Frequency selection input (Note 1)
GND	-	Ground connection
REFCLK	O	Reference Clock output, outputs crystal or input clock frequency
VCC	-	Power Supply connection
X1/ICLK	I	Crystal connection or external clock frequency input
X2	O	Crystal connection. leave unconnected when using external clock

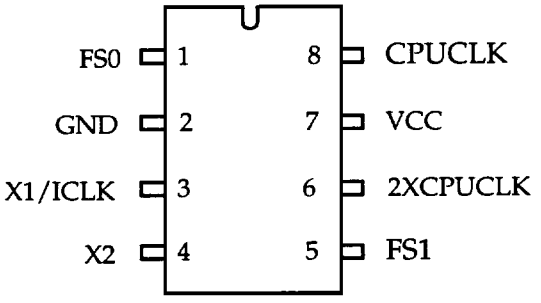
Note 1: All inputs, except for X1/ICLK, have an internal pull up resistor. Unconnected inputs will assume a logic high condition.

PIN CONFIGURATIONS

ω 42C07A-01
ω 42C07A-10
Top View



ω 42C07A-06
Top View



FREQUENCY SELECTION FOR ω42C07A (using 14.318MHz input; 3.3V and 5.0V)

IC WORKS Part Number	ω42C07A-01	ω42C07A-06		ω42C07A-10
Cross Reference	AV9107-05	N/A		AV9107-10
FS1, FS0	CPUCLK (MHz)	CPUCLK (MHz)	2XCPUCLK (MHz)	CPUCLK (MHz)
00	40	25	50	25
01	50	33.3	66.6	33.3
10	66.6	40	80	40
11	80	50 (Note 2)	100 (Note 2)	50
REFCLK	14.318	N/A		14.318

Note 2: Not guaranteed when Vcc < 4.5V.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Voltage on Any Pin with Respect to Ground	V_{CC},V_{IN}	-0.5 to 7.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Ambient Temperature Under Bias	T_B	-55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

Note 1: Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AT 5V

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$) (Note 2)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Note 2		10	20	mA
Input Low Voltage	V_{IL}	$V_{CC} = 5V$			0.8	V
Input High Voltage	V_{IH}	$V_{CC} = 5V$	2.0			V
Output Low Voltage	V_{OL}	$I_{OL} = 8$ mA			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4			V
Output Freq. Change	F_D	Over supply and temperature		.002	.01	%
Input Capacitance	C_I	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		20		pF
Input Low Current	I_{IL}	$V_{IN} = 0V$ (includes pull-up res.)			-10	µA
Input High Current	I_{IH}	$V_{IN} = V_{CC}$			10	µA
Input Pull-Up Resistor	R_P	$V_{IN} = 0V$		250		kΩ

Note 2: With no load, 14.318MHz crystal input, and CLK1 running at 40MHz. Power supply current varies with frequency and output load capacitance.

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_W	20			ns
Setup Time Data to Enable	T_{SU}	20			ns
Output Frequency (CPUCLK & 2XCPUCLK)	F_O	2		120	MHz
Input Frequency	F_I	2	14.318	32	MHz
Hold Time Data to Enable	T_{HD}	10			ns
Input Clock Rise Time	$ICLK_R$			20	ns
Input Clock Fall time	$ICLK_F$			20	ns
Output Rise Time, 0.8 to 2.0V, 25pF load	T_R		1	2	ns
Rise Time, 20 to 80% V_{CC}, 25pF load	T_R		2	4	ns
Output Fall Time, 2.0 to 0.8V, 25pF load	T_F		1	2	ns
Fall Time, 80 to 20% V_{CC}, 25pF load	T_F		2	4	ns
Duty Cycle, 15pF load	D_T	40	50/50	60	%
Jitter, 1 Sigma, all frequencies	T_{J1S}		±0.5	±2	%
Jitter, Absolute, all frequencies	T_{JABS}		±3	±5	%
Fequency Transition Time, 50 to 4MHz	T_{FT}			20	ms
Powerup Time, off to 100MHz	T_{PU}		15	30	ms
Clock Skew, CPUCLK vs 2xCPUCLK (-06)	T_{SK}		±0.5	±1.0	ns

ELECTRICAL CHARACTERISTICS AT 3.3V

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 3.3V \pm 10\%$) (Note 2)

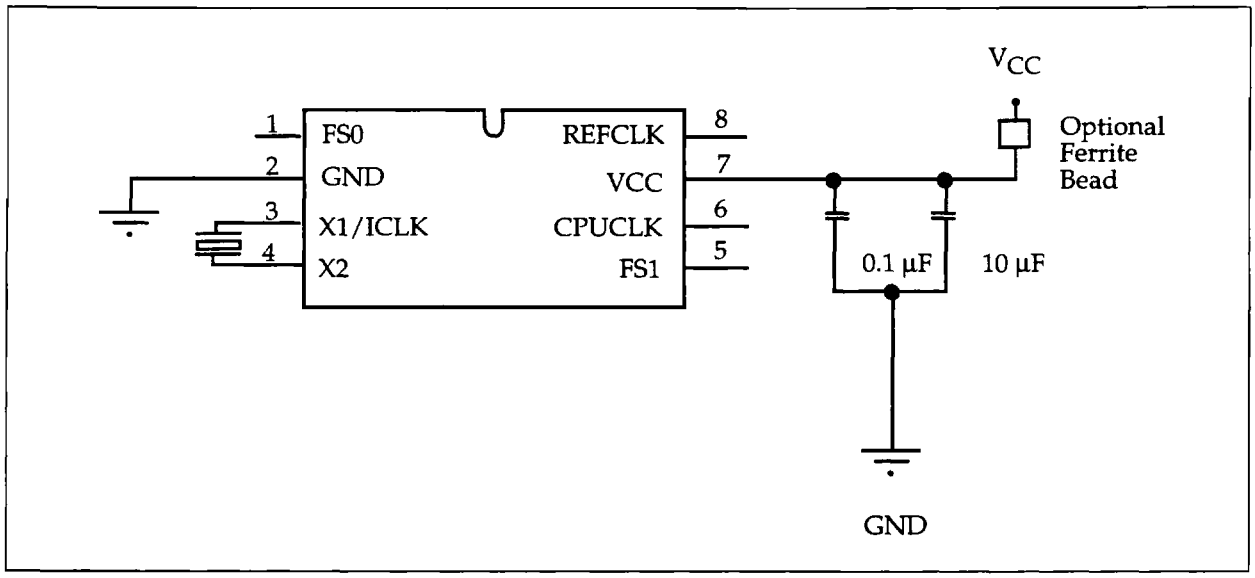
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Note 2		8	16	mA
Input Low Voltage	V_{IL}	$V_{CC} = 3.3V$			0.15Vcc	V
Input High Voltage	V_{IH}	$V_{CC} = 3.3V$	0.7Vcc			V
Output Low Voltage	V_{OL}	$I_{OL} = 8$ mA			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4			V
Output Freq. Change	F_D	Over supply and temperature		.002	.01	%
Input Capacitance	C_I	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		20		pF
Input Low Current	I_{IL}	$V_{IN} = 0V$ (incl. pull-up res.)			-10	µA
Input High Current	I_{IH}	$V_{IN} = V_{CC}$			10	µA
Input Pull-Up Resistor	R_P	$V_{IN} = 0V$		250		kΩ

Note 2: With no load, 14.318MHz crystal input, and CLK1 running at 40MHz. Power supply current varies with frequency and output load capacitance.

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 3.3V \pm 10\%$)

Parameter	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_W	20			ns
Setup Time Data to Enable	T_{SU}	20			ns
Output Frequency (CPUCLK & 2XCPUCLK)	F_O	2		80	MHz
Input Frequency	F_I	2	14.318	32	MHz
Hold Time Data to Enable	T_{HD}	10			ns
Input Clock Rise Time	$ICLK_R$			20	ns
Input Clock Fall time	$ICLK_F$			20	ns
Rise Time, 20 to 80% V_{CC}, 15pF load	T_R		2	4	ns
Fall Time, 80 to 20% V_{CC}, 15pF load	T_F		2	4	ns
Duty Cycle, 15pF load	D_T	40	50/50	60	%
Jitter, 1 Sigma, all frequencies	T_{J1S}		±0.5	±2	%
Jitter, Absolute, all frequencies	T_{JABS}		±3	±5	%
Fequency Transition Time, 50 to 4MHz	T_{FT}			20	ms
Powerup Time, off to 100MHz	T_{PU}		15	30	ms
Clock Skew, CPUCLK vs 2xCPUCLK (-06)	T_{SK}		±0.5	±1.0	ns

RECOMMENDED CIRCUIT CONFIGURATION



ω42C07A RECOMMENDED BOARD LAYOUT

For optimum performance in system applications the above power supply decoupling scheme should be used. All GND pins are connected directly to the ground plane. All VCC connections are connected directly to the power plane.

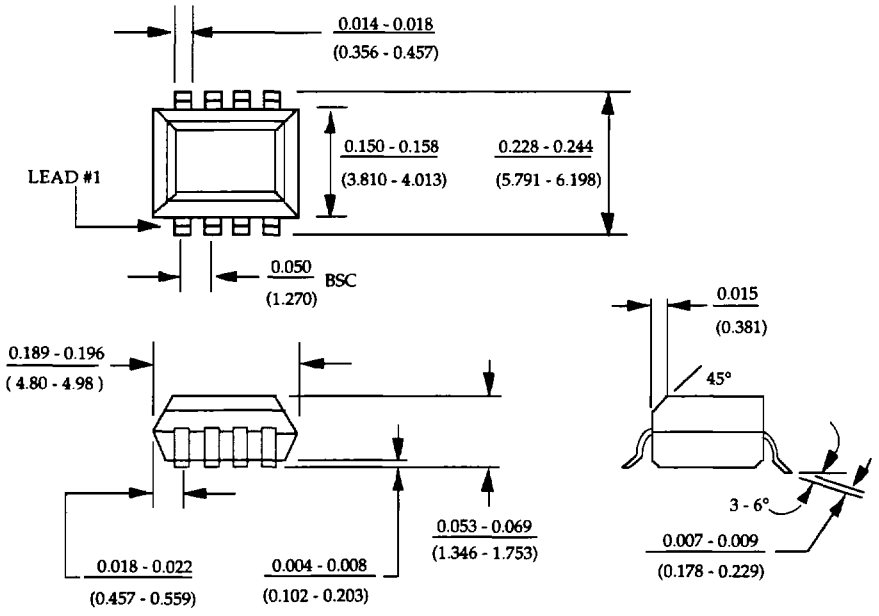
VCC decoupling is important to both reduce phase jitter and EMI radiation. The 0.1µf decoupling capacitor should be placed as close to its VCC pin as possible, otherwise the increased trace inductance will negate its decoupling capability. The 10µf decoupling capacitor shown should be a tantalum type. For further EMI protection, the VCC connection can be made via a ferrite bead, as shown above.

An isolated ground plane should not be used, even though this is a common recommendation. An isolated ground plane only works well when the clock source and load share the same isolated ground area. Ground plane isolation will only cause increased EMI, ground bounce, and in many cases increased output clock jitter.

When using the ω42C07A, unused input select pins can be left floating since internal pull-up resistors are incorporated (hence a floating input will assume a logic 1 condition). Output clocks should utilize a series termination resistor (about 33Ω) placed as close to the clock outputs as possible; this will also help to decrease jitter and EMI.

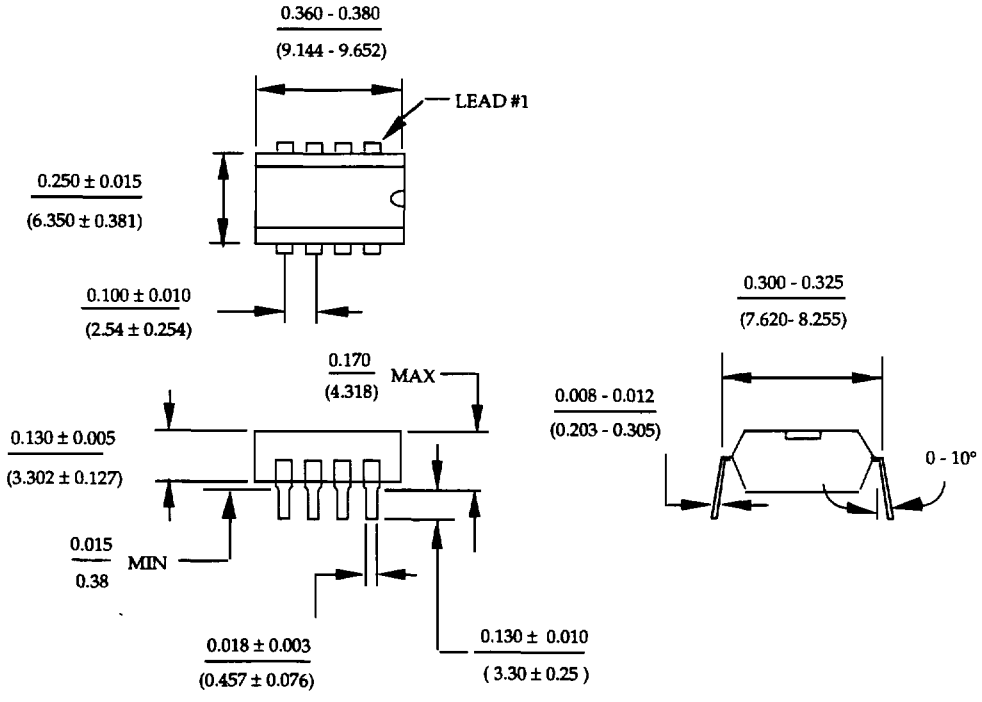
PACKAGING INFORMATION

Plastic SOIC (8pin, 150mil)



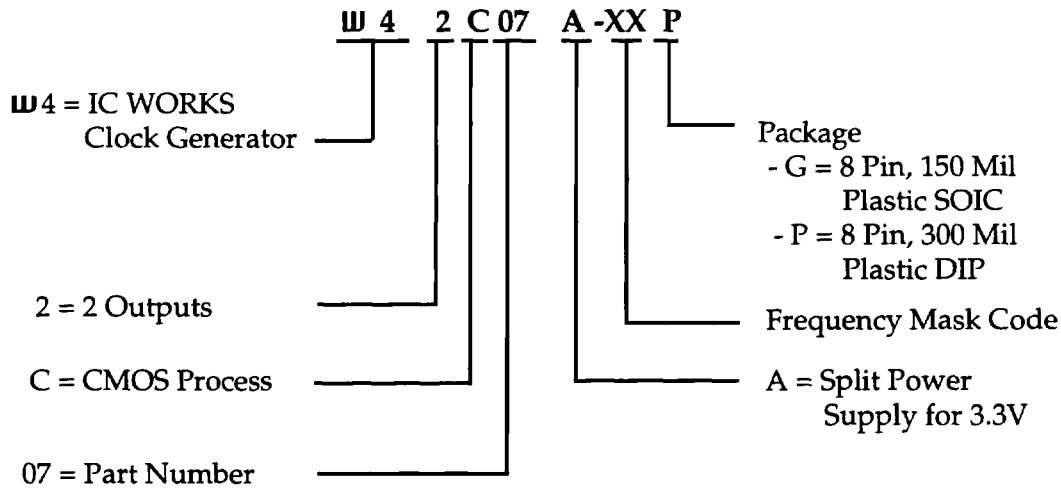
Note: All linear dimensions are in inches and parenthetically in millimeters, min-max.

Plastic DIP (8pin, 300mil)



Note: All linear dimensions are in inches and parenthetically in millimeters, min-max.

ORDERING INFORMATION



VALID PART NUMBERS

ɯ42C07A-01G	ɯ42C07A-06G	ɯ42C07A-10G
ɯ42C07A-01P	ɯ42C07A-06P	ɯ42C07A-10P

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