ROHM SEMICONDUCTOR

Technical Note

High-performance Clock Generator Series

Compact 1ch Clock Generators for Digital Cameras

Pb Free ROHM Electronic Components

RoHS Directive Compliance

BU7344HFV,BU7345HFV,BU7346GUL

No.11005EAT06

●Description

These Clock Generators incorporates compact package compared to oscillators, which provides the generation of high-frequency CCD clocks necessary for digital still cameras and digital video cameras.

●Features

1) SEL pin allowing for the selection of frequencies
2) Selection of OE (PDB) pin enabling Power-down function
3) Crystal-oscillator-level clock precision with high C/N characteristics and low jitter
4) Micro miniature Package incorporated
5) Single power supply of 3.3 V

●Applications

Digital Still Camera, Digital Video Camera, and others

●Line up matrix

Parameter	BU7344HFV	BU7345HFV	BU7346GUL
Supply voltage	2.7V～3.6V	2.7V～3.6V	2.7V～3.6V
Operating temperature range	-5 ℃～75 ℃	-5 ℃～75 ℃	-5 ℃～75 ℃
Reference input clock	27.0000MHz	27.0000MHz	27.0000MHz
Output clock	40.5000MHz	38.0000MHz	38.0000MHz
	36.0000MHz	36.0000MHz	36.0000MHz
Standby current(MAX.)	1.0μA	1.0μA	1.0μA
Operating current (TYP)	4.0mA	3.5mA	3.5mA
Package	HVSOF6	HVSOF6	VCSP50L1 1.5mm×1.0mm

●Absolute maximum ratings (Ta=25 ℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 ~ 4.0	V
Input voltage	VIN	-0.3 ~ VDD+0.3	V
Storage temperature range	Tstg	-55 ~ 125	℃
Power dissipation	Pd	410(BU7344HFV,BU7345HFV)[*1]	mW
		460(BU7346GUL)[*2]	

*1 Mounted on 70mm * 70mm * 1.6mm Glass-epoxy PCB. Derating: 4.1mW / ℃ at Ta > 25°C
*2 Mounted on 50mm * 58mm * 1.75mm Glass-epoxy PCB. Derating: 4.6mW / ℃ at Ta > 25°C
* Operating is not guaranteed.
* The radiation-resistance design is not carried out.

●Operating conditions

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	2.7 ~ 3.6	V
Input H voltage	VINH	0.8VDD ~ VDD	V
Input L voltage	VINL	0.0 ~ 0.2VDD	V
Operating temperature	Topr	-5 ~ 75	℃
Output load	CL	15(MAX.)	pF

●Electrical characteristics

○BU7344HFV (Ta=25 ℃, VDD=3.3V, Crystal frequency=27.0000MHz, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output H voltage	VOH	2.8	-	VDD	V	IOH = -3.0mA
Output L voltage	VOL	0.0	-	0.5	V	IOL = 3.0mA
Standby current	IDDst	-	-	1.0	μA	OE = L
Consumption current 1	IDD1	-	4.0	5.2	mA	40.5000MHz output SEL = L
Consumption current 2	IDD2	-	3.5	4.6	mA	36.0000MHz output SEL = H
Pull-down load	Rpd	50	100	200	kΩ	input PIN, pull-down load value
Output frequency						
OUT1	CLK40.5	40.5000			MHz	IN*12/4/2, SEL = L
OUT2	CLK36	36.0000			MHz	IN*8/3/2, SEL = H

* The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

○BU7345HFV (Ta=25 ℃, VDD=3.3V, Crystal frequency=27.0000MHz, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output H voltage	VOH	2.8	-	VDD	V	IOH = -3.0mA
Output L voltage	VOL	0.0	-	0.5	V	IOL = 3.0mA
Standby current	IDDst	-	-	1.0	μA	OE = L
Consumption current 1	IDD1	-	3.5	4.6	mA	38.0000MHz output SEL = L
Consumption current 2	IDD2	-	3.5	4.6	mA	36.0000MHz output SEL = H
Pull-down load	Rpd	50	100	200	kΩ	input PIN, pull-down load value
Output frequency						
OUT1	CLK38	38.0000			MHz	IN*76/27/2, SEL = L
OUT2	CLK36	36.0000			MHz	IN*8/3/2, SEL = H

* The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to IN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

○BU7346GUL (Ta=25 ℃, VDD=3.3V, Crystal frequency=27.0000MHz, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output H voltage	VOH	2.8	-	VDD	V	IOH = -3.0mA
Output L voltage	VOL	0.0	-	0.5	V	IOL = 3.0mA
Standby current	IDDst	-	-	1.0	μA	PDB = L
Consumption current 1	IDD1	-	3.5	4.6	mA	38.0000MHz output SEL = L
Consumption current 2	IDD2	-	3.5	4.6	mA	36.0000MHz output SEL = H
Pull-down load	Rpd	50	100	200	kΩ	input PIN, pull-down load value
Output frequency						
OUT1	CLK38	38.0000			MHz	XIN*76/27/2, SEL = L
OUT2	CLK36	36.0000			MHz	XIN*8/3/2, SEL = H

* The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to XIN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

●**Reference data** (BU7344HFV basic data)

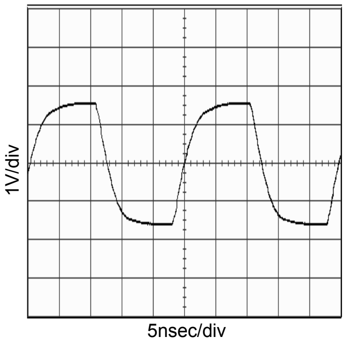


Fig.1 40.5MHz output waveform
(CL=15pF,Ta=25 ℃)

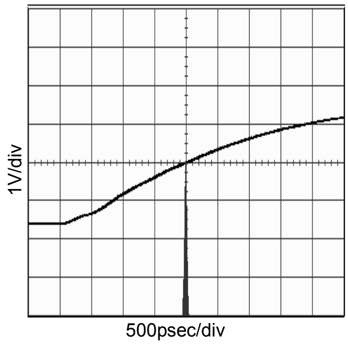


Fig.2 40.5MHz Period-Jitter
(CL=15pF,Ta=25 ℃)

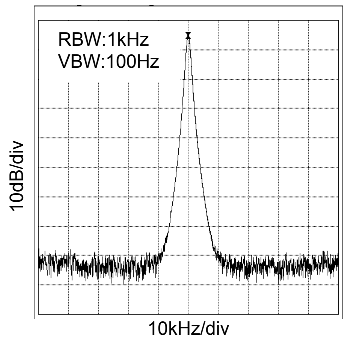


Fig.3 40.5MHz spectrum
(CL=15pF,Ta=25 ℃)

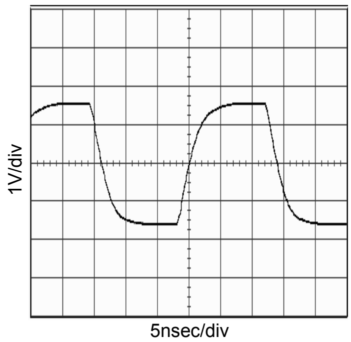


Fig.4 36MHz output waveform
(CL=15pF,Ta=25 ℃)

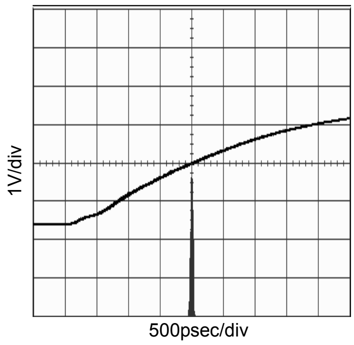


Fig.5 36MHz Period-Jitter
(CL=15pF,Ta=25 ℃)

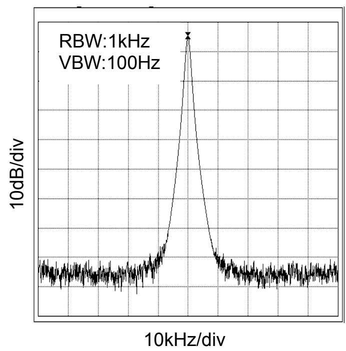


Fig.6 36MHz spectrum
(CL=15pF,Ta=25 ℃)

●**Reference data** (BU7345HFV basic data)

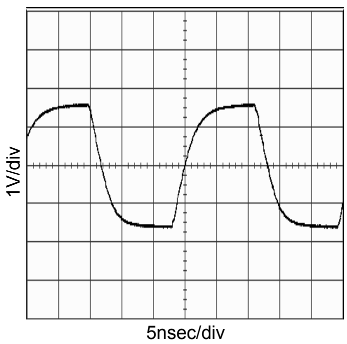


Fig.7 38MHz output waveform
(CL=15pF,Ta=25 ℃)

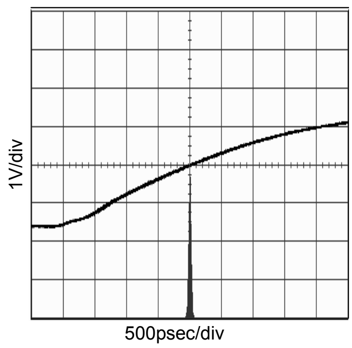


Fig.8 38MHz Period-Jitter
(CL=15pF,Ta=25 ℃)

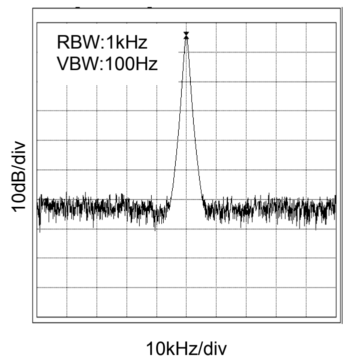


Fig.9 38MHz spectrum
(CL=15pF,Ta=25 ℃)

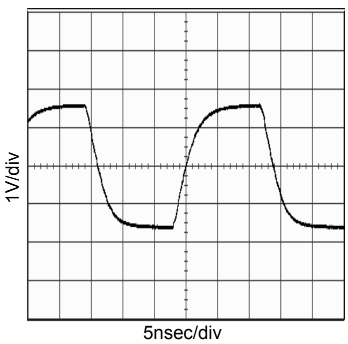


Fig.10 36MHz output waveform
(CL=15pF,Ta=25 ℃)

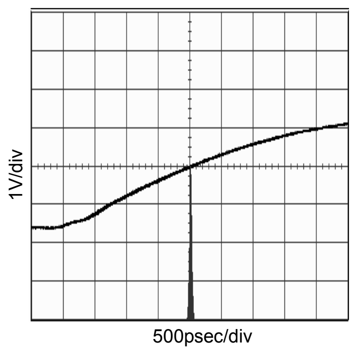


Fig.11 36MHz Period-Jitter
(CL=15pF,Ta=25 ℃)

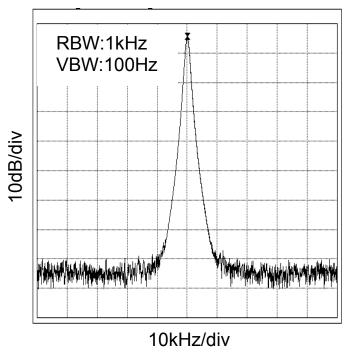


Fig.12 36MHz spectrum
(CL=15pF,Ta=25 ℃)

●**Reference data** (BU7346GUL basic data)

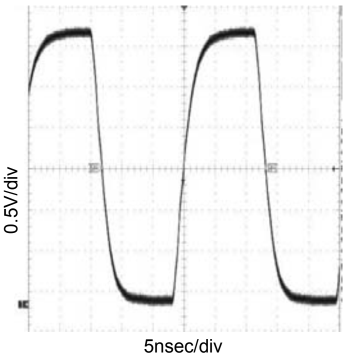


Fig.13 38MHz output waveform
(CL=15pF,Ta=25 ℃)

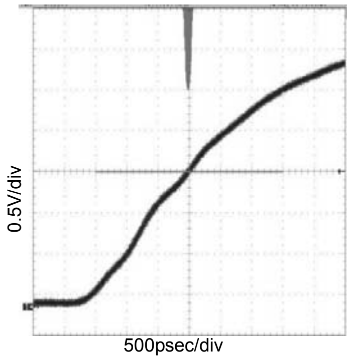


Fig.14 38MHz Period-Jitter
(CL=15pF,Ta=25 ℃)

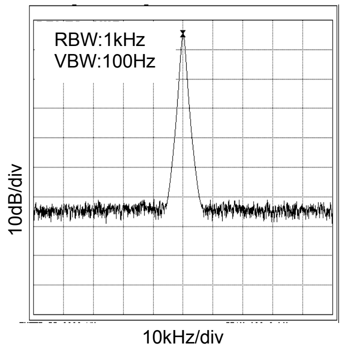


Fig.15 38MHz spectrum
(CL=15pF,Ta=25 ℃)

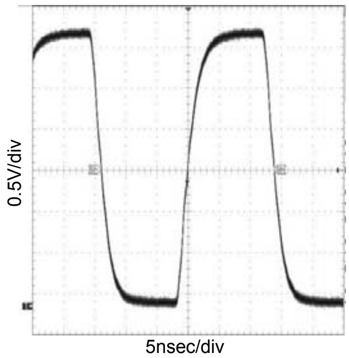


Fig.16 36MHz output waveform
(CL=15pF,Ta=25 ℃)

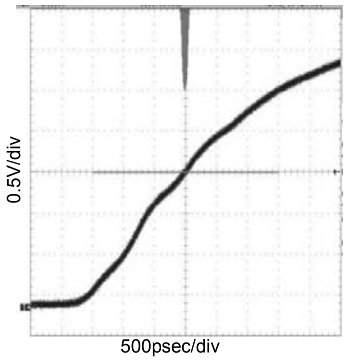


Fig.17 36MHz Period-Jitter
(CL=15pF,Ta=25 ℃)

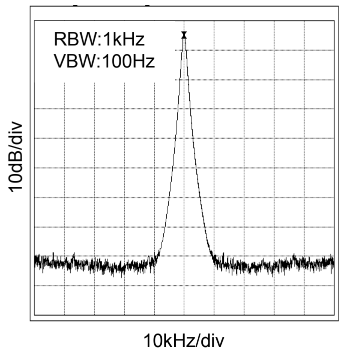


Fig.18 36MHz spectrum
(CL=15pF,Ta=25 ℃)

●**Reference data** (BU7344HFV Temperature and Supply voltage variations data)

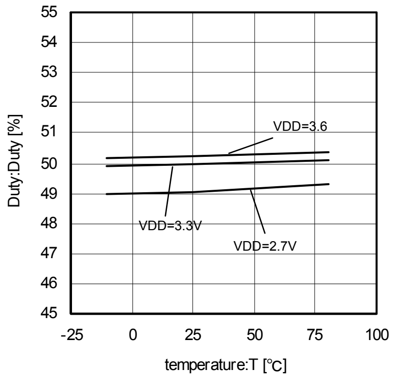


Fig.19 40.5MHz
Temperature－Duty

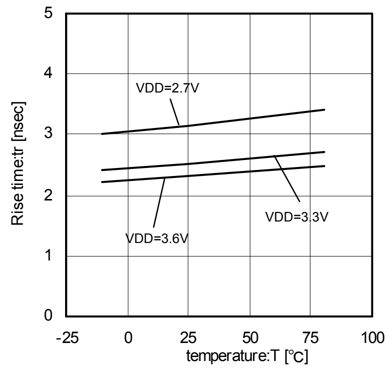


Fig.20 40.5MHz
Temperature－Rise-time

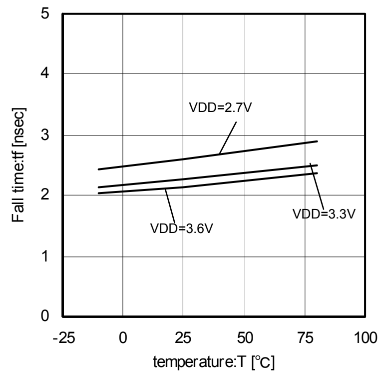


Fig.21 40.5MHz
Temperature－Fall-time

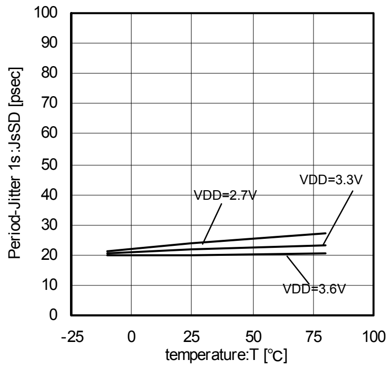


Fig.22 40.5MHz
Temperature－Period-Jitter 1σ

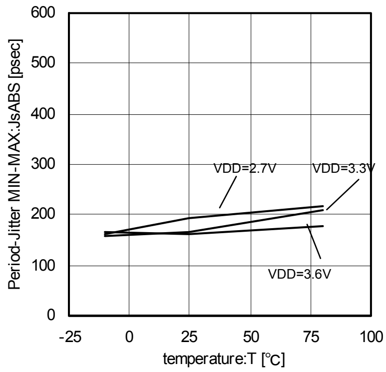


Fig.23 40.5MHz
Temperature－Period-Jitter MIN-MAX

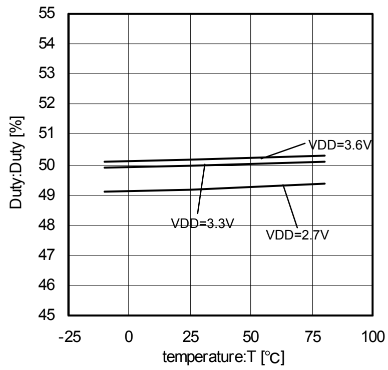


Fig.24 36MHz
Temperature－Duty

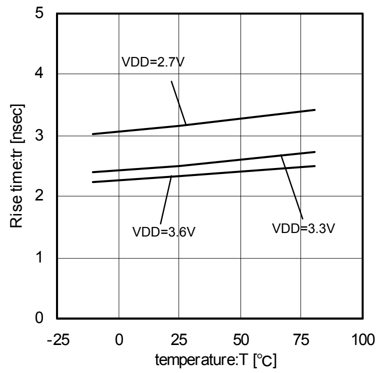


Fig.25 36MHz
Temperature－Rise-time

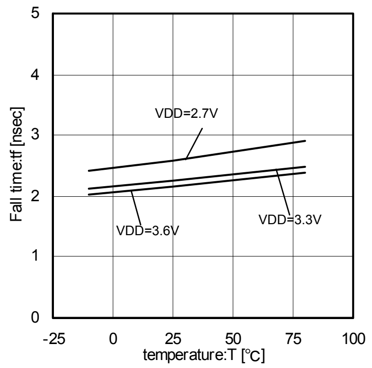


Fig.26 36MHz
Temperature－Fall-time

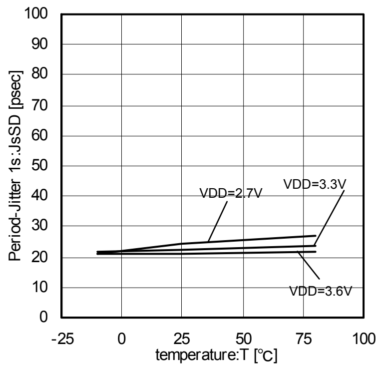


Fig.27 36MHz
Temperature－Period-Jitter 1σ

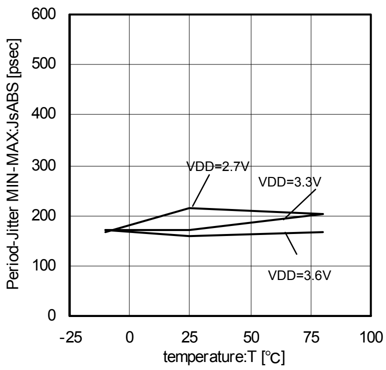


Fig.28 36MHz
Temperature－Period-Jitter MIN-MAX

●**Reference data** (BU7345HFV Temperature and Supply voltage variations data)

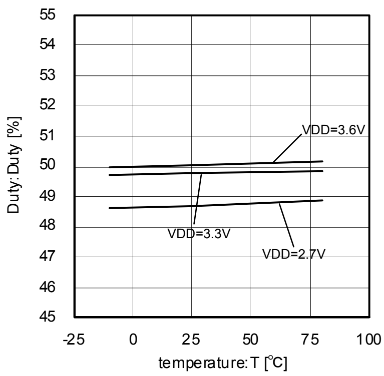


Fig.29 38MHz
Temperature－Duty

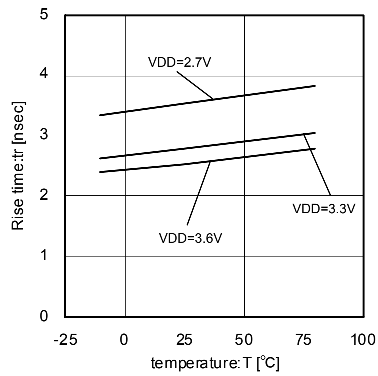


Fig.30 38MHz
Temperature－Rise-time

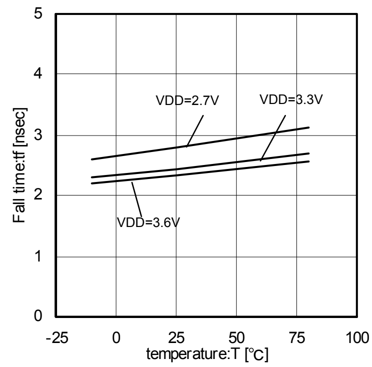


Fig.31 38MHz
Temperature－Fall-time

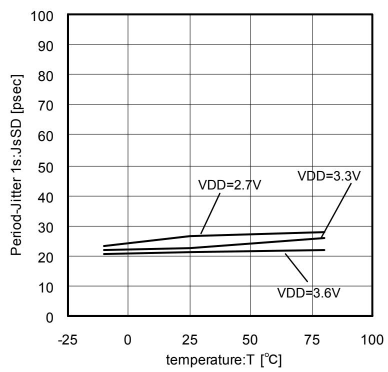


Fig.32 38MHz
Temperature－Period-Jitter 1σ

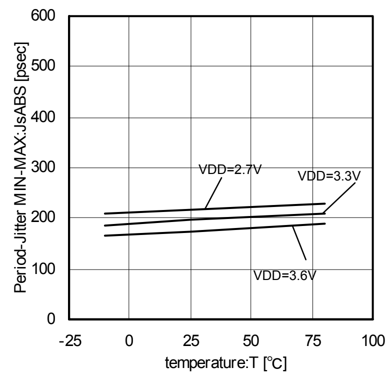


Fig.33 38MHz
Temperature－Period-Jitter MIN-MAX

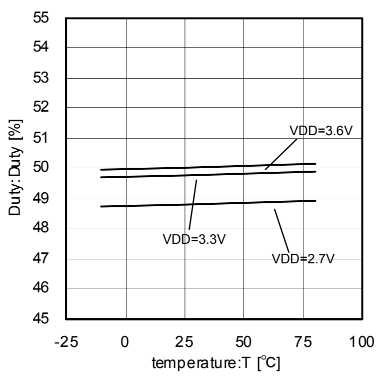


Fig.34 36MHz
Temperature－Duty

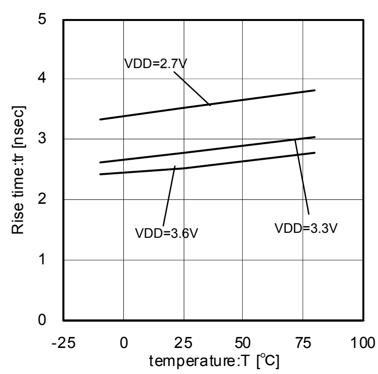


Fig.35 36MHz
Temperature－Rise-time

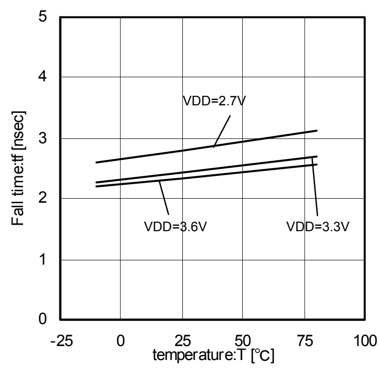


Fig.36 36MHz
Temperature－Fall-time

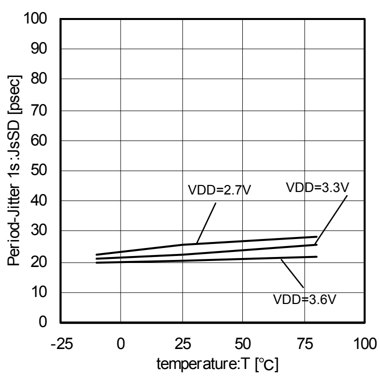


Fig.37 36MHz
Temperature－Period-Jitter 1σ

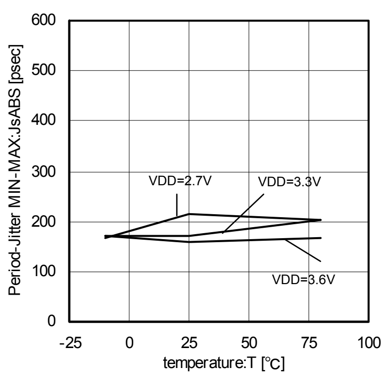


Fig.38 36MHz
Temperature－Period-Jitter MIN-MAX

●**Reference data** (BU7346GUL Temperature and Supply voltage variations data)

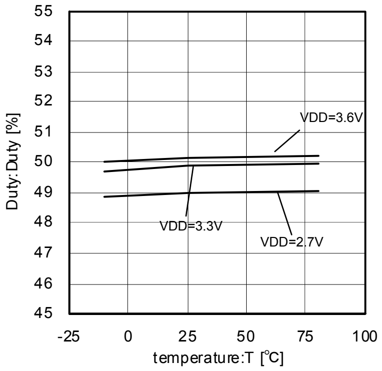


Fig.39 38MHz
Temperature－Duty

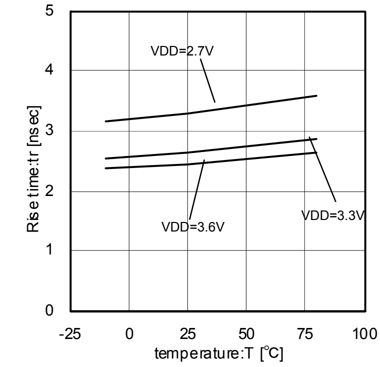


Fig.40 38MHz
Temperature－Rise-time

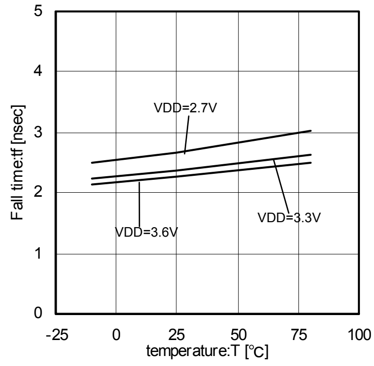


Fig.41 38MHz
Temperature－Fall-time

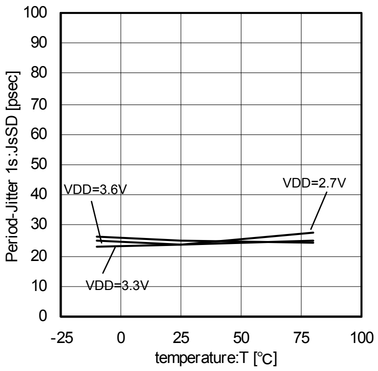


Fig.42 38MHz
Temperature－Period-Jitter 1σ

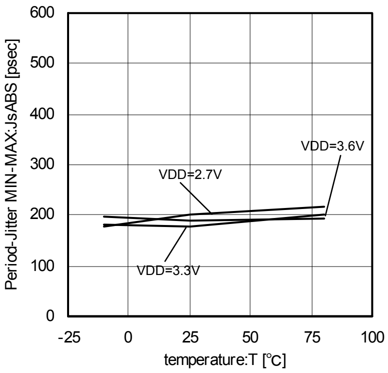


Fig.43 38MHz
Temperature－Period-Jitter MIN-MAX

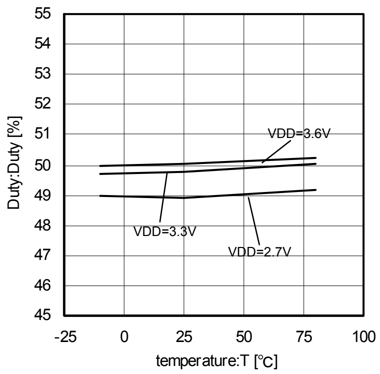


Fig.44 36MHz
Temperature－Duty

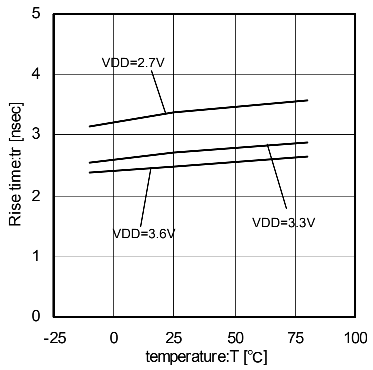


Fig.45 36MHz
Temperature－Rise-time

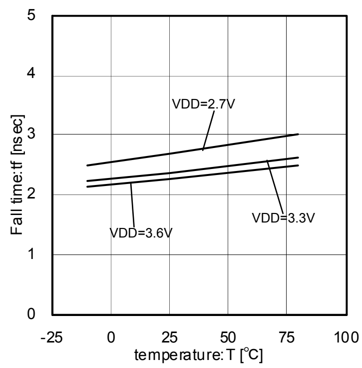


Fig.46 36MHz
Temperature－Fall-time

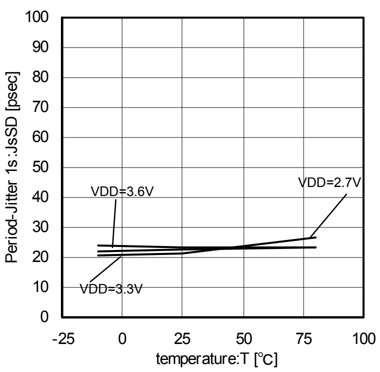


Fig.47 36MHz
Temperature－Period-Jitter 1σ

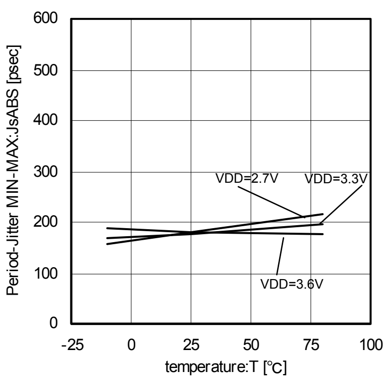


Fig.48 36MHz
Temperature－Period-Jitter MIN-MAX

● Block diagram, pin assignment/functions

○BU7344HFV

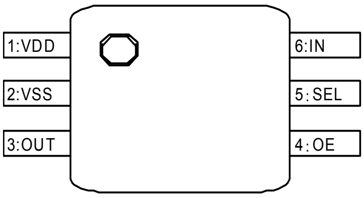


Fig.49 Pin assignment

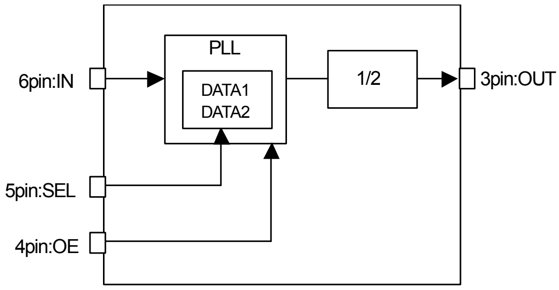


Fig.50 Block diagram

PIN No.	PIN Name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (SEL=L:40.5000MHz, SEL=H:36.0000MHz)
4	OE	Power-down pin (L:disable, H:enable), equipped with Pull-down function, output set to L at disable
5	SEL	Output selection (L:40.5000MHz, H:36.0000MHz)
6	IN	Clock input pin (27.0000MHz input)

○BU7345HFV

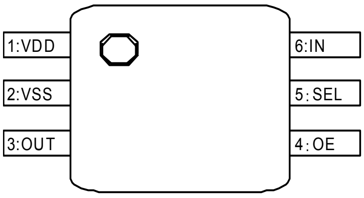


Fig.51 Pin assignment

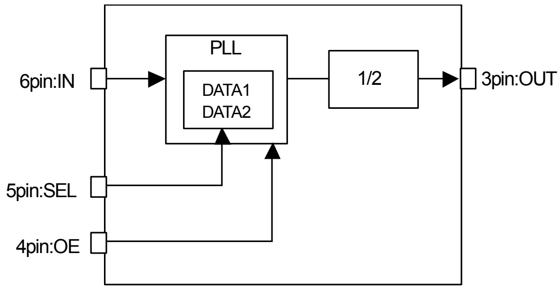


Fig.52 Block diagram

PIN No.	PIN Name	Function
1	VDD	Power supply
2	VSS	GND
3	OUT	Clock output terminal (SEL=L:38.0000MHz, SEL=H:36.0000MHz)
4	OE	Power-down pin (L:disable, H:enable), equipped with Pull-down function, output set to L at disable
5	SEL	Output selection (L:38.0000MHz, H:36.0000MHz)
6	IN	Clock input pin (27.0000MHz input)

○BU7346GUL

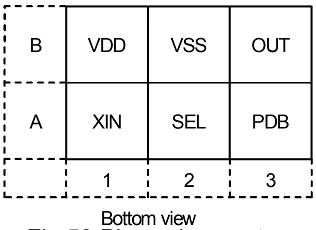


Fig.53 Pin assignment

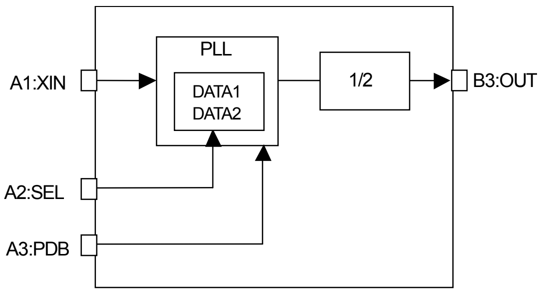


Fig.54 Block diagram

PIN No.	PIN Name	Function
A1	XIN	Clock input pin (27.0000MHz input)
A2	SEL	Output selection (L:38.0000MHz, H:36.0000MHz)
A3	PDB	Power-down pin (L:disable, H:enable), equipped with Pull-down function, output set to L at disable
B1	VDD	Power supply
B2	VSS	GND
B3	OUT	Clock output terminal (SEL=L:38.0000MHz, SEL=H:36.0000MHz)

●Application circuit example

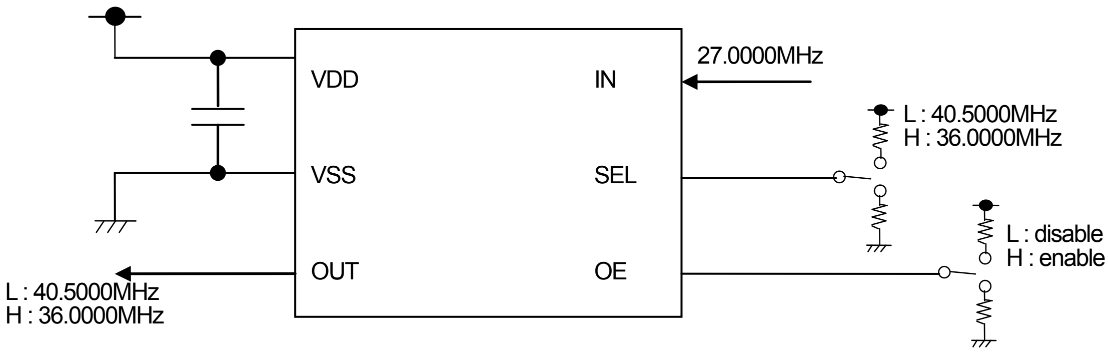
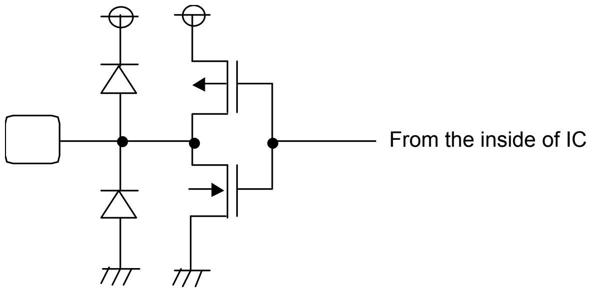
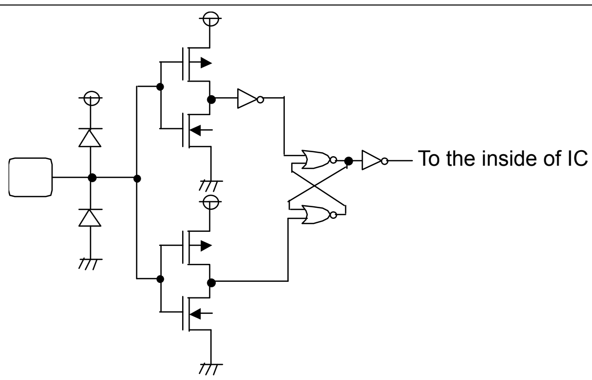
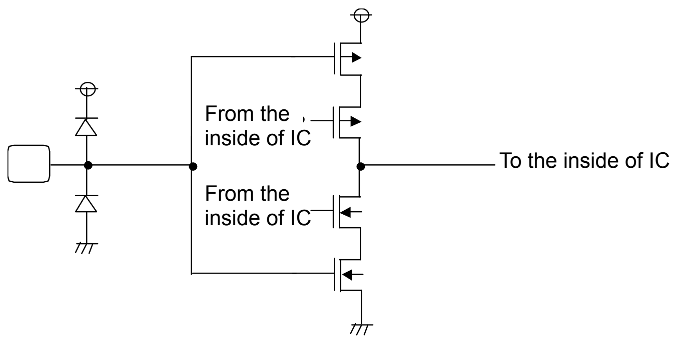


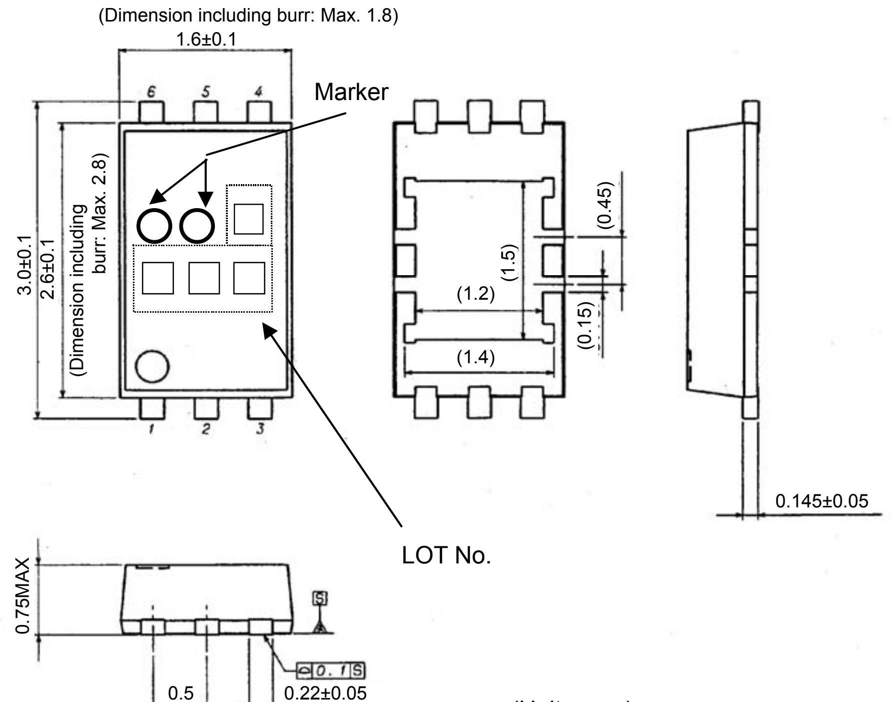
Fig.55 Application circuit example(BU7344HFV)

* For VDD and VSS, insert a bypass capacitor of approx. 0.1μF as close as possible to the pin.Bypass capacitors with good high-frequency characteristics are recommended. Even though we believe that the typical application circuit is worth of a recommendation, please be sure to thoroughly recheck the characteristics before use.

●Equivalent circuit

Pin name	Pin number	Equivalent circuit
OUT	3, B3	
OE(PDB) SEL	4, A2 5, A3	
IN(XIN)	6, A1	

●Appearance of Marker

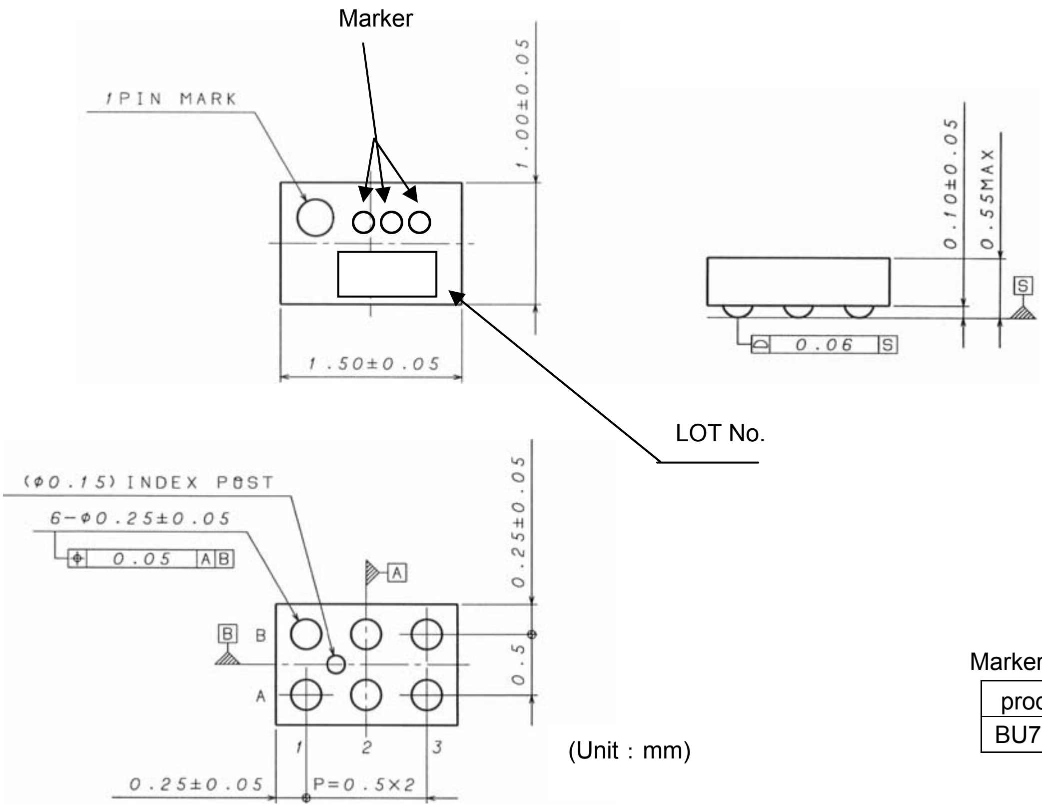


(Unit : mm)

Fig.56 HVSOF6 Appearance of Marker

Marker lists

product name	marker
BU7344HFV	AN
BU7345HFV	AP



(Unit : mm)

Marker lists

product name	marker
BU7346GUL	AA8

Fig.57 VCSP50L1 Appearance of Marker

●Notes for use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as applied voltage (VDD or VIN), operating temperature range (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

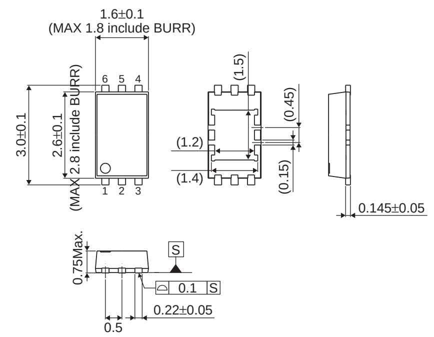
(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Ordering part number

B	D		7	3	4	4		H	F	V	-	T	R

- **Part No** (BD)
- **Part No**: 7344, 7345, 7346
- **Package**: HFV: HVSOF6; GUL: VCSP50L1
- **Packaging and forming specification**: TR: Embossed tape and reel (HVSOF6); E2: Embossed tape and reel (VCSP50L1)

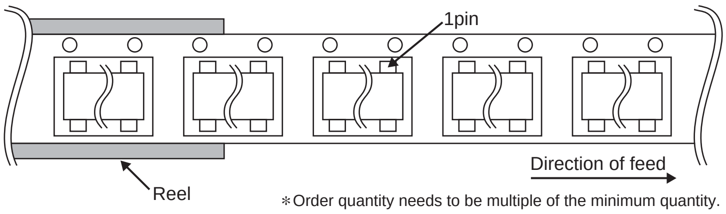
HVSOF6



(Unit : mm)

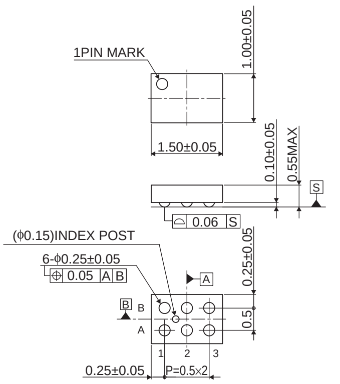
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



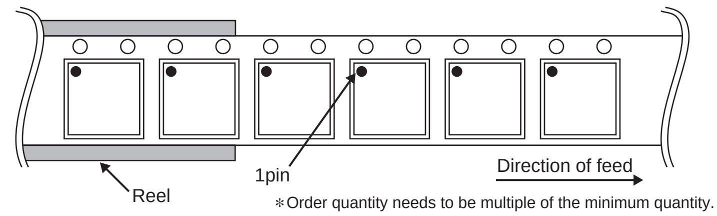
∗Order quantity needs to be multiple of the minimum quantity.

VCSP50L1(BU7346GUL)



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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