Saratoga Semiconductor

SSM6116

16K 2,048 Words by 8 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  15/20/25ns Commercial Temperature
  20/25/35ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883B Compliant**
- **Industry Standard Packages**
  24-Pin DIP
  24-Pin SOJ
  24-Pin SOG
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

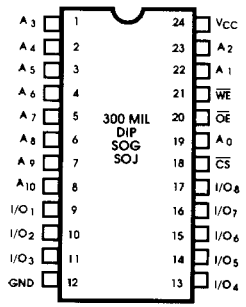
The SSM6116 is a high performance 16K BiCMOS static RAM organized 2048 words by 8 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (15ns), low active power consumption (120mA) and high output drive (16mA) of the SSM6116 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low. Data on the Input/Output pins (I/O_1 - I/O_8) is written into the memory cell specified by the 11 bit address placed on the Address Inputs (A_0- A_{10}). With $\overline{CS}$ low, $\overline{WE}$ high and the Output Enable input LOW, the content of the addressed memory cell is transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

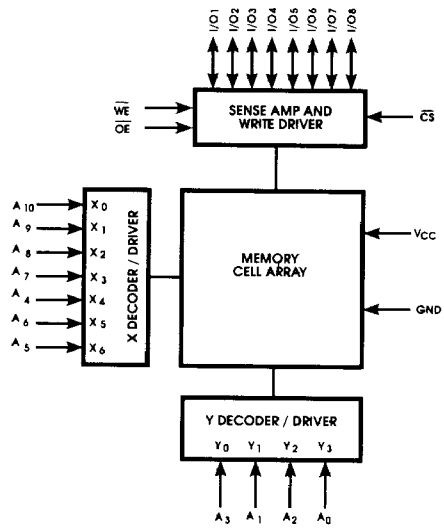
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{10}	Address Inputs
I/O_1 - I/O_8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply Pin
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



April 1989

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/On	POWER
Read	L	H	L	DO	ACTIVE
Write '0'	L	L	X	L	ACTIVE
Write '1'	L	L	X	H	ACTIVE
Output Disabled	L	H	H	HIGH Z	ACTIVE
Disabled	H	X	X	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM6118 MIN	SSM6118 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=16mA ; V_{CC}= min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		120	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

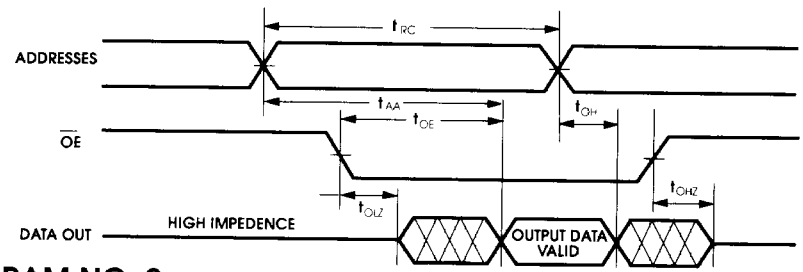
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM6116-15*	COM/MIL SSM6116-20	COM/MIL SSM6116-25	MIL SSM6116-35	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
Read Cycle Time	t_{RC}	15	20	25	35	ns
Address Access Time	t_{AA}	15	20	25	35	ns
Chip Select Access Time	t_{ACS}	12	15	20	25	ns
Output Hold from Address Change	t_{OH}	3	3	3	3	ns
Chip Selection to Output in LOW Z	t_{LZ} [5]	3	3	3	3	ns
Chip Selection to Output in HIGH Z	t_{HZ} [5]	8	15	20	25	ns
Output Enable to Output Valid	t_{OE}	12	15	18	20	ns
Output Enable to Output in LOW Z	t_{OLZ}	0	0	0	0	ns
Output Disable to Output in HIGH Z	t_{OHZ}	8	12	15	20	ns

[2] These parameters are sampled and not 100% tested. * Advance Information.
[5] These parameters are guaranteed and not tested.

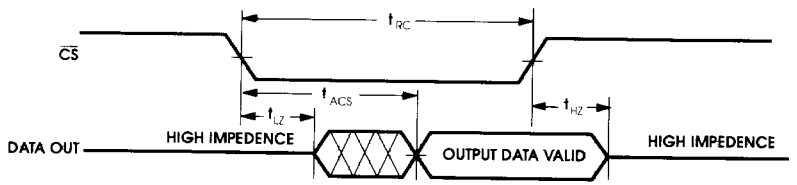
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}. Transition is measured ±500mV from steady state.



READ CYCLE TIMING DIAGRAM NO. 2

$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.

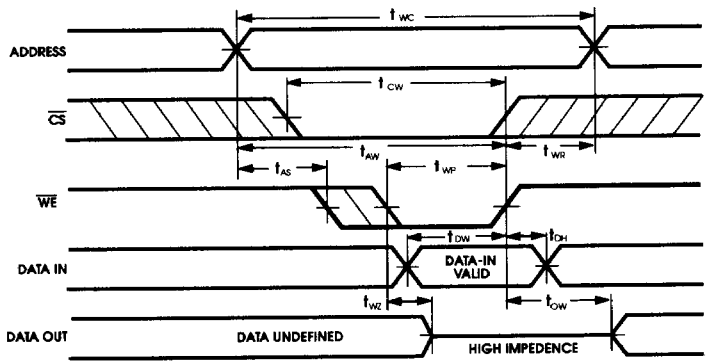


WRITE CYCLE

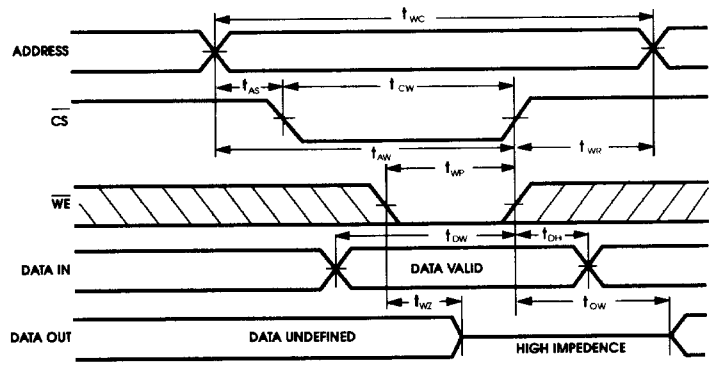
		VALUE				
		COM SSM6116-15*	COM/MIL SSM6116-20	COM/MIL SSM6116-25	MIL SSM6116-35	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	15	20	25	35	ns
Chip Selection to End of Write	t_{CW}	15	20	25	35	ns
Address Valid to End of Write	t_{AW}	15	20	25	35	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	15	20	25	35	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	9	12	15	20	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	8	10	15	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

* Advance Information.

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	MAX VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

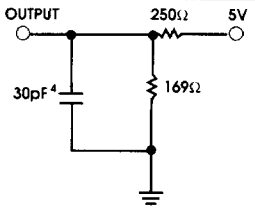


Figure 1

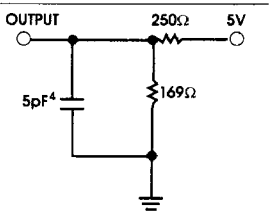
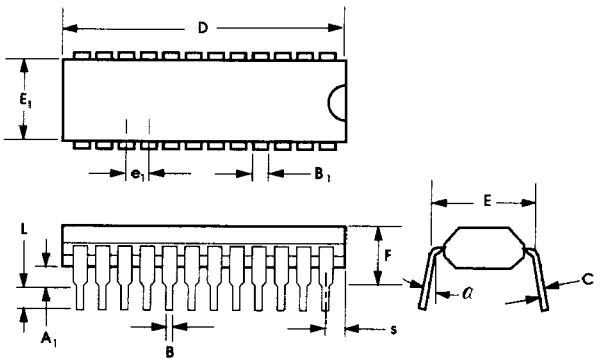


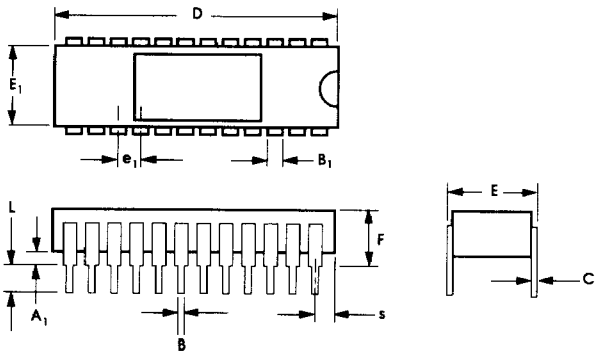
Figure 2

PACKAGE DIMENSIONS



24 LEAD 300 MIL PDIP

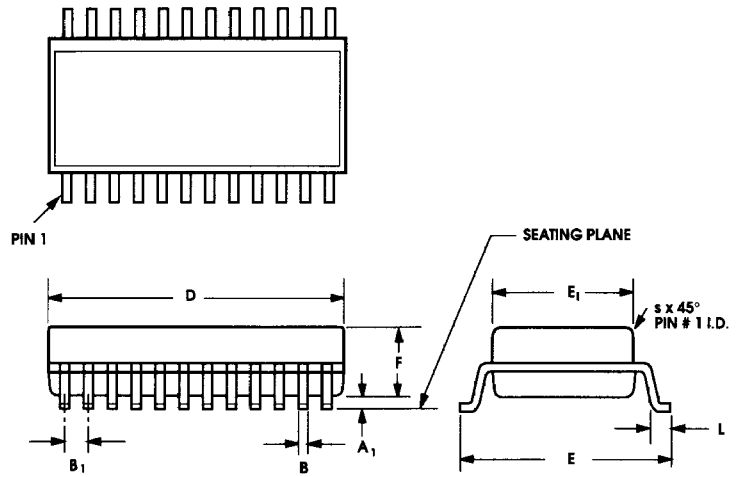
	INCHES	
PARAMETER	MIN	MAX
A_1	.010	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	1.245	1.255
E	.300	.325
E_1	.250	.270
e_1	.100	
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



24 LEAD 300 MIL SIDEBRAZE DIP

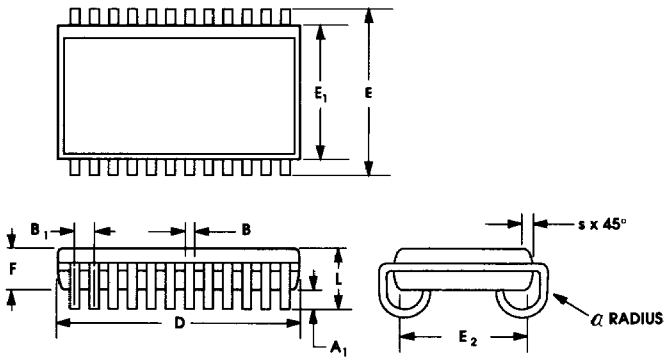
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.185	1.215
E	.290	.310
E_1	.285	.305
e_1	.100	
F		.232
L	.125	.200
s		.100

PACKAGE DIMENSIONS (CONTINUED)



24 LEAD MOLDED SOG

PARAMETER	INCHES MIN	INCHES MAX
A_1	.006	.010
B	.014	.019
B_1	.050	
D	.602	.612
E	.400	.416
E_1	.292	.299
F	.090	.094
L	.030	.040
s	.010	.020



24 LEAD MOLDED SOJ

PARAMETER	INCHES MIN	INCHES MAX
A_1	.028	.036
B	.014	.019
B_1	.050	
D	.602	.612
E	.335	.347
E_1	.292	.299
E_2	.262	.272
F	.090	.094
L	.120	.140
s	.010	.016
α	.031	.042

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM6116-15PC SSM6116-20PC SSM6116-25PC	15ns 20ns 25ns	24-Pin PDIP	0	+70	°C
SSM6116-15DC SSM6116-20DC SSM6116-25DC	15ns 20ns 25ns	24-Pin Plastic SOG			
SSM6116-15EC SSM6116-20EC SSM6116-25EC	15ns 20ns 25ns	24-Pin Plastic SOJ			
SSM6116-15SC SSM6116-20SC SSM6116-25SC	15ns 20ns 25ns	24-Pin Sidebraze DIP			
SSM6116-20SB SSM6116-25SB SSM6116-35SB	20ns 25ns 35ns	24-Pin Sidebraze DIP	-55	+125	°C

NOTE: Please contact factory regarding CERDIP, FLATPACK and PLCC packages.