

✓ 54S/74S289 611743
 ✓ 54LS/74LS289 011748

64-BIT RANDOM ACCESS MEMORY
 (With Open-Collector Outputs)

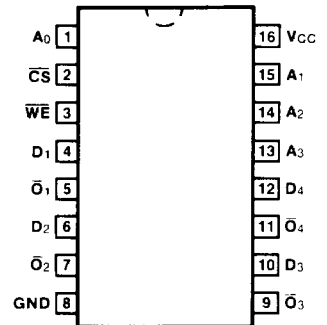
DESCRIPTION — The '289 is a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select (CS) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

- OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS
- BUFFERED INPUTS MINIMIZE LOADING
- ADDRESS DECODING ON-CHIP
- DIODE CLAMPED INPUTS MINIMIZE RINGING

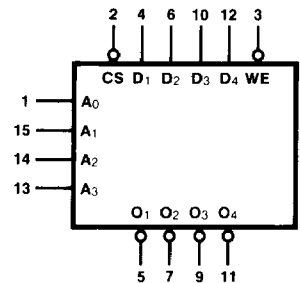
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74S289PC, 74LS289PC		9B
Ceramic DIP (D)	A	74S289DC, 74LS289DC	54S289DM, 54LS289DM	6B
Flatpak (F)	A	74S289FC, 74LS289FC	54S289FM, 54LS289FM	4L

CONNECTION DIAGRAM
 PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
 GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A ₀ — A ₃	Address Inputs	0.63/0.16	0.5/0.013
CS	Chip Select Input (Active LOW)	0.63/0.16	0.5/0.013
WE	Write Enable Input (Active LOW)	0.63/0.16	0.5/0.013
D ₁ — D ₄	Data Inputs	0.63/0.16	0.5/0.013
O ₁ — O ₄	Inverted Data Outputs	OC*/10	OC*/10 (5.0)

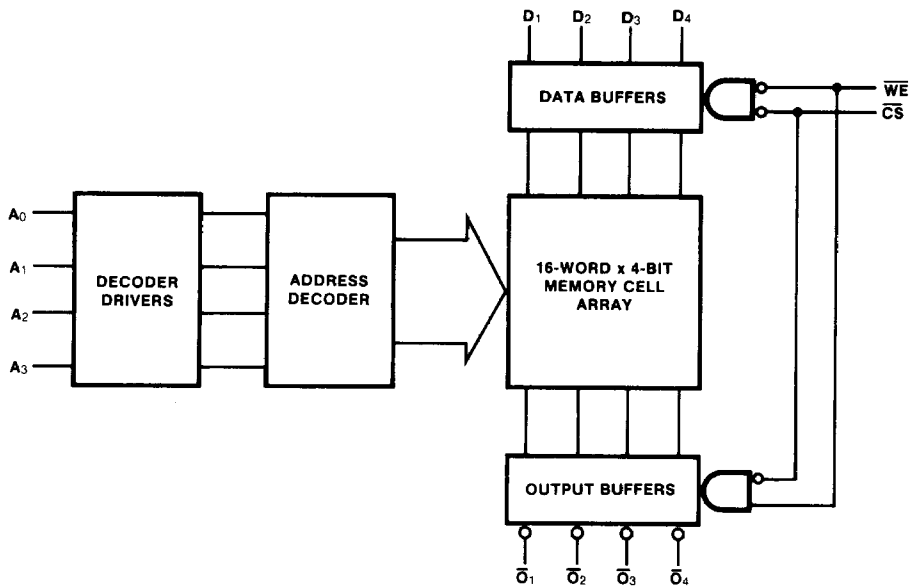
*OC — Open Collector

FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
CS	\overline{WE}		
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
VOL	Output LOW Voltage	XM	0.5	0.4	V	V _{CC} = Min I _{OL} = 16 mA ('S289) I _{OL} = 8.0 mA (54LS289) I _{OL} = 16 mA (74LS289)	
		XC	0.45	0.5			
I _{OH}	Output HIGH Current	40	20	100	μA	V _{OH} = 2.4 V V _{OH} = 5.5 V	
I _{CC}	Power Supply Current	105	40		mA	V _{CC} = Max	

AC CHARACTERISTICS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C _L = 30 pF R _L = *		C _L = 15 pF R _L = 2 kΩ			
		Min	Max	Min	Max		
t _{PLH} t _{PHL}	Access Time, HIGH or LOW, A _n to \overline{O}_n	XM	50	37**	ns	Figs. 3-2, 3-20	
		XC	35	37**			
t _{PHL}	Access Time \overline{CS} to \overline{O}_n	XM	25	10**	ns	Figs. 3-2, 3-5	
		XC	17	10**			
t _{PLH}	Disable Time \overline{CS} to \overline{O}_n	XM	20		ns		
		XC	17				
t _{PHL}	Recovery Time WE to \overline{O}_n	XM	40	30**	ns	Figs. 3-2, 3-4	
		XC	35	30**			
t _{PLH}	Disable Time WE to \overline{O}_n	XM	30		ns		
		XC	25				

AC OPERATING REQUIREMENTS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time, HIGH or LOW A _n to \overline{WE}	0		10**		ns	Fig. 3-21
t _h (H) t _h (L)	Hold Time, HIGH or LOW A _n to \overline{WE}	0		0**			
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to \overline{WE}	20		25**		ns	Fig. 3-13
t _h (H) t _h (L)	Hold Time HIGH or LOW D _n to \overline{WE}	0		0*			
t _s (L)	Setup Time LOW \overline{CS} to \overline{WE}	0				ns	Fig. 3-14
t _h (L)	Hold Time LOW \overline{CS} to \overline{WE}	0				ns	Fig. 3-13
t _w (L)	\overline{WE} Pulse Width LOW	20		25**		ns	Fig. 3-14

*R_L = 300 Ω to V_{CC} and 600 Ω to Gnd.

**Typical Value