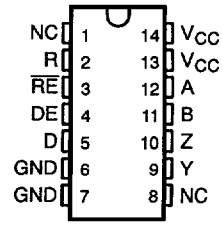
SLLS052C – D3043, AUGUST 1987 – REVISED FEBRUARY 1992

- **Meets EIA Standards RS-422A and RS-485† and CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation in Both Serial and Parallel Applications**
- **Low Skew Between Devices . . . 6 ns Max**
- **Low Supply Current Requirements 30 mA Max**
- **Individual Driver and Receiver I/O Pins With Dual V_{CC} and Dual GND**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

DRIVER

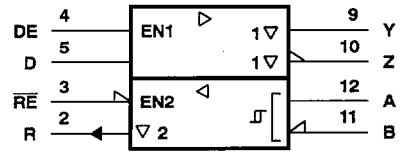
INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

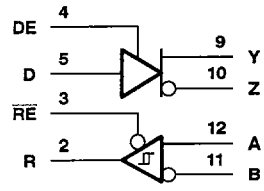
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

The SN65ALS180 and SN75ALS180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver

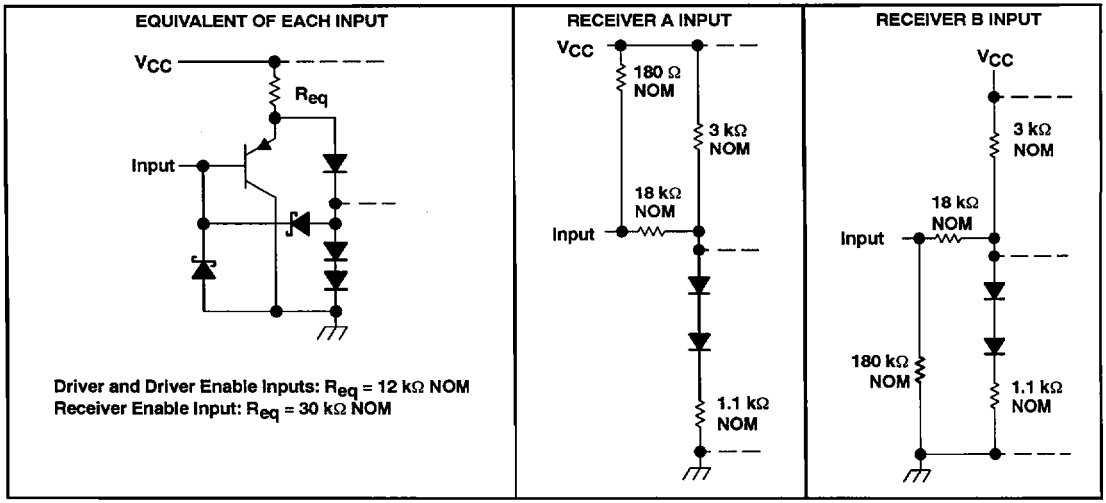
† These devices meet or exceed the requirements of EIA RS485 except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are –6 V to 8 V for the SN75ALS180 and –4.5 V to 8 V for the SN65ALS180.

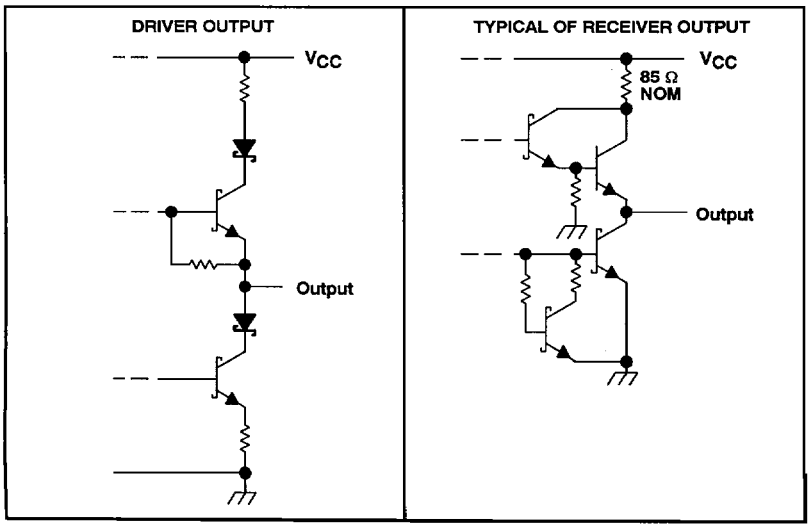
description (continued)

differential inputs are connected to separate pins for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS180 is characterized for operation from −40°C to 85°C. The SN75ALS180 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs





TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS180 ..... −40°C to 85°C
SN75ALS180 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12 −7	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS180	−40		85	°C
	SN75ALS180	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A/Y with respect to the inverting terminal B/Z.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	1/2V_{OD1} or 2§			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	$R_L = 54\ \Omega$ or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 3	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	µA
I_{OS}	Short-circuit output current#	$V_O = -6$ V	SN75ALS180			−250	mA
		$V_O = -4$ V	SN65ALS180				
		$V_O = 0$	All			−150	
		$V_O = V_{CC}$	All				
		$V_O = 8$ V	All				
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
§ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
¶ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
# Duration of the short circuit does not exceed one second for this test.
NOTE 3: This applies for both power on and off; refer to EIA standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{dD}	Differential output delay time	$R_L = 54\ \Omega$, $C_L = 50$ pF, See Figure 3	3	8	13	ns
	Pulse skew ($\lvert t_{dDH} - t_{dDL} \rvert$)			1	6	ns
t_{tD}	Differential output transition time		3	8	13	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$, See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$, See Figure 5		19	24	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$, See Figure 4		8	13	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$, See Figure 5		8	13	ns

‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 7	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output		9	14	19	ns
	Skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level			7	14	ns
t_{PHZ}	Output disable time from high level			20	35	ns
t_{PLZ}	Output disable time from low level			8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

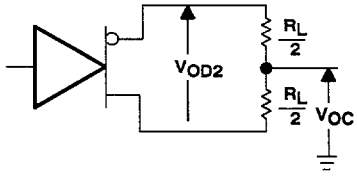


Figure 1. Driver V_{OD} and V_{OC}

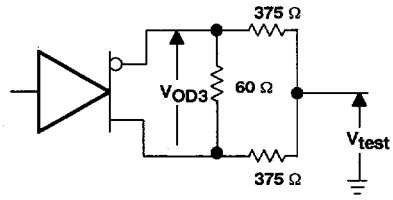
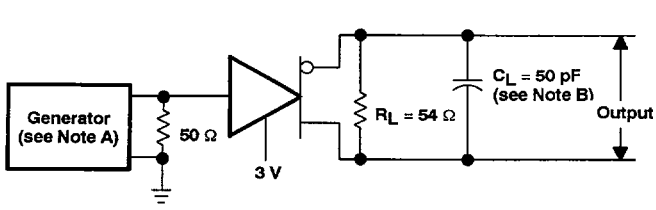
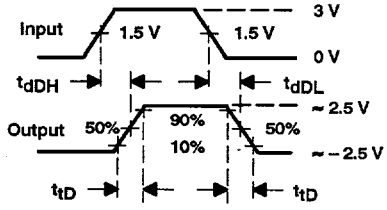


Figure 2. Driver V_{OD3}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

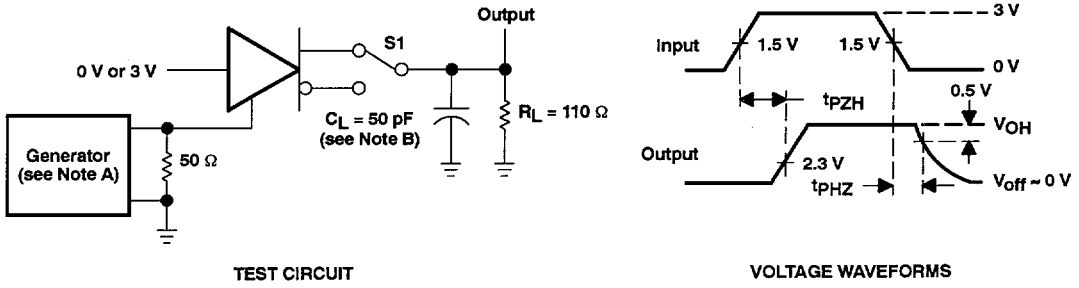


Figure 4. Driver Test Circuit and Voltage Waveforms

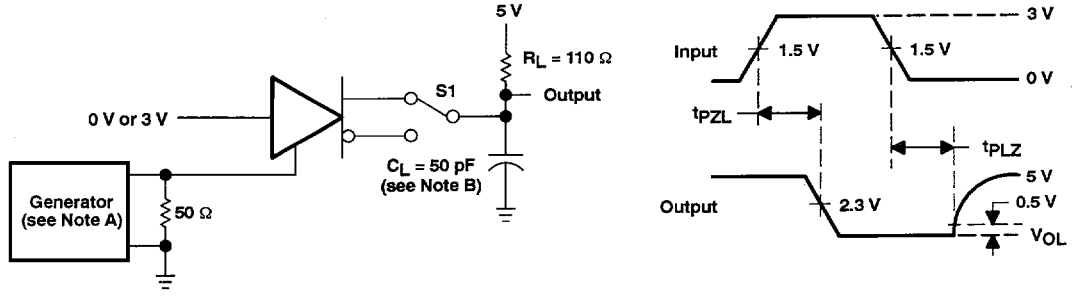


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

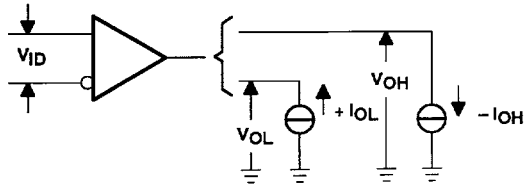


Figure 6. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

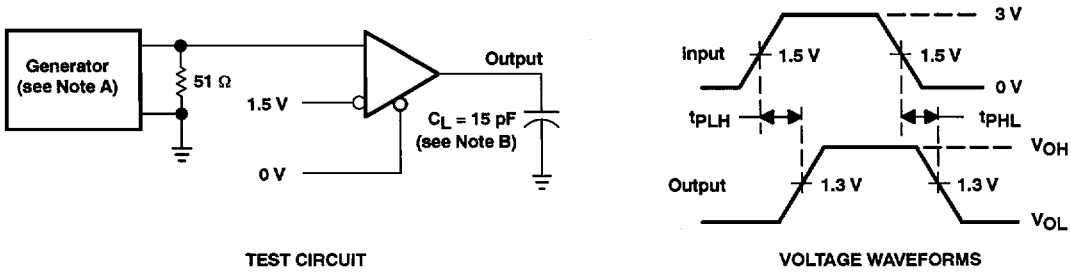


Figure 7. Receiver Test Circuit and Voltage Waveforms

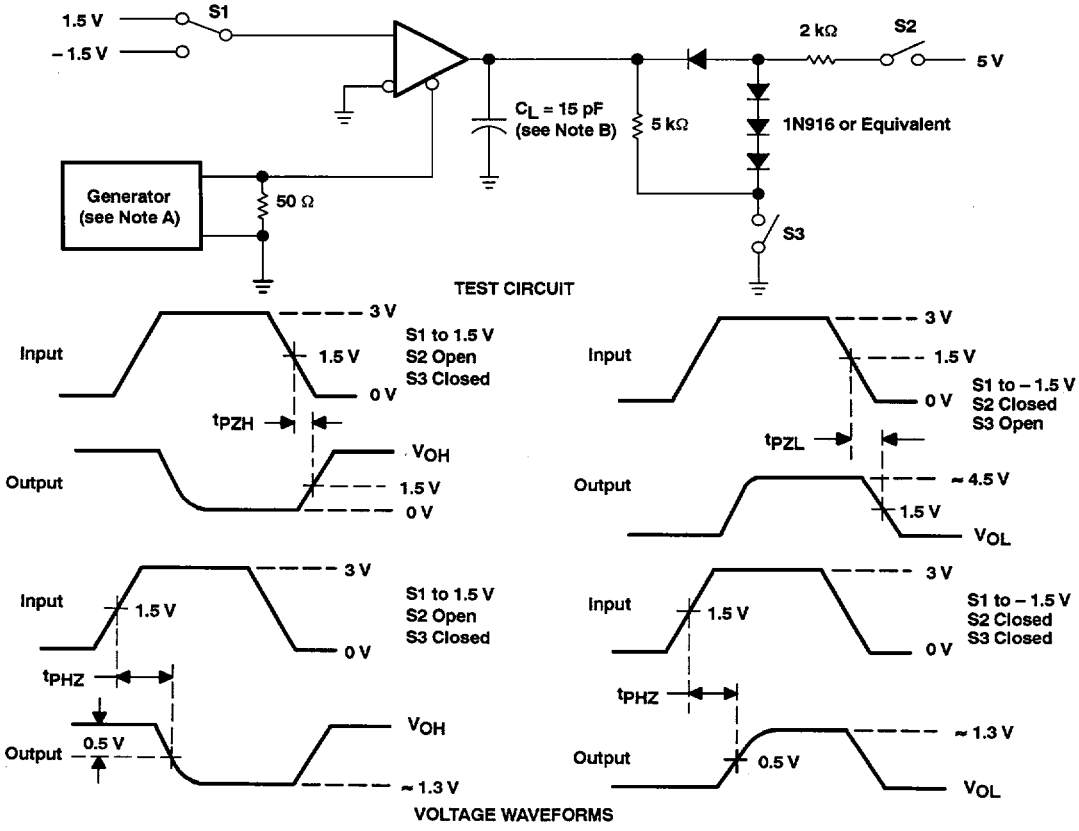


Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

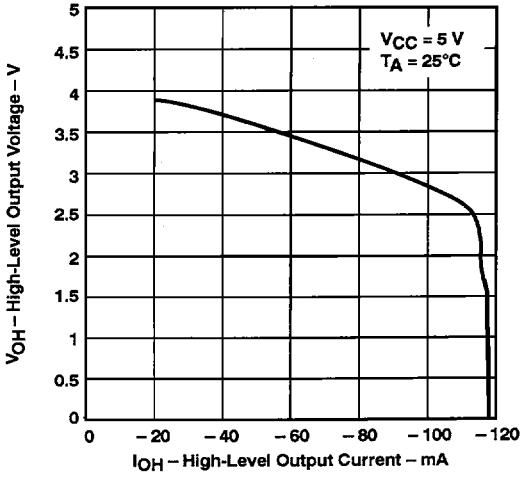


Figure 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

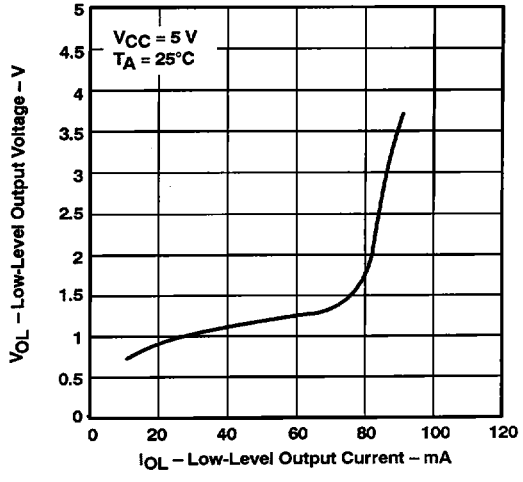


Figure 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

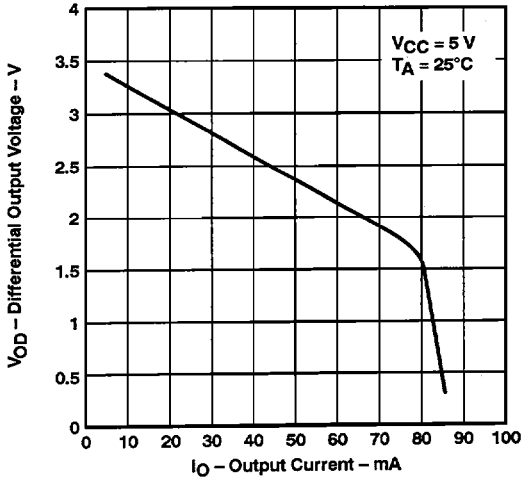


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

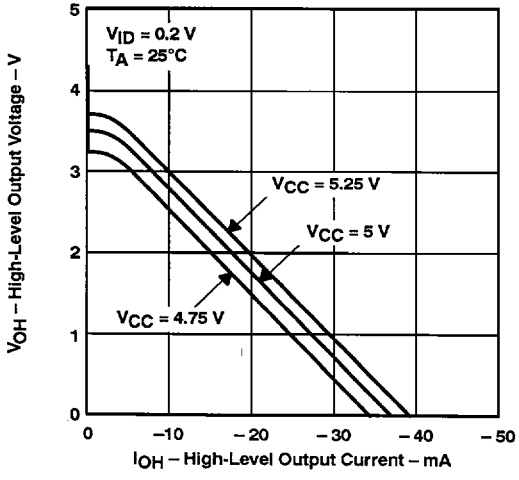


Figure 12

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

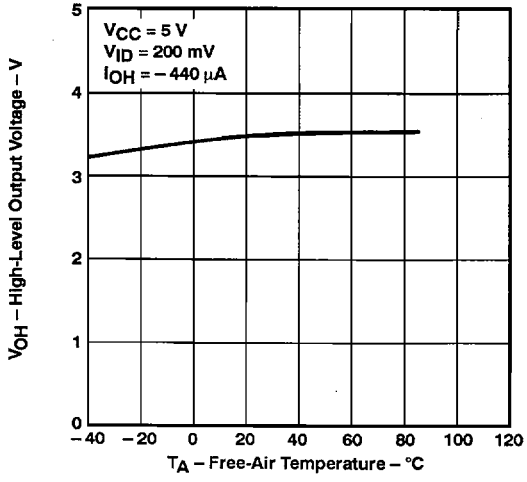


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

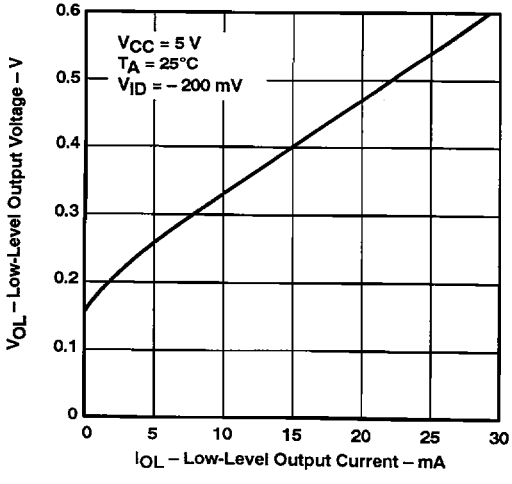


Figure 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

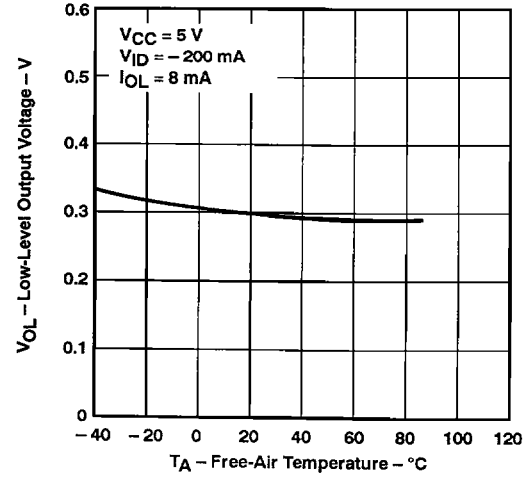


Figure 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

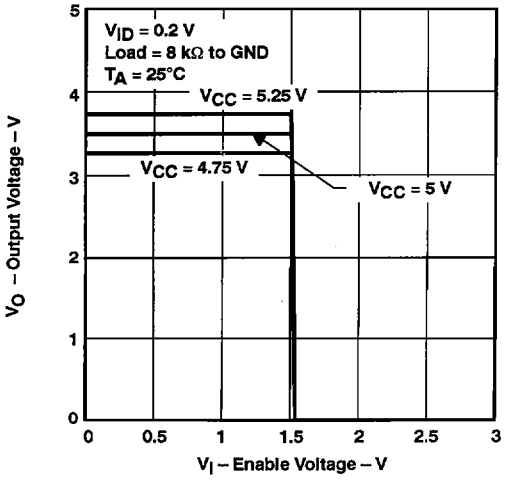


Figure 16

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

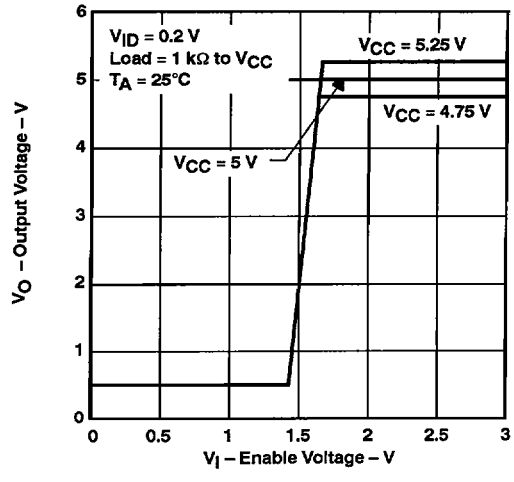
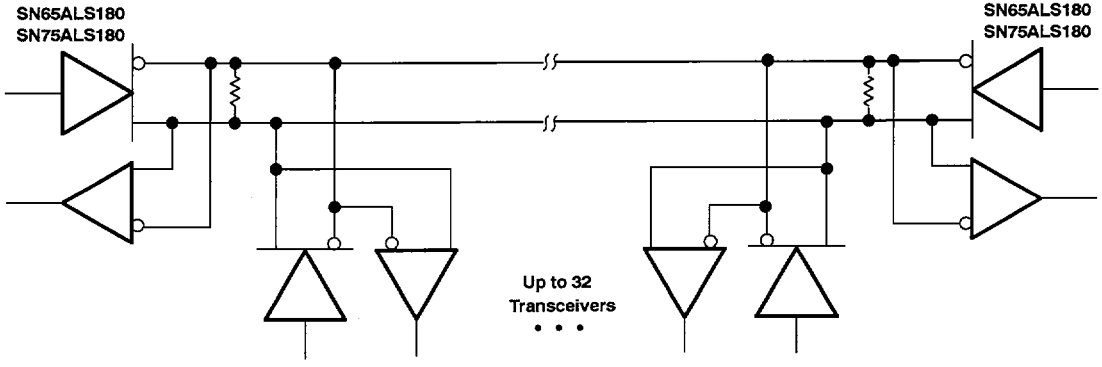


Figure 17

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit