

# LMX2330U/LMX2331U/LMX2332U PLLatinum™ Ultra Low Power Dual Frequency Synthesizer for RF Personal Communications

**LMX2330U** 2.5 GHz/600 MHz

**LMX2331U** 2.0 GHz/600 MHz

**LMX2332U** 1.2 GHz/600 MHz

## General Description

The LMX233xU family of monolithic, integrated dual frequency synthesizers, including prescalers, is to be used as a local oscillator for RF and first IF of a dual conversion transceiver.

The LMX233xU contains dual modulus prescalers. A 64/65 or a 128/129 prescaler (32/33 or 64/65 in the 2.5 GHz LMX2330U) can be selected for the RF synthesizer and a 8/9 or a 16/17 prescaler can be selected for the IF synthesizer. LMX233xU, which employs a digital phase locked loop technique, combined with a high quality reference oscillator, provides the tuning voltages for voltage controlled oscillators to generate very stable, low noise signals for RF and IF local oscillators. Serial data is transferred into the LMX233xU via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX233xU family features very low current consumption;

LMX2330U—3.3 mA at 3V, LMX2331U—2.9 mA at 3V, LMX2332U—2.5 mA at 3V.

The LMX233xU are available in TSSOP 20-pin and CSP 24-pin surface mount plastic packages.

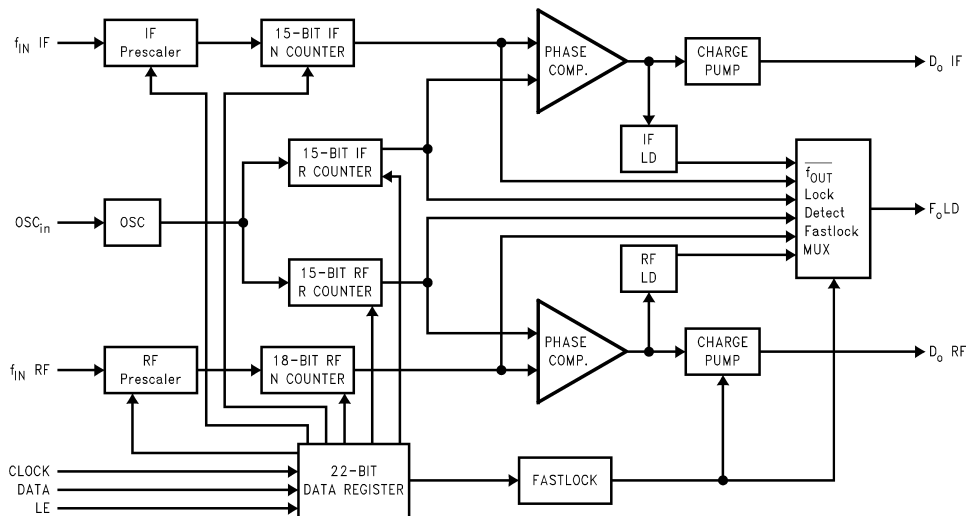
## Features

- Ultra low current consumption
- 2.7V to 5.5V operation
- Selectable synchronous or asynchronous powerdown mode:
  - $I_{CC} = 1 \mu\text{A}$  typical at 3V
- Dual modulus prescaler:
  - LMX2330U (RF) 32/33 or 64/65
  - LMX2331U/32U (RF) 64/65 or 128/129
  - LMX2330U/31U/32U (IF) 8/9 or 16/17
- Selectable charge pump TRI-STATE® mode
- Selectable charge pump current levels
- Selectable Fastlock™ mode
- Upgrade and compatible to LMX233xL family
- Available in 20 - Lead TSSOP and 24 - Pin CSP

## Applications

- Portable Wireless Communications (PCS/PCN, cordless)
- Cordless and cellular telephone systems
- Wireless Local Area Networks (WLANs)
- Cable TV tuners (CATV)
- Other wireless communication systems

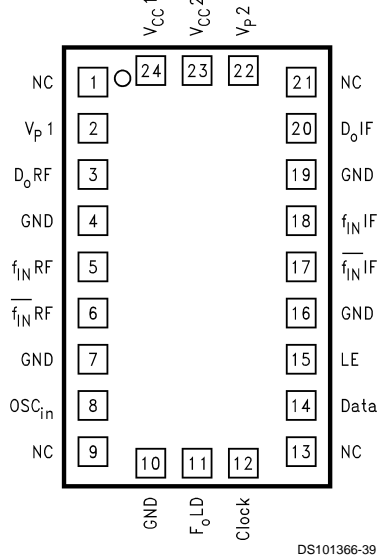
## Functional Block Diagram



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Fastlock™, MICROWIRE™ and PLLatinum™ are trademarks of National Semiconductor Corporation.

## Connection Diagrams

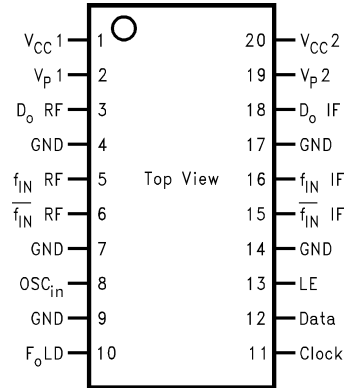
**Chip Scale Package (SLB)  
(Top View)**



DS101366-39

**Order Number LMX2330USLB, LMX2331USLB or  
LMX2332USLB  
NS Package Number SLB24A**

**Thin Shrink Small Outline Package (TM)  
(Top View)**



DS101366-2

**Order Number LMX2330UTM, LMX2331UTM or  
LMX2332UTM  
NS Package Number MTC20**

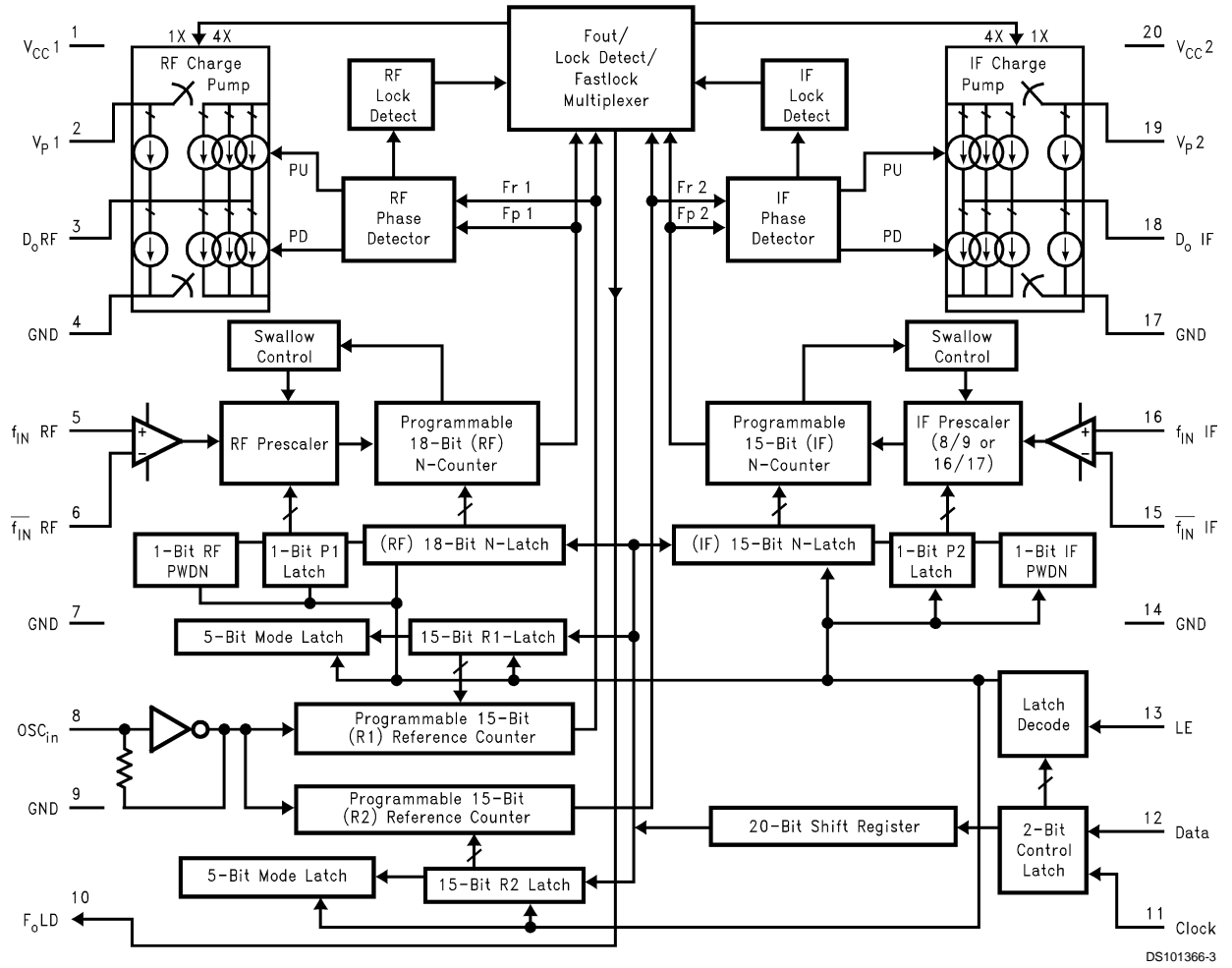
## Pin Descriptions

Pin No. LMX233xUSLB 24-pinCSP Package	Pin No. LMX233xUTM 20-pin TSSOP Package	Pin Name	I/O	Description
24	1	V <sub>CC1</sub>	—	Power supply voltage input for RF analog and RF digital circuits. Input may range from 2.7V to 5.5V. V <sub>CC1</sub> must equal V <sub>CC2</sub> . Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	2	V <sub>P1</sub>	—	Power Supply for RF charge pump. Must be ≥ V <sub>CC</sub> .
3	3	D <sub>O</sub> RF	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
4	4	GND	—	Ground for RF digital circuitry.
5	5	f <sub>IN</sub> RF	I	RF prescaler input. Small signal input from the VCO.
6	6	f <sub>IN</sub> RF	I	RF prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
7	7	GND	—	Ground for RF analog circuitry.
8	8	OSC <sub>in</sub>	I	Oscillator input. The input has a V <sub>CC</sub> /2 input threshold and can be driven from an external CMOS or TTL logic gate.
10	9	GND	—	Ground for IF digital, MICROWIRE™, F <sub>o</sub> LD, and oscillator circuits.
11	10	F <sub>o</sub> LD	O	Multiplexed output of the RF/IF programmable or reference dividers, RF/IF lock detect signals and Fastlock mode. CMOS output ( <i>see Programmable Modes</i> ).
12	11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.
14	12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.

## Pin Descriptions (Continued)

Pin No. LMX233xULSLB 24-pinCSP Package	Pin No. LMX233xUTM 20-pin TSSOP Package	Pin Name	I/O	Description
15	13	LE	I	Load enable high impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).
16	14	GND	—	Ground for IF analog circuitry.
17	15	$\overline{f_{IN}}$ IF	I	IF prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
18	16	$f_{IN}$ IF	I	IF prescaler input. Small signal input from the VCO.
19	17	GND	—	Ground for IF digital, MICROWIRE, $F_{oLD}$ , and oscillator circuits.
20	18	$D_o$ IF	O	IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
22	19	$V_{P2}$	—	Power Supply for IF charge pump. Must be $\geq V_{CC}$ .
23	20	$V_{CC2}$	—	Power supply voltage input for IF analog, IF digital, MICROWIRE, $F_{oLD}$ , and oscillator circuits. Input may range from 2.7V to 5.5V. $V_{CC2}$ must equal $V_{CC1}$ . Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
1, 9, 13, 21	X	NC	—	No connect.

### Block Diagram



DS101366-3

**Note:** The RF prescaler for the LMX2331U/32U is either 64/65 or 128/129, while the prescaler for the LMX2330U is 32/33 or 64/65.  
**Note:** V<sub>CC1</sub> supplies power to the RF prescaler, N-counter, R-counter and phase detector. V<sub>CC2</sub> supplies power to the IF prescaler, N-counter, phase detector, R-counter along with the OSC<sub>in</sub> buffer, MICROWIRE, and F<sub>o</sub>LD. V<sub>CC1</sub> and V<sub>CC2</sub> are clamped to each other by diodes and must be run at the same voltage level.  
**Note:** V<sub>p1</sub> and V<sub>p2</sub> can be run separately as long as V<sub>p</sub> ≥ V<sub>CC</sub>.

**Absolute Maximum Ratings** (Notes 1,

2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage

$$V_{CC} \quad -0.3V \text{ to } +6.5V$$

$$V_P \quad -0.3V \text{ to } +6.5V$$

Voltage on Any Pin

$$\text{with GND} = 0V (V_I) \quad -0.3V \text{ to } V_{CC} + 0.3V$$

Storage Temperature Range ( $T_S$ )  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$ Lead Temperature (solder 4 sec.) ( $T_L$ )  $+260^\circ\text{C}$ **Recommended Operating Conditions**

Power Supply Voltage

$$V_{CC} \quad 2.7V \text{ to } 5.5V$$

$$V_P \quad V_{CC} \text{ to } +5.5V$$

Operating Temperature ( $T_A$ )

$$-40^\circ\text{C} \text{ to } +85^\circ\text{C}$$

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the conditions listed.

**Note 2:** This device is a high performance RF integrated circuit with an ESD rating  $<2$  kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

**Electrical Characteristics**
 $V_{CC} = 3.0V$ ,  $V_P = 3.0V$ ;  $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ , except as specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
$I_{CC}$	Power Supply Current	LMX2330U RF + IF			3.3	4.3	mA
		LMX2330U RF Only			2.3	3.4	
		LMX2331U RF + IF			2.9	3.8	
		LMX2331U RF Only			1.9	2.5	
		LMX2332U RF + IF			2.5	3.3	
		LMX2332U RF Only			1.5	2.0	
		LMX233xU IF Only			1.0	1.3	
$I_{CC-PWDN}$	Powerdown Current		(Note 3)		1.0	10	$\mu\text{A}$
$f_{IN}$ RF	Operating Frequency	LMX2330U		0.5		2.5	GHz
		LMX2331U		0.2		2.0	
		LMX2332U		0.1		1.2	
$f_{IN}$ IF	Operating Frequency	LMX233xU		45		600	MHz
$f_{OSC}$	Oscillator Frequency			5		40	MHz
$f_\phi$	Maximum Phase Detector Frequency			10			MHz
$Pf_{IN}$ RF	RF Input Sensitivity		$V_{CC} = 3.0V$	-15		0	dBm
			$V_{CC} = 5.5V$	-10		0	dBm
$Pf_{IN}$ IF	IF Input Sensitivity		$V_{CC} = 2.7V \text{ to } 5.5V$	-10		0	dBm
$V_{OSC}$	Oscillator Sensitivity			0.5			$V_{PP}$
$V_{IH}$	High-Level Input Voltage		(Note 4)	$0.8 V_{CC}$			V
$V_{IL}$	Low-Level Input Voltage		(Note 4)			$0.2 V_{CC}$	V
$I_{IH}$	High-Level Input Current		$V_{IH} = V_{CC} = 5.5V$ (Note 4)	-1.0		1.0	$\mu\text{A}$
$I_{IL}$	Low-Level Input Current		$V_{IL} = 0V$ , $V_{CC} = 5.5V$ (Note 4)	-1.0		1.0	$\mu\text{A}$
$I_{IH}$	Oscillator Input Current		$V_{IH} = V_{CC} = 5.5V$			100	$\mu\text{A}$
$I_{IL}$	Oscillator Input Current		$V_{IL} = 0V$ , $V_{CC} = 5.5V$	-100			$\mu\text{A}$
$V_{OH}$	High-Level Output Voltage (for $F_oLD$ )		$I_{OH} = -500 \mu\text{A}$	$V_{CC} - 0.4$			V
$V_{OL}$	Low-Level Output Voltage (for $F_oLD$ )		$I_{OL} = 500 \mu\text{A}$			0.4	V
$t_{CS}$	Data to Clock Set Up Time		See Data Input Timing	50			ns
$t_{CH}$	Data to Clock Hold Time		See Data Input Timing	10			ns
$t_{CWH}$	Clock Pulse Width High		See Data Input Timing	50			ns

## Electrical Characteristics (Continued)

$V_{CC} = 3.0V$ ,  $V_P = 3.0V$ ;  $-40^{\circ}C < T_A < 85^{\circ}C$ , except as specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
$t_{CWL}$	Clock Pulse Width Low	See Data Input Timing	50			ns
$t_{ES}$	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
$t_{EW}$	Load Enable Pulse Width	See Data Input Timing	50			ns

**Note 3:** Clock, Data and LE = GND or  $V_{CC}$ .

**Note 4:** Clock, Data and LE does not include  $f_{IN}$  RF,  $f_{IN}$  IF and  $OSC_{IN}$ .

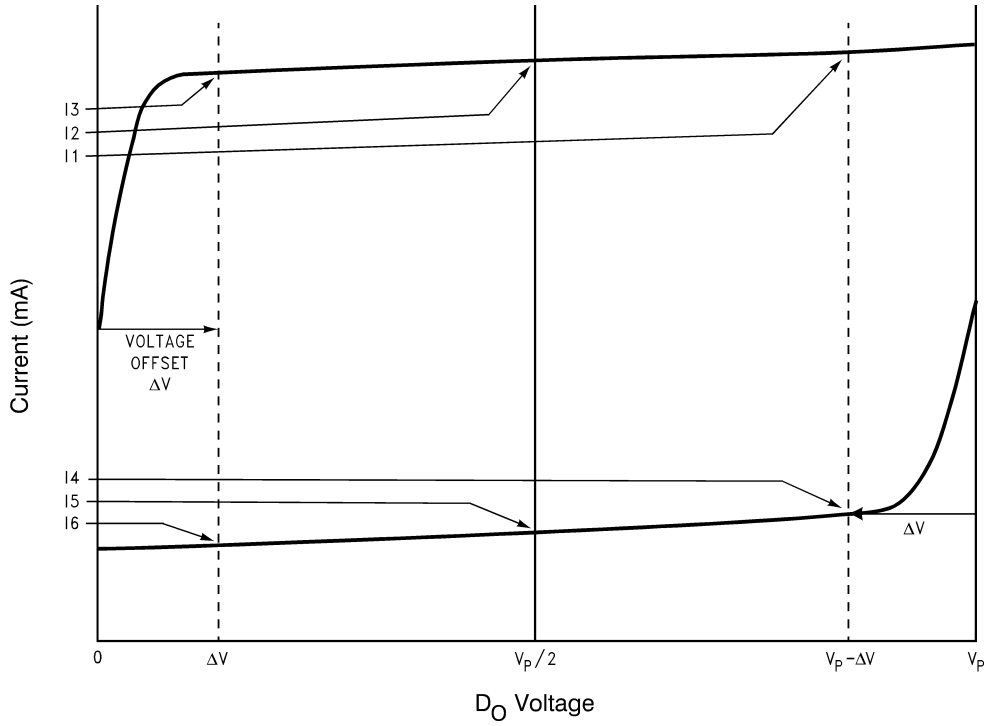
## Charge Pump Characteristics

$V_{CC} = 3.0V$ ,  $V_P = 3.0V$ ;  $-40^{\circ}C < T_A \leq 85^{\circ}C$ , except as specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
$I_{D0}$ -SOURCE	Charge Pump Output Current	$V_{D0} = V_P/2$ , $I_{CP0} = \text{HIGH}$ (Note 5)		-3.8		mA
$I_{D0}$ -SINK		$V_{D0} = V_P/2$ , $I_{CP0} = \text{HIGH}$ (Note 5)		3.8		mA
$I_{D0}$ -SOURCE		$V_{D0} = V_P/2$ , $I_{CP0} = \text{LOW}$ (Note 5)		-0.95		mA
$I_{D0}$ -SINK		$V_{D0} = V_P/2$ , $I_{CP0} = \text{LOW}$ (Note 5)		0.95		mA
$I_{D0}$ -TRI	Charge Pump TRI-STATE Current	$0.5V \leq V_{D0} \leq V_P - 0.5V$	-2.5		2.5	nA
$I_{D0}$ -SINK vs $I_{D0}$ -SOURCE	CP Sink vs Source Mismatch (Note 7)	$V_{D0} = V_P/2$ $T_A = 25^{\circ}C$		3	10	%
$I_{D0}$ vs $V_{D0}$	CP Current vs Voltage (Note 6)	$0.5 \leq V_{D0} \leq V_P - 0.5V$ $T_A = 25^{\circ}C$		10	15	%
$I_{D0}$ vs $T_A$	CP Current vs Temperature (Note 8)	$V_{D0} = V_P/2$ $-40^{\circ}C \leq T_A \leq 85^{\circ}C$		10		%

**Note 5:** See PROGRAMMABLE MODES for  $I_{D0}$  description.

## Charge Pump Current Specification Definitions



DS101366-37

- I1 = CP sink current at  $V_{D0} = V_p - \Delta V$
- I2 = CP sink current at  $V_{D0} = V_p/2$
- I3 = CP sink current at  $V_{D0} = \Delta V$
- I4 = CP source current at  $V_{D0} = V_p - \Delta V$
- I5 = CP source current at  $V_{D0} = V_p/2$
- I6 = CP source current at  $V_{D0} = \Delta V$

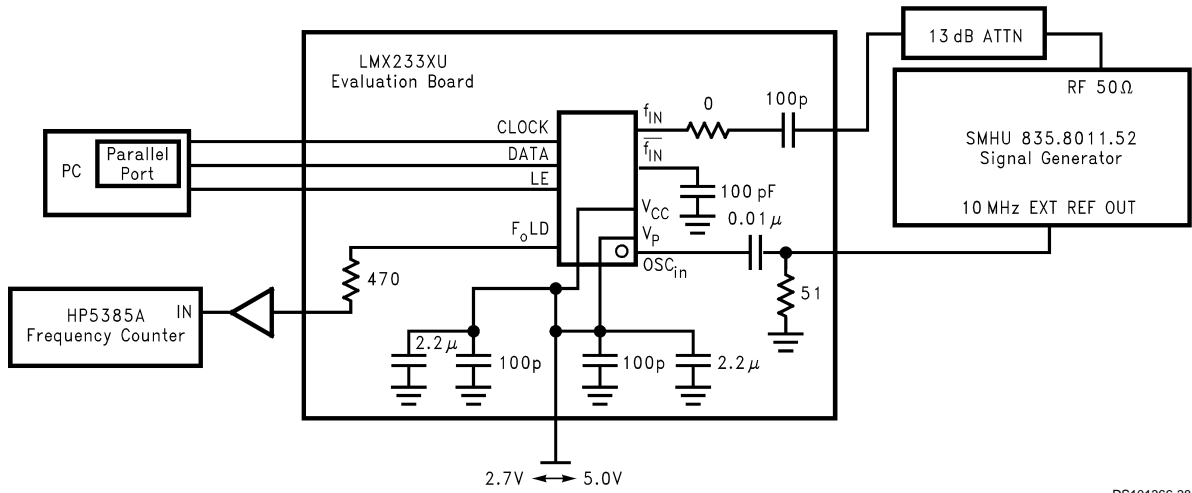
$\Delta V$  = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to  $V_{CC}$  and ground. Typical values are between 0.5V and 1.0V.

**Note 6:**  $I_{D0}$  vs  $V_{D0}$  = Charge Pump Output Current magnitude variation vs Voltage =  
 $[\frac{1}{2} * \{|I1| - |I3|\}] / [\frac{1}{2} * \{|I1| + |I3|\}] * 100\%$  and  $[\frac{1}{2} * \{|I4| - |I6|\}] / [\frac{1}{2} * \{|I4| + |I6|\}] * 100\%$

**Note 7:**  $I_{D0-sink}$  vs  $I_{D0-source}$  = Charge Pump Output Current Sink vs Source Mismatch =  
 $[|I2| - |I5|] / [\frac{1}{2} * \{|I2| + |I5|\}] * 100\%$

**Note 8:**  $I_{D0}$  vs  $T_A$  = Charge Pump Output Current magnitude variation vs Temperature =  
 $[|I2 @ temp| - |I2 @ 25^\circ C|] / |I2 @ 25^\circ C| * 100\%$  and  $[|I5 @ temp| - |I5 @ 25^\circ C|] / |I5 @ 25^\circ C| * 100\%$

# RF Sensitivity Test Block Diagram



**Note 1:** N = 10,000 R = 50 P = 64

**Note 2:** Sensitivity limit is reached when the error of the divided RF output, F<sub>o</sub>LD, is ≥ 1 Hz.

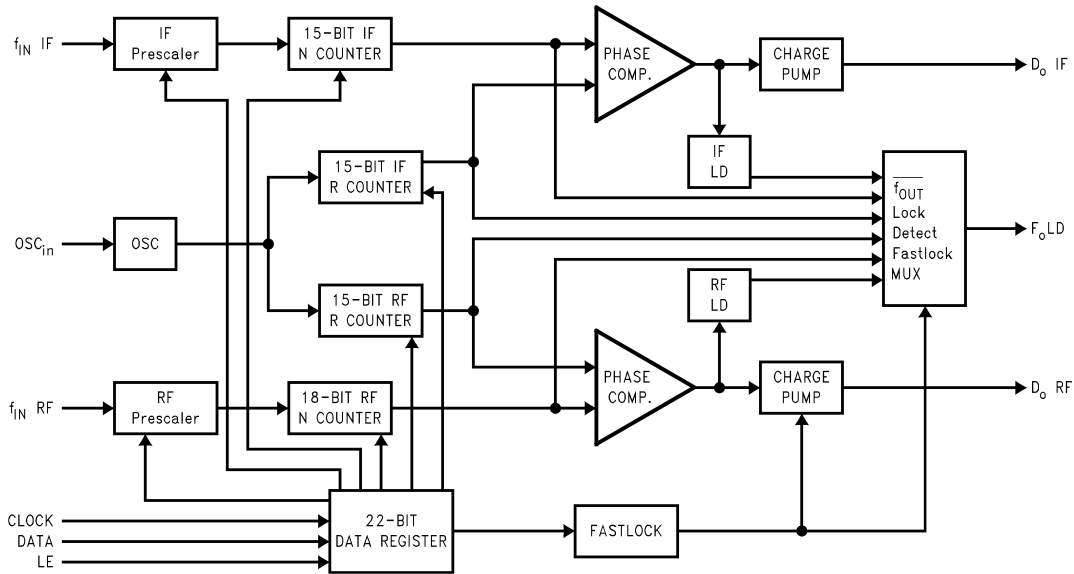
DS101366-38



## Functional Description

The simplified block diagram below shows the 22-bit data register, two 15-bit R Counters and the 15- and 18-bit N Counters (intermediate latches are not shown). The data stream is clocked (on the rising edge of Clock) into the DATA register, MSB first. The data stored in the shift register is loaded into one of 4 appropriate latches on the rising edge of LE. The last two bits are the Control Bits. The DATA is transferred into the counters as follows:

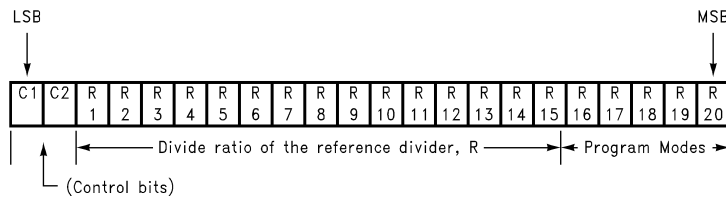
Control Bits		DATA Location
C1	C2	
0	0	IF R Counter
0	1	RF R Counter
1	0	IF N Counter
1	1	RF N Counter



DS101366-6

### PROGRAMMABLE REFERENCE DIVIDERS (IF AND RF R COUNTERS)

If the Control Bits are 00 or 01 (00 for IF and 01 for RF) data is transferred from the 22-bit shift register into a latch which sets the 15-bit R Counter. Serial data format is shown below.



DS101366-7

### 15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

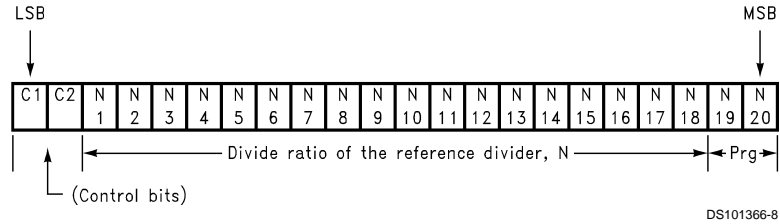
**Notes:**

- Divide ratios less than 3 are prohibited.
- Divide ratio: 3 to 32767
- R1 to R15: These bits select the divide ratio of the programmable reference divider.
- Data is shifted in MSB first.

## Functional Description (Continued)

### PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for IF counter and 11 for RF counter) data is transferred from the 22-bit shift register into a 4-bit or 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below. **For the IF N counter bits 5, 6, and 7 are don't care bits.** The RF N counter does not have don't care bits.



### 7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

RF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Notes: Divide ratio: 0 to 127  
B ≥ A

IF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

X = DON'T CARE condition

### 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio B	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)  
B ≥ A

### PULSE SWALLOW FUNCTION

$$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$$

- f<sub>VCO</sub>: Output frequency of external voltage controlled oscillator (VCO)
- B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)
- A: Preset divide ratio of binary 7-bit swallow counter  
(0 ≤ A ≤ 127 {RF}, 0 ≤ A ≤ 15 {IF}, A ≤ B)
- f<sub>OSC</sub>: Output frequency of the external reference frequency oscillator
- R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)
- P: Preset modulus of dual modulus prescaler (for IF; P = 8 or 16;  
for RF; LMX2330U: P = 32 or 64 LMX2331U/32U: P = 64 or 128)

## Functional Description (Continued)

### PROGRAMMABLE MODES

Several modes of operation can be programmed with bits R16–R20 including the phase detector polarity, charge pump TRI-STATE and the output of the F<sub>o</sub>LD pin. The prescaler and powerdown modes are selected with bits N19 and N20. The programmable modes are shown in *Table 1*. Truth table for the programmable modes and F<sub>o</sub>LD output are shown in *Table 2* and *Table 3*.

**TABLE 1. Programmable Modes**

C1	C2	R16	R17	R18	R19	R20
0	0	IF Phase Detector Polarity	IF I <sub>CPo</sub>	IF D <sub>o</sub> TRI-STATE	IF LD	IF F <sub>o</sub>
0	1	RF Phase Detector Polarity	RF I <sub>CPo</sub>	RF D <sub>o</sub> TRI-STATE	RF LD	RF F <sub>o</sub>

C1	C2	N19	N20
1	0	IF Prescaler	Pwdn IF
1	1	RF Prescaler	Pwdn RF

**TABLE 2. Mode Select Truth Table**

	Phase Detector Polarity (Note 11)	D <sub>o</sub> TRI-STATE (Note 9)	I <sub>CPo</sub> (Note 10)	IF Prescaler	2330L RF Prescaler	2331L/32L RF Prescaler	Pwdn (Note 9)
0	Negative	Normal Operation	LOW	8/9	32/33	64/65	PwrD Up
1	Positive	TRI-STATE	HIGH	16/17	64/65	128/129	PwrD Dn

**Note 9:** Refer to POWERDOWN OPERATION in Functional Description.

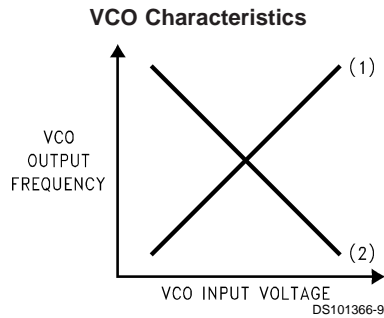
**Note 10:** The I<sub>CPo</sub> LOW current state = 1/4 x I<sub>CPo</sub> HIGH current.

**Note 11:** PHASE DETECTOR POLARITY

Depending upon VCO characteristics, R16 bit should be set accordingly: (see figure right)

When VCO characteristics are positive like (1), R16 should be set HIGH;

When VCO characteristics are negative like (2), R16 should be set LOW.



## Functional Description (Continued)

**TABLE 3. The F<sub>o</sub>LD (Pin 10) Output Truth Table**

RF R[19] (RF LD)	IF R[19] (IF LD)	RF R[20] (RF F <sub>o</sub> )	IF R[20] (IF F <sub>o</sub> )	F <sub>o</sub> Output State
0	0	0	0	Disabled (Note 12)
0	1	0	0	IF Lock Detect (Note 13)
1	0	0	0	RF Lock Detect (Note 13)
1	1	0	0	RF/IF Lock Detect (Note 13)
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output
0	0	1	1	Fastlock (Note 14)
0	1	1	1	IF Counter Reset (Note 15)
1	0	1	1	RF Counter Reset (Note 15)
1	1	1	1	IF and RF Counter Reset (Note 15)

X = don't care condition

**Note 12:** When the F<sub>o</sub>LD output is disabled, it is actively pulled to a low logic state.

**Note 13:** Lock detect output provided to indicate when the VCO frequency is in "lock." When the loop is locked and a lock detect mode is selected, the pins output is HIGH, with narrow pulses LOW. In the RF/IF lock detect mode a locked condition is indicated when RF and IF are both locked.

**Note 14:** The Fastlock mode utilizes the F<sub>o</sub>LD output pin to switch a second loop filter damping resistor to ground during fastlock operation. Activation of Fastlock occurs whenever the RF loop's lcpo magnitude bit #17 is selected HIGH (while the #19 and #20 mode bits are set for Fastlock).

**Note 15:** The IF Counter Reset mode resets IF PLL's R and N counters and brings IF charge pump output to a TRI-STATE condition. The RF Counter Reset mode resets RF PLL's R and N counters and brings RF charge pump output to a TRI-STATE condition. The IF and RF Counter Reset mode resets all counters and brings both charge pump outputs to a TRI-STATE condition. Upon removal of the Reset bits then N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle.)

### POWERDOWN OPERATION

Synchronous and asynchronous powerdown modes are both available by MICROWIRE selection. Synchronous powerdown occurs if the respective loop's R18 bit (Do TRI-STATE) is LOW when its N20 bit (Pwdr) becomes HI. Asynchronous powerdown occurs if the loop's R18 bit is HI when its N20 bit becomes HI.

In the synchronous powerdown mode, the powerdown function is gated by the charge pump to prevent unwanted frequency jumps. Once the powerdown program bit N20 is loaded, the part will go into powerdown mode when the charge pump reaches a TRI-STATE condition.

In the asynchronous powerdown mode, the device powers down immediately after the LE pin latches in a HI condition on the powerdown bit N20.

Activation of either the IF or RF PLL powerdown conditions in either synchronous or asynchronous modes forces the respective loop's R and N dividers to their load state condition and debiasing of its respective f<sub>IN</sub> input to a high impedance state. The oscillator circuitry function does not become disabled until both IF and RF powerdown bits are activated. The MICROWIRE control register remains active and capable of loading and latching data during all of the powerdown modes.

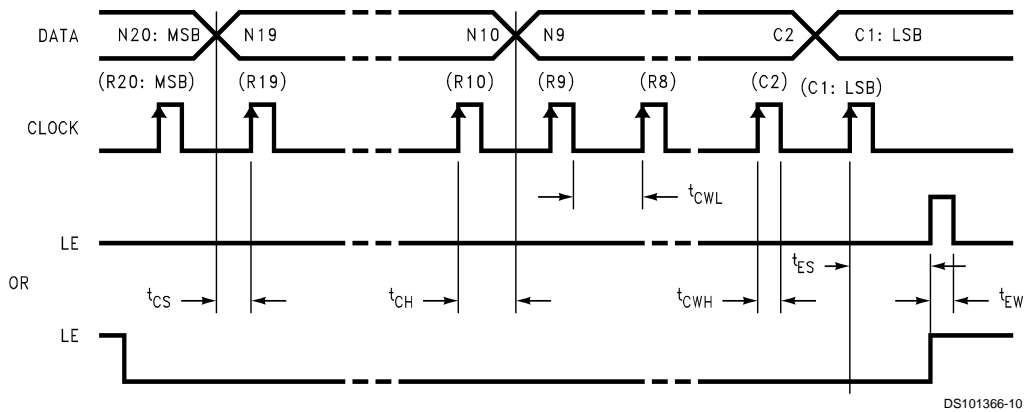
The device returns to an actively powered up condition in either synchronous or asynchronous modes immediately upon LE latching LOW data into bit N20.

### Powerdown Mode Select Table

R18	N20	Powerdown Status
0	0	PLL Active
1	0	PLL Active (Charge Pump Output TRI-STATE)
0	1	Synchronous Powerdown Initiated
1	1	Asynchronous Powerdown Initiated

## Functional Description (Continued)

### SERIAL DATA INPUT TIMING



DS101366-10

**Note 1:** Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

**Note 2:**  $t_{cs}$  = Data to Clock Set-Up Time

$t_{ch}$  = Data to Clock Hold Time

$t_{cwh}$  = Clock Pulse Width High

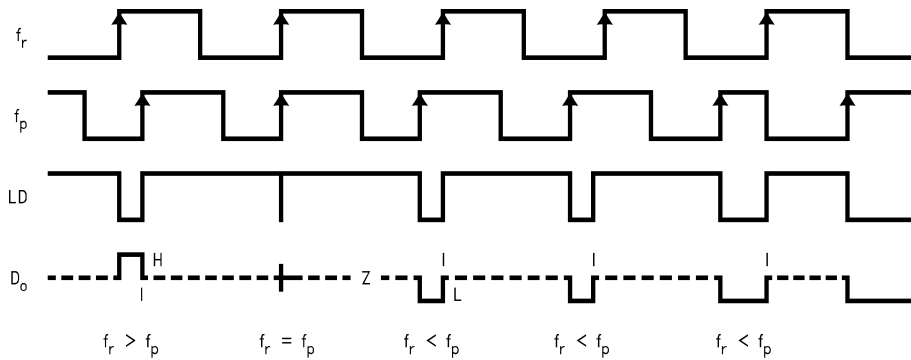
$t_{cwl}$  = Clock Pulse Width Low

$t_{es}$  = Clock to Load Enable Set-Up Time

$t_{ew}$  = Load Enable Pulse Width

**Test Conditions:** The Serial Data Input Timing is tested using a symmetrical waveform around  $V_{CC}/2$ . The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @  $V_{CC} = 2.7V$  and 2.6V @  $V_{CC} = 5.5V$ .

### PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



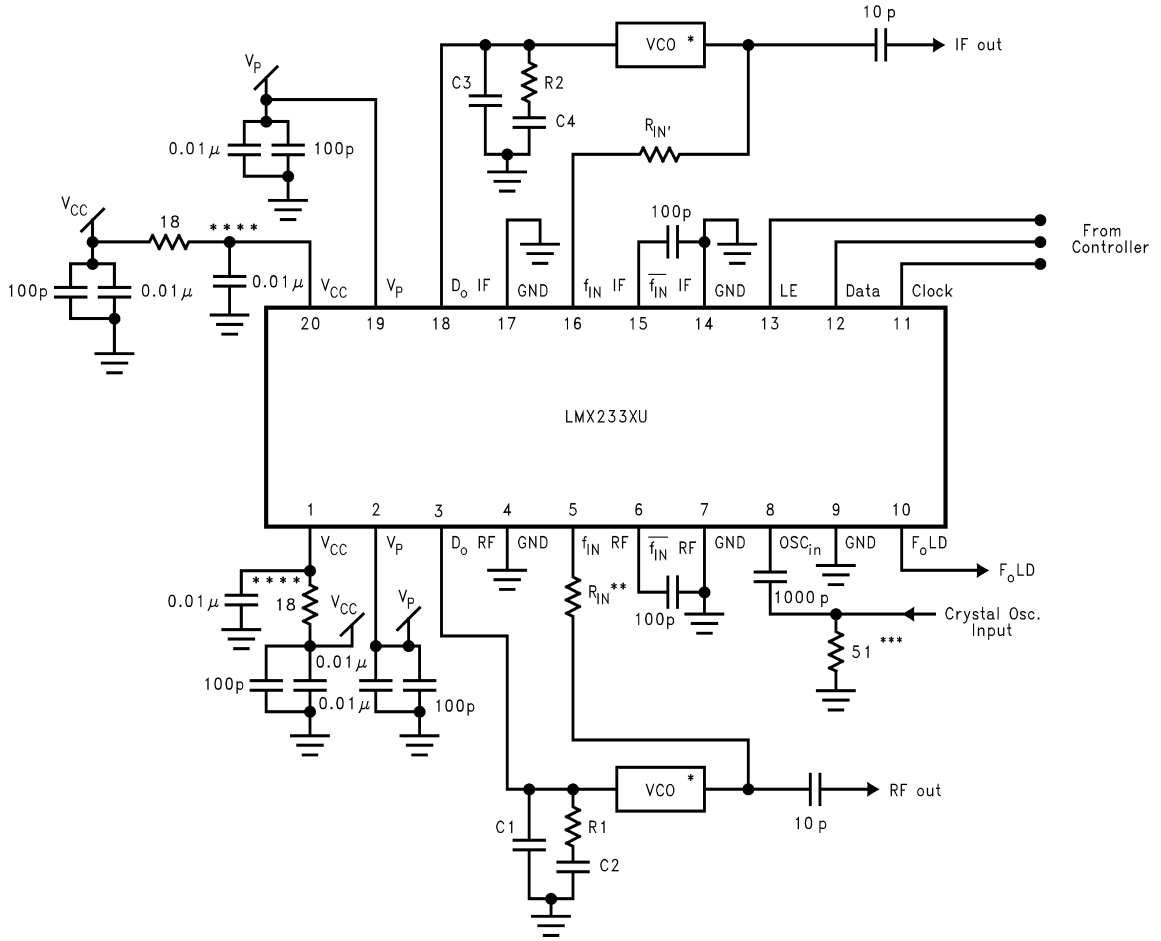
DS101366-11

**Notes:** Phase difference detection range:  $-2\pi$  to  $+2\pi$

The minimum width pump up and pump down current pulses occur at the  $D_o$  pin when the loop is locked.

R16 = HIGH

## Typical Application Example



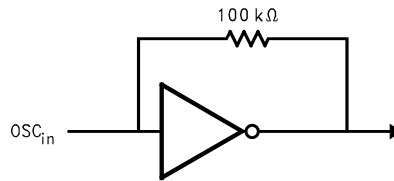
DS101366-12

### Operational Notes:

\* VCO is assumed AC coupled.

\*\*  $R_{IN}$  increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10 $\Omega$  to 200 $\Omega$  depending on the VCO power level.  $f_{IN}$  RF impedance ranges from 40 $\Omega$  to 100 $\Omega$ .  $f_{IN}$  IF impedances are higher.

\*\*\* Adding RC filters to the  $V_{CC}$  lines is recommended to reduce loop-to-loop noise coupling.



DS101366-13

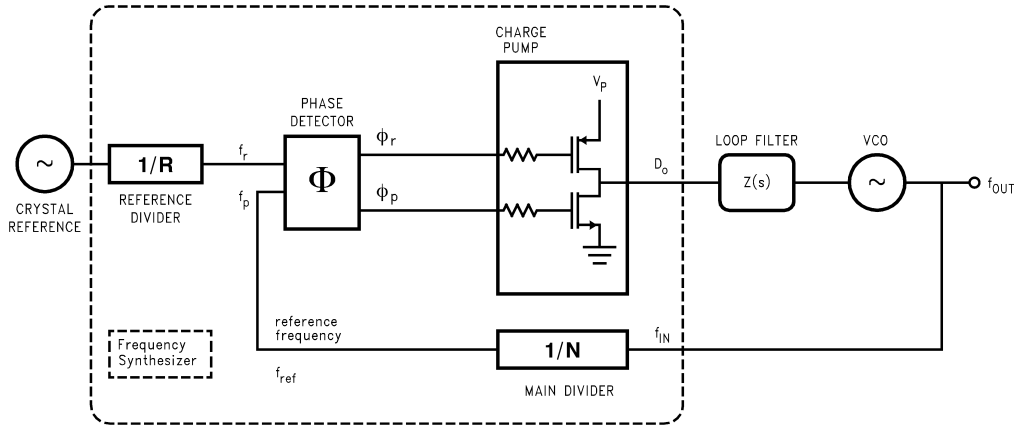
### Application Hints:

Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.

This is an electrostatic sensitive device. It should be handled only at static free work stations.

## Application Information

A block diagram of the basic phase locked loop is shown in *Figure 1*.

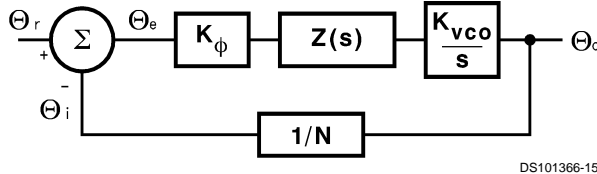


DS101366-14

**FIGURE 1. Basic Charge Pump Phase Locked Loop**

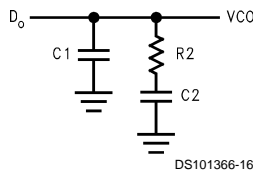
### LOOP GAIN EQUATIONS

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain ( $K_\phi$ ), the VCO gain ( $K_{VCO}/s$ ), and the loop filter gain  $Z(s)$  divided by the gain of the feedback counter modulus ( $N$ ). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in *Equation (1)*.



DS101366-15

**FIGURE 2. PLL Linear Model**



DS101366-16

**FIGURE 3. Passive Loop Filter**

$$\begin{aligned} \text{Open loop gain} &= H(s)G(s) = \Theta_i/\Theta_e \\ &= K_\phi Z(s) K_{VCO}/Ns \\ Z(s) &= \frac{s(C2 \cdot R2) + 1}{s^2(C1 \cdot C2 \cdot R2) + sC1 + sC2} \end{aligned} \quad (1)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \cdot \frac{C1 \cdot C2}{C1 + C2} \quad (2)$$

and

$$T2 = R2 \cdot C2 \quad (3)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency,  $\omega$ , the filter time constants  $T1$  and  $T2$ , and the design constants  $K_\phi$ ,  $K_{VCO}$ , and  $N$ .

$$G(s) \cdot H(s) \Big|_{s=j\omega} = \frac{-K_\phi \cdot K_{VCO} (1 + j\omega \cdot T2)}{\omega^2 C1 \cdot N (1 + j\omega \cdot T1)} \cdot \frac{T1}{T2} \quad (4)$$

From *Equations (2)*, *(3)* we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in *Equation (5)*.

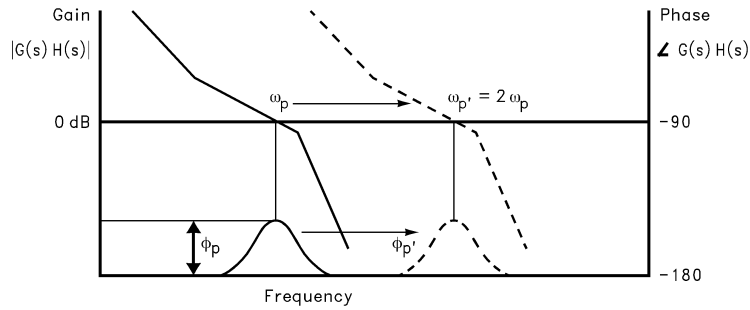
$$\phi(\omega) = \tan^{-1}(\omega \cdot T2) - \tan^{-1}(\omega \cdot T1) + 180^\circ \quad (5)$$

A plot of the magnitude and phase of  $G(s)H(s)$  for a stable loop, is shown in *Figure 4* with a solid trace. The parameter  $\phi_p$  shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency  $\omega_p$  of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency,  $\omega_p'$ , as double the frequency which gave us our original bandwidth,  $\omega_p$ , the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase *Equation (4)* and *Equation (5)* will have to compensate by the corresponding "1/w" or "1/w<sup>2</sup>" factor. Examination of *Equations (2)*, *(3)* and *Equation (5)* indicates the damping resistor variable  $R2$  could be chosen to compensate the "w" terms for the phase margin. This implies that another resistor of equal value to  $R2$  will need to be switched in parallel with  $R2$  during the initial lock period. We must also insure that the magnitude of the open loop gain,  $H(s)G(s)$  is equal to zero at  $\omega_p' = 2\omega_p$ .  $K_{VCO}$ ,  $K_\phi$ ,  $N$ , or the net product of these terms can be changed by a factor of 4, to counteract the  $w^2$  term present in the denominator of *Equation (2)* and *Equation (3)*. The  $K_\phi$  term was chosen to complete the transformation because it

## Application Information (Continued)

can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in Fastlock.



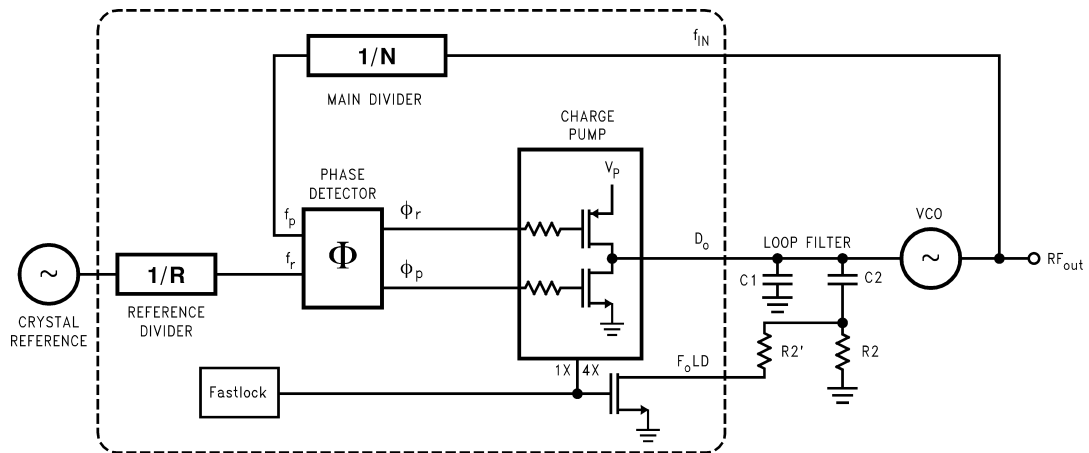
DS101366-17

**FIGURE 4. Open Loop Response Bode Plot**

### FASTLOCK CIRCUIT IMPLEMENTATION

A diagram of the Fastlock scheme as implemented in National Semiconductors LMX233xU PLL is shown in *Figure 5*. When a new frequency is loaded, and the RF Icp<sub>o</sub> bit is set high, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second

identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending a MICROWIRE instruction with the RF Icp<sub>o</sub> bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronously with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

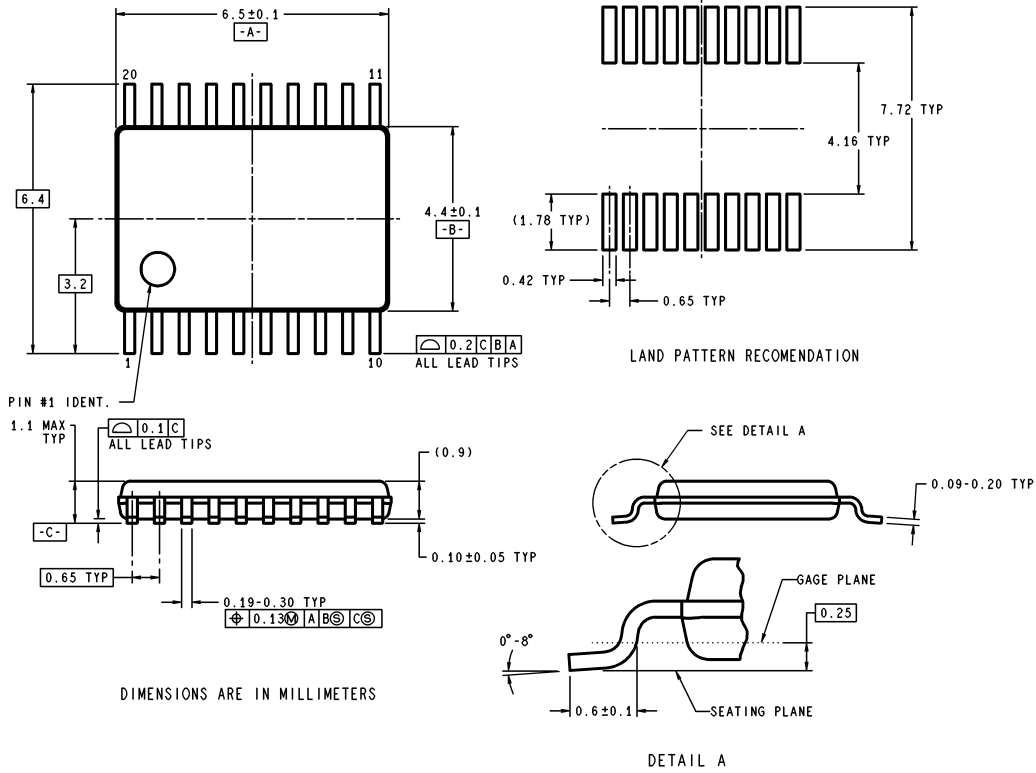


DS101366-18

**FIGURE 5. Fastlock PLL Architecture**

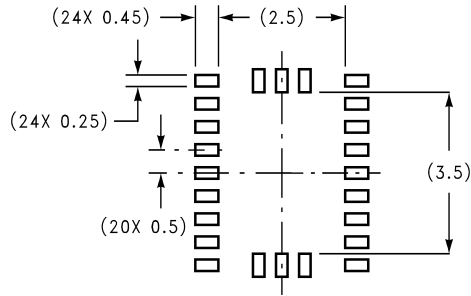


**Physical Dimensions** inches (millimeters) unless otherwise noted



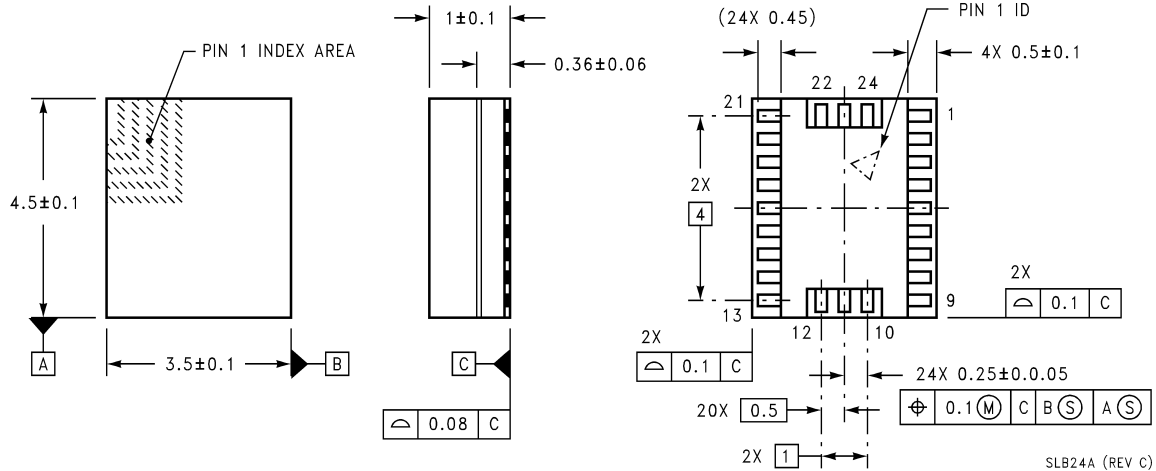
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**\*For Tape and Reel (2500 units per reel)**  
**Order Number LMX2330UTMX, LMX2331UTMX or LMX2332UTMX**  
**NS Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

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