INCH-POUND

MIL-M-38510/22D
12 August 2005
SUPERSEDING
MIL-M-38510/22C
27 February 1989

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, HIGH-SPEED TTL, FLIP-FLOPS, MONOLITHIC SILICON

Inactive for new design after 6 September 1996.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, high speed TTL, bistable logic microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop
03	Dual, D-type edge-triggered flip-flop
04	Dual J-K master-slave flip-flop
05	Single J-K edge-triggered flip-flop
06	Dual J-K edge-triggered flip-flop

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A	GDFP5-F14 or CDFP6-F14	14	Flat pack
B	GDFP4-F14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 to 7.0 V dc
Input voltage range	-1.5 V dc at 12 mA to 5.5 V dc
Storage temperature range	-65°C to 150°C
Maximum power dissipation per flip-flop (P_D): 1/	
Device types 01, 02, 03, and 04	137 mW
Device types 05 and 06	210 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	(See MIL-STD-1835)
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc
Normalized fanout (each output): 2/	
Device types 01, 02, 04, 05, and 06	10 maximum
Device type 03	10 maximum (low logic) 20 maximum (high logic)
Case operating temperature range (T_C)	55°C to +125°C
Width of clock pulse, t_P (clock):	
Device types 01, 02, and 04	12 ns, minimum
Device type 03	15 ns, minimum
Device types 05 and 06	10 ns, minimum
Width of preset or clear pulse:	
Device types 01, 02, 04, 05, and 06	16 ns, minimum
Device type 03	25 ns, minimum
Input setup time $t_{(SETUP)}$:	
Device types 01, 02, and 04	$\geq t_P$(clock)
Device type 03	15 ns, minimum (low level data) 10 ns, minimum (high level data)
Device types 05 and 06	10 ns, minimum (high level data) 13 ns, minimum (low level data)
Input hold time $t_{(HOLD)}$	5 ns, minimum

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

1/ Must withstand the added P_D due to short circuit condition (e.g., I_{OS}) at one output for 5 seconds duration.
2/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3.2 Terminal connections. The terminal connections shall be as specified on figures 1.

3.3.3 Truth tables. The truth tables shall be as specified on figures 2.

3.3.4 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 3 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device types	Terminals (device type)						Limits		Unit
				01	02	03	04	05	06	Min	Max	
High level output voltage	V_{OH}	V_{IN} = 0.8 V V_{CC} = 4.5 V I_{OH} = -500 µA	01,02							2.4		V
		I_{OH} = -1 mA	03									
		I_{OH} = -0.5 mA	04,05,06									
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 20 mA									0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -12 mA T_C = +25°C									-1.5	V
Low level input current	I_{IL1}	V_{CC} = 5.5 V V_{IN} = 0.4 V		J, K Clock	J, K Clock	D	J, K Clock	Preset J, K	J, K Clear	-1.0	-2.0	mA
Low level input current	I_{IL2}	V_{CC} = 5.5 V V_{IN} = 0.4 V	01,02, 03,04	Preset Clear	Clear	Preset Clock Clear	Preset Clear			-2.0	-4.0	mA
			05,06					Clock	Clock	-2.0	-4.8	
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.4 V		J, K	J, K	D	J, K	J, K	J, K		50	µA
High level input current	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 5.5 V	01,02, 03,04	J, K	J, K	D	J, K	J, K			100	µA
			05, 06						J, K		1	mA
High level input current	I_{IH3}	V_{CC} = 5.5 V V_{IN} = 2.4 V	01,02, 03,04,05	Clear Preset	Clear	Clock Preset	Preset Clock Clear	Preset			100	µA
			06						Clock	-1	1	mA
High level input current	I_{IH4}	V_{CC} = 5.5 V V_{IN} = 5.5 V	01,02, 03,04,05	Clear Preset	Clear	Clock Preset	Preset Clock Clear	Preset			200	µA
			06						Clock		1	mA
High level input current	I_{IH5}	V_{CC} = 5.5 V V_{IN} = 2.4 V	01,02	Clock	Clock	Clear					100	µA
			03								150	µA
			05					Clock			-1	mA
			06						Clear		100	µA
High level input current	I_{IH6}	V_{CC} = 5.5 V V_{IN} = 5.5 V	01,02	Clock	Clock	Clear					200	µA
			03								300	µA
			05,06					Clock	Clear		1	mA
Short circuit output current 1/	I_{OS}	V_{CC} = 5.5 V V_{IN} = 0 V								-40	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V	01								25	mA
			02,03,04								50	
			05								38	
			06								76	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device types	Limits		Unit
					Min	Max	
Maximum clock frequency 2/	f_{MAX}	C_L = 50 pF R_L = 280Ω	Figure 4	01	20		MHz
			Figure 6	02	20		
			Figure 8	03	28		
			Figure 11	04	20		
			Figure 13	05	30		
			Figure 15	06	30		
Propagation delay to a logical 1 (clear or preset to output)	t_{PLH1}	C_L = 50 pF R_L = 280Ω	Figure 3	01	2	20	ns
			Figure 5	02	"	20	
			Figure 7	03	"	27	
			Figure 10	04	"	20	
			Figure 12	05	"	28	
			Figure 14	06	"	18	
Propagation delay to a logical 0 (clear or preset to output)	t_{PHL1}	C_L = 50 pF R_L = 280Ω	Figure 3	01	2	31	ns
			Figure 5	02	"	31	
			Figure 7	03	"	38	
			Figure 10	04	"	32	
			Figure 12	05	"	28	
			Figure 14	06	"	46	
Propagation delay to a logical 1 (clock to output)	t_{PLH2}	C_L = 50 pF R_L = 280Ω	Figure 4	01	2	28	ns
			Figure 6	02	"	35	
			Figure 8 and 9	03	"	22	
			Figure 11	04	"	28	
			Figure 13	05	"	23	
			Figure 15	06	"	23	
Propagation delay to a logical 0 (clock to output)	t_{PHL2}	C_L = 50 pF R_L = 280Ω	Figure 4	01	2	37	ns
			Figure 6	02	"	42	
			Figure 8 and 9	03	"	28	
			Figure 11	04	"	36	
			Figure 13	05	"	28	
			Figure 15	06	"	28	

1/ Not more than one output should be shorted at a time.
2/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroup (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3	N/A
Group C end-point electrical parameters	1, 2, 3	1, 2, 3
Additional electrical subgroups for Group C periodic inspections	N/A	10, 11
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A. The sample size series number shall be 5 (45 devices accept on 0).

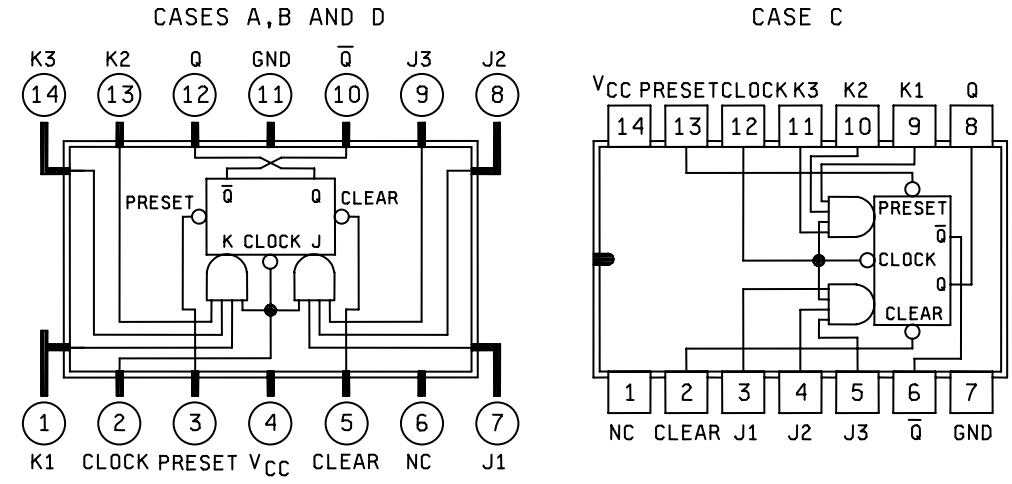
c. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

DEVICE TYPE 01



DEVICE TYPE 02

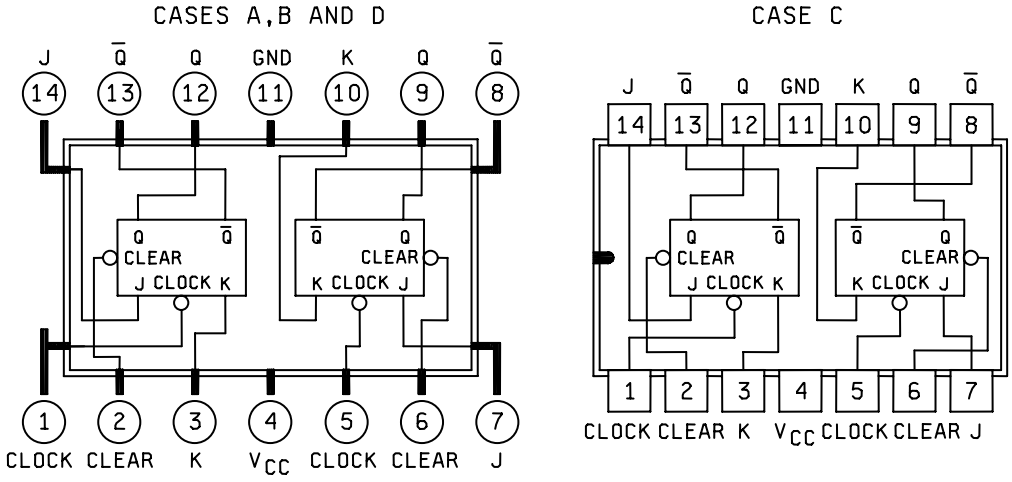
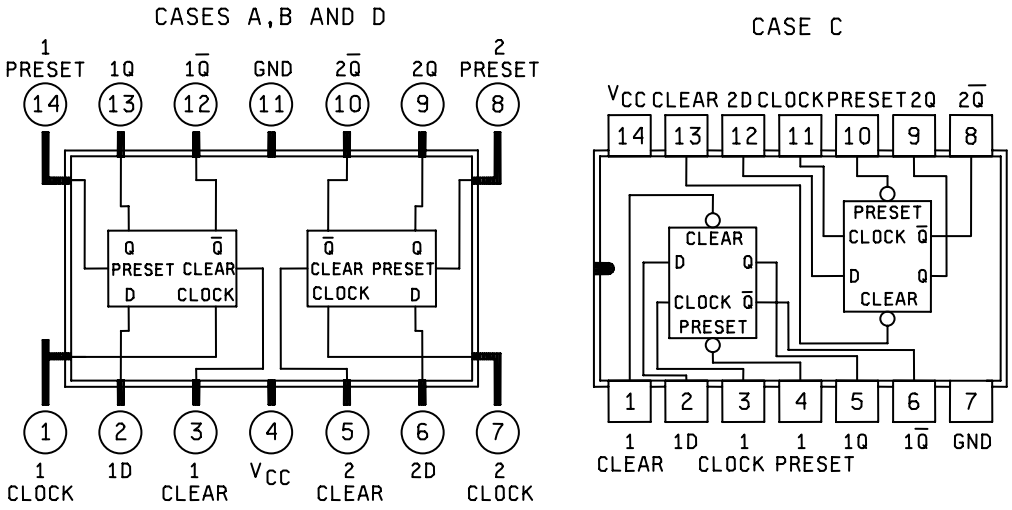


FIGURE 1. Terminal connections.

DEVICE TYPE 03



DEVICE TYPE 04

CASES E AND F

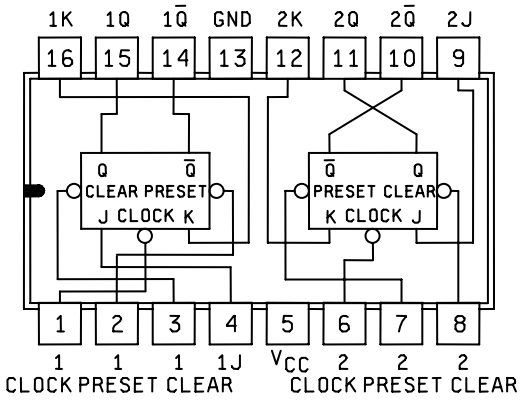
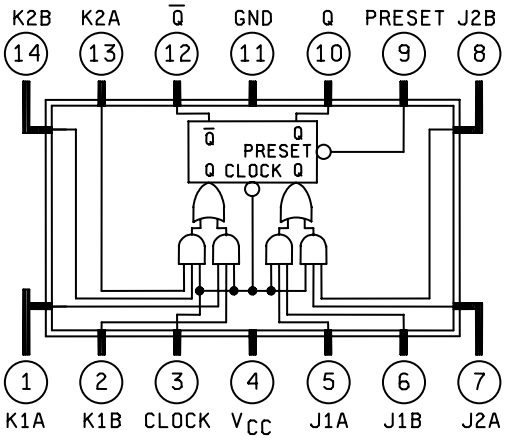


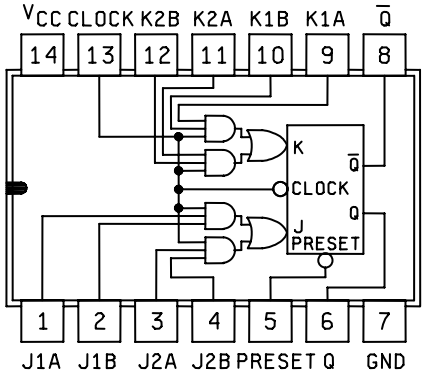
FIGURE 1. Terminal connections - Continued.

DEVICE TYPE 05

CASES A,B AND D

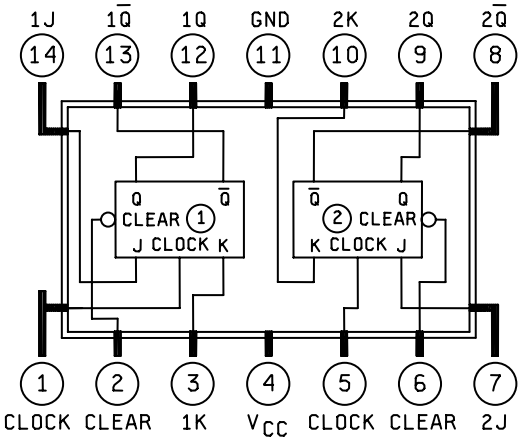


CASE C



DEVICE TYPE 06

CASES A,B AND D



CASE C

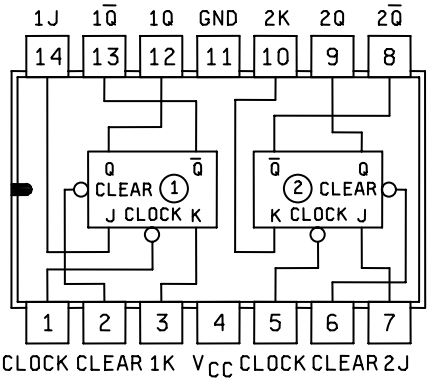


FIGURE 1. Terminal connections - Continued.

Device type 01

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}n$

Positive logic: Low input to preset sets Q to high level.
Low input to clear sets Q to low level.
Preset and clear are independent of clock.

NOTES:

1. J = J1 · J2 · J3
2. K = K1 · K2 · K3
3. tn = Bit time before clock pulse.
4. tn+1 = Bit time after clock pulse.

Device type 02

Truth table Each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}n$

Positive logic: Low input to clear sets Q to low level.
Clear is independent of clock.

NOTES:

1. tn = Bit time before clock pulse.
2. tn+1 = Bit time after clock pulse.

FIGURE 2. Truth table.

Device type 03

Truth table Each flip-flop		
t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
L	L	H
H	H	L

Positive logic: Low input to preset sets Q to high level.
Low input to clear sets Q to low level.
Preset and clear are independent of clock.

NOTES:

1. tn = Bit time before clock pulse.
2. tn+1 = Bit time after clock pulse.

Device type 04

Truth table Each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

Positive logic: Low input to preset sets Q to high level.
Low input to clear sets Q to low level.
Preset and clear are independent of clock.

NOTES:

1. tn = Bit time before clock pulse.
2. tn+1 = Bit time after clock pulse.

FIGURE 2. Truth table - Continued.

Device type 05

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}n$

Positive logic: Low input to preset sets Q to high level.
Preset is independent of clock.

NOTES:

1. J = (J1A · J1B) + (J2A · J2B)
2. K = (K1A · K1B) + (K2A · K2B)
3. tn = Bit time before clock pulse.
4. tn+1 = Bit time after clock pulse.

Device type 06

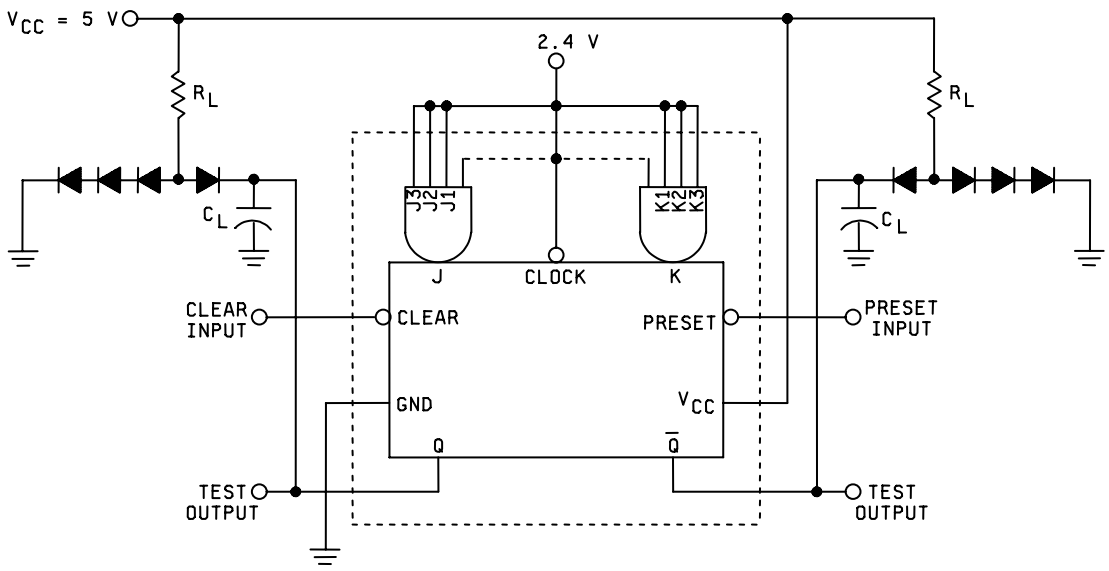
Truth table Each flip-flop		
t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}n$

Positive logic: Low input to preset sets Q to high level.
Clear is independent of clock.

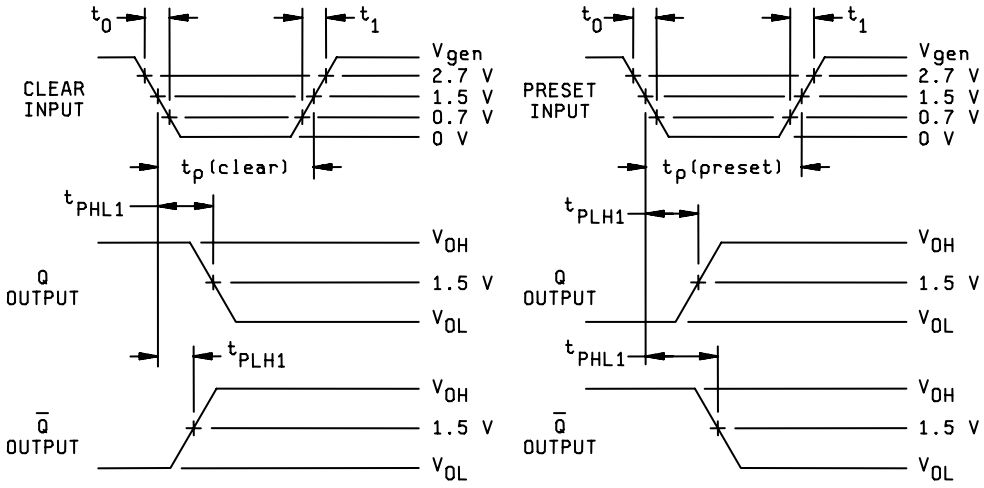
NOTES:

1. tn = Bit time before clock pulse.
2. tn+1 = Bit time after clock pulse.

FIGURE 2. Truth table - Continued.



TEST CIRCUIT

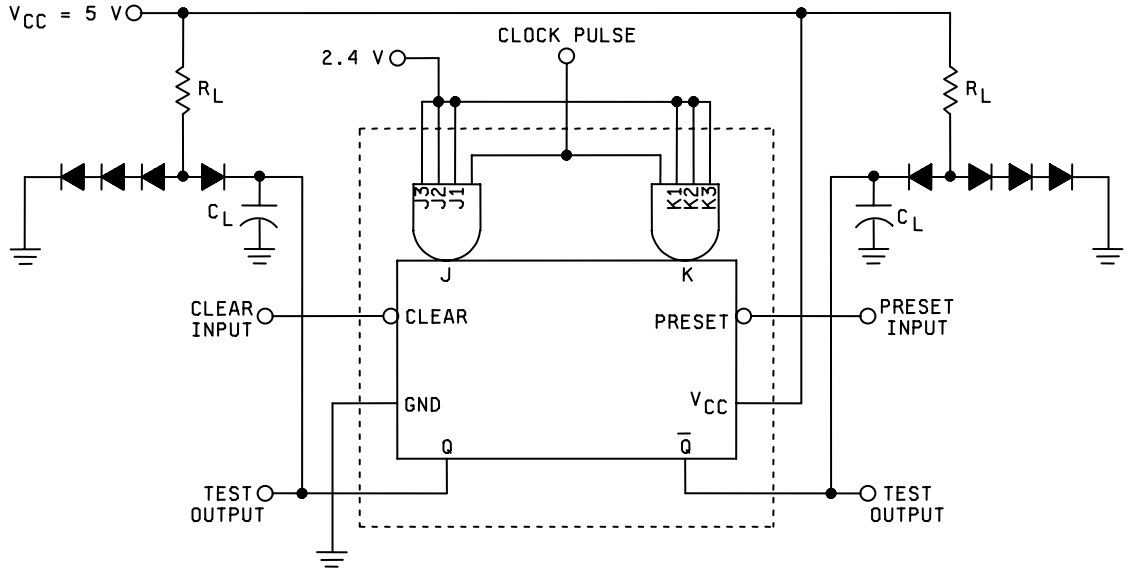


VOLTAGE WAVEFORMS

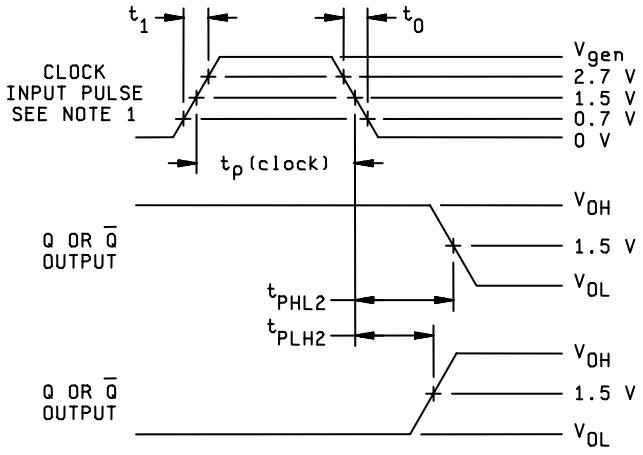
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clear) = t_P(preset) = 20 ns, PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
3. C_L = 50 pF ±5% (C_L includes probe and jig capacitance).
4. R_L = 280 Ω ±5%.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 3. Clear and preset switching test circuit and waveforms for device type 01.



TEST CIRCUIT

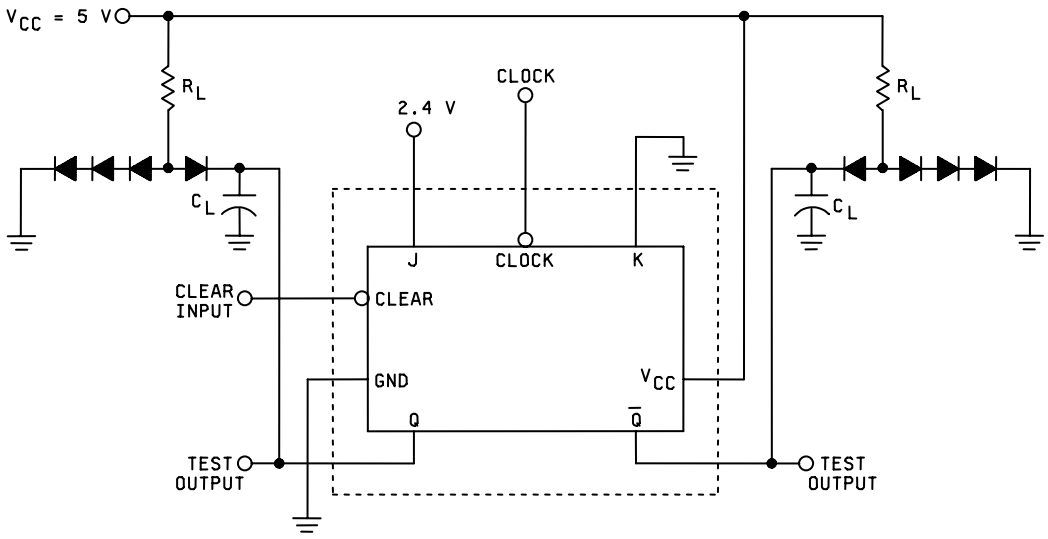


VOLTAGE WAVEFORMS

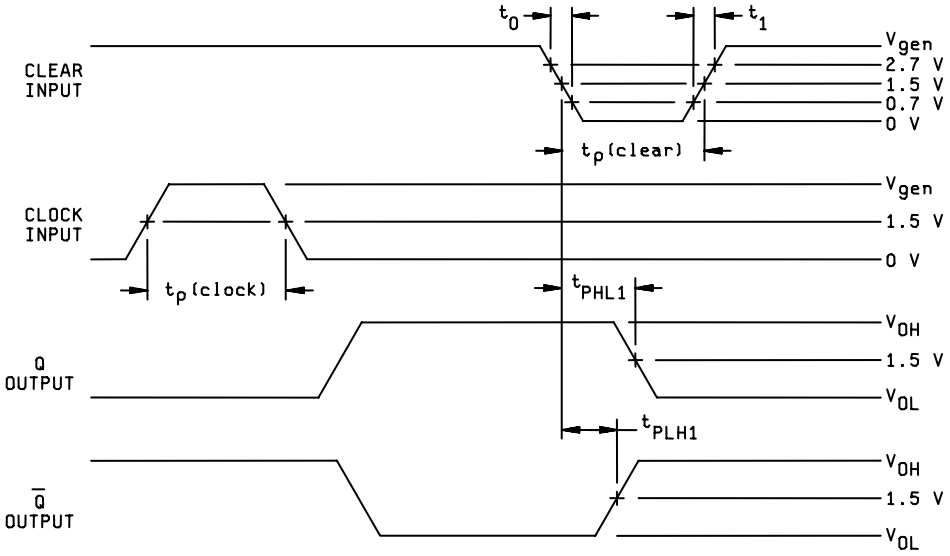
NOTES:

1. Clock input pulse characteristics for t_{PLH}, t_{PHL} (clock to output), Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clock) = 20 ns, PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are Vgen = 3 V, $t_1 = t_0 = 3$ ns, t_P(clock) = 20 ns, f = 25 MHz for subgroup 9 and f = 20 MHz for subgroups 10 and 11.
2. J = J1 · J2 · J3; and K = K1 · K2 · K3.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ±5% (C_L includes probe and jig capacitance).
5. R_L = 280 Ω ±5%.

FIGURE 4. Synchronous switching test circuit for device type 01.



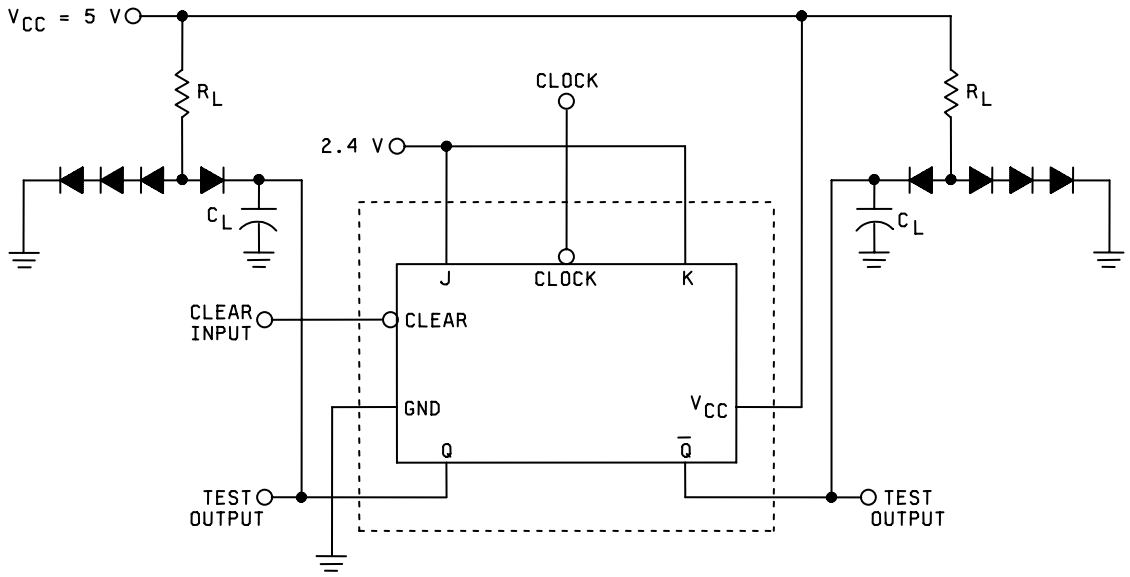
TEST CIRCUIT



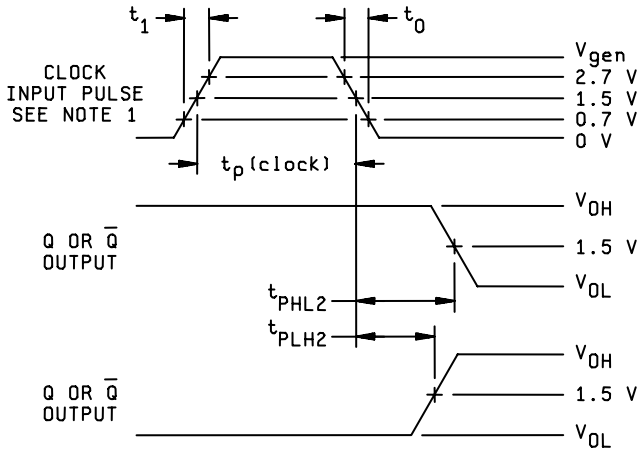
VOLTAGE WAVEFORMS

NOTES:
1. Clear inputs dominate regardless of the state of clock or J-K inputs.
2. Clear input pulse characteristics: Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clear) = 25 ns, PRR = 1 MHz.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280 Ω ±5%.
6. Clock input pulse characteristics: Vgen = 3 V, t_P(clock) ≥ 20 ns, PRR = 1 MHz.

FIGURE 5. Clear switching test circuit and waveforms for device type 02.



TEST CIRCUIT

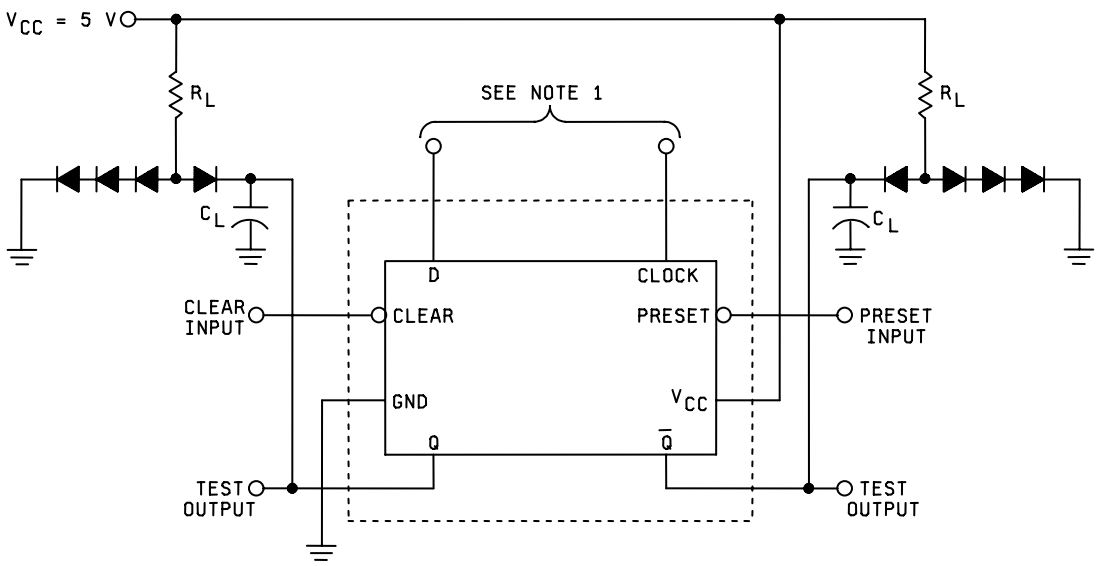


VOLTAGE WAVEFORMS

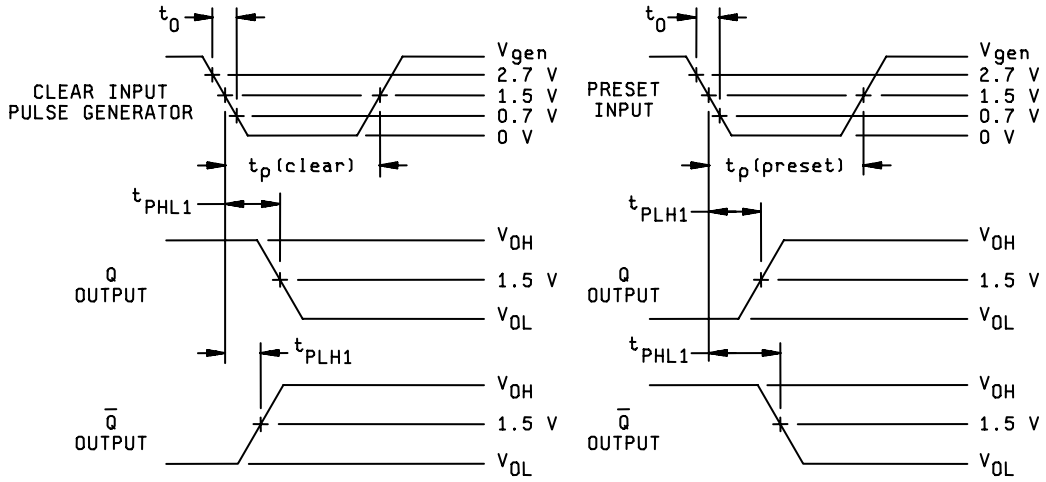
NOTES:

1. Clock input pulse characteristics for t_{PLH}, t_{PHL} (clock to output), Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clock) = 25 ns, PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are Vgen = 3 V, $t_1 = t_0 = 3$ ns, t_P(clock) = 25 ns, f = 23 MHz for subgroup 9 and f = 20 MHz for subgroups 10 and 11.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ±5% (including jig and probe capacitance).
4. R_L = 280 Ω ±5%.

FIGURE 6. Synchronous switching test circuit for device type 02.



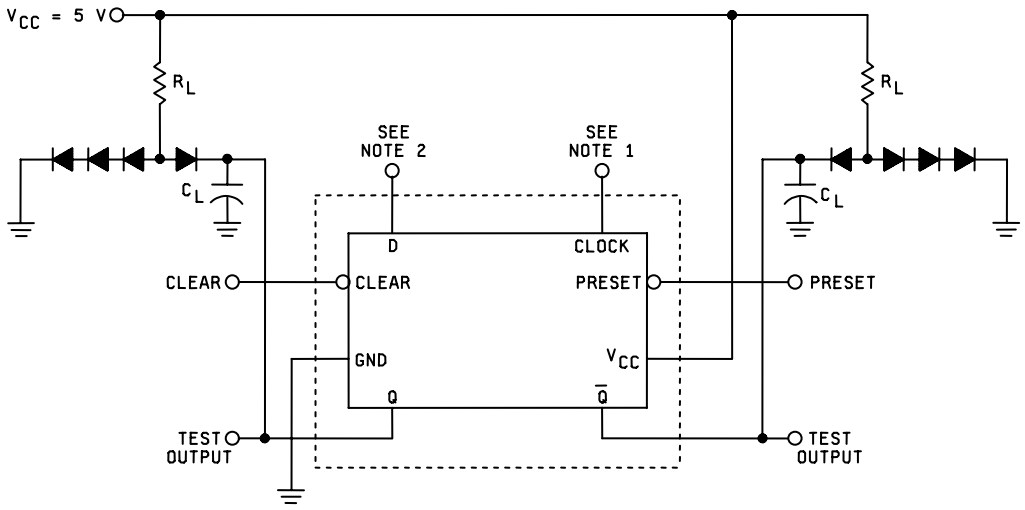
TEST CIRCUIT



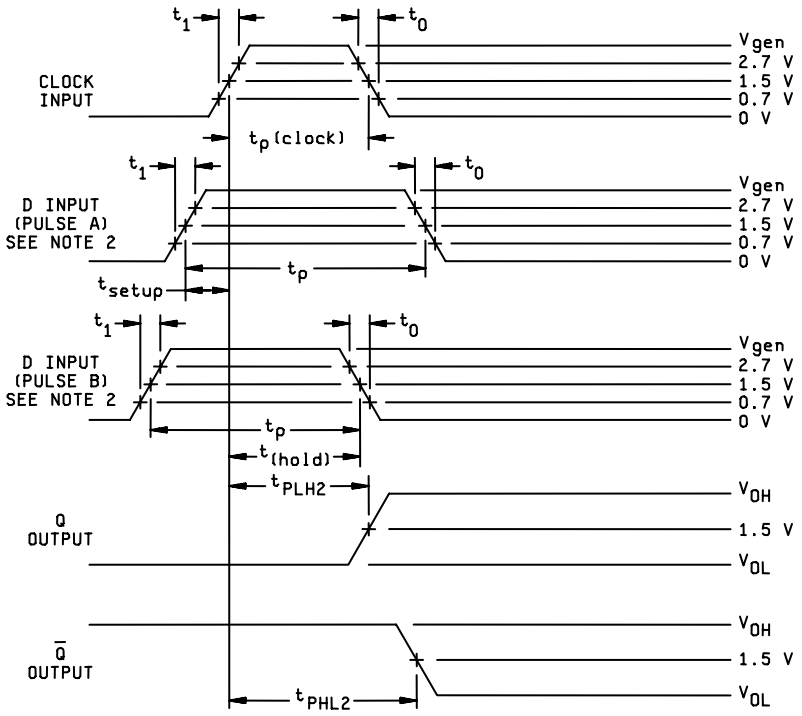
VOLTAGE WAVEFORMS

NOTES:
1. Clear or preset inputs dominate regardless of the state of clock or D inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear or preset input pulse characteristics: Vgen = 3 V, $t_0 \leq 7$ ns, t_P(clear) = t_P(preset) = 25 ns, PRR = 1 MHz.
4. C_L = 50 pF ±5% (including probe and jig capacitance).
5. R_L = 280 Ω ±5%.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 7. Clear and preset switching test circuit and waveforms for device type 03.



TEST CIRCUIT

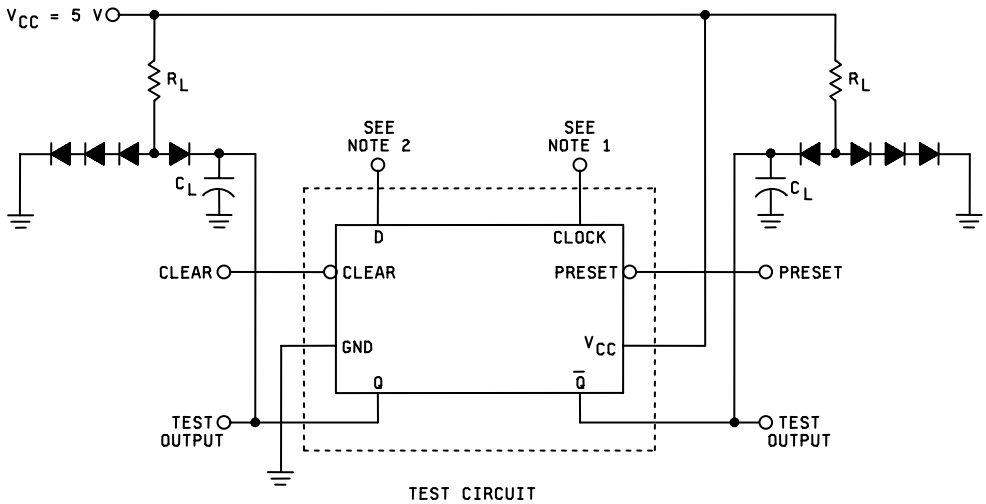


VOLTAGE WAVEFORMS

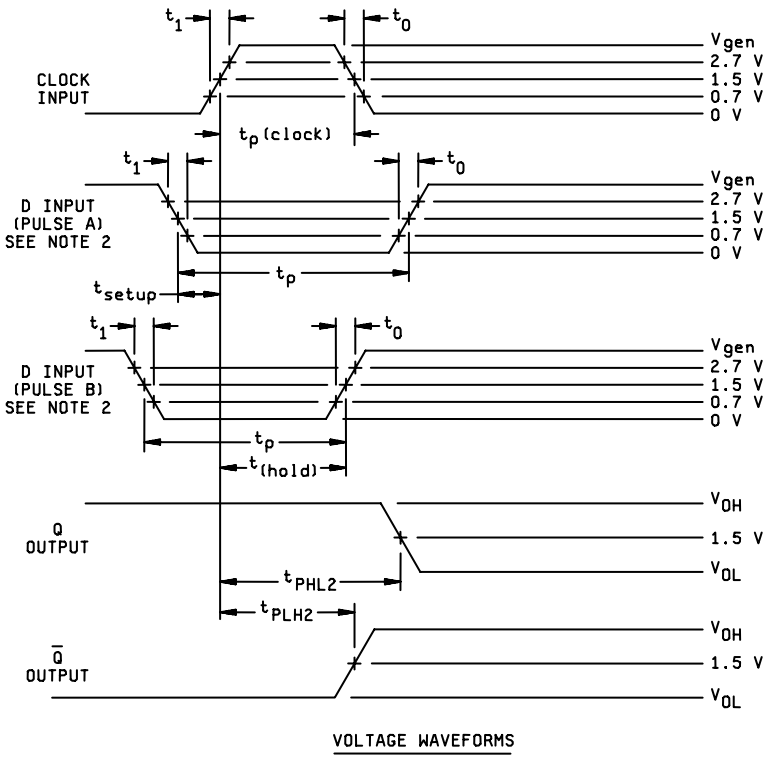
NOTES:

1. Clock input pulse has the following characteristics; Vgen = 3 V, $t_0 = t_1 \leq 7$ ns, t_P(clock) = 20 ns, PRR = 1 MHz. When testing f_{MAX} , f = 36 MHz for subgroup 9 and f = 28 MHz for subgroups 10 and 11.
2. D input (pulse A) has the following characteristics: Vgen = 3 V, $t_0 \leq 7$ns, t_{setup} = 10 ns, t_P = 60 ns, PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: Vgen = 3 V, $t_0 = t_1 \leq 7$ ns, $t_{(hold)}$ = 5 ns, t_P = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280 Ω ±5%.

FIGURE 8. Synchronous switching test circuit (high level) for device type 03.



TEST CIRCUIT

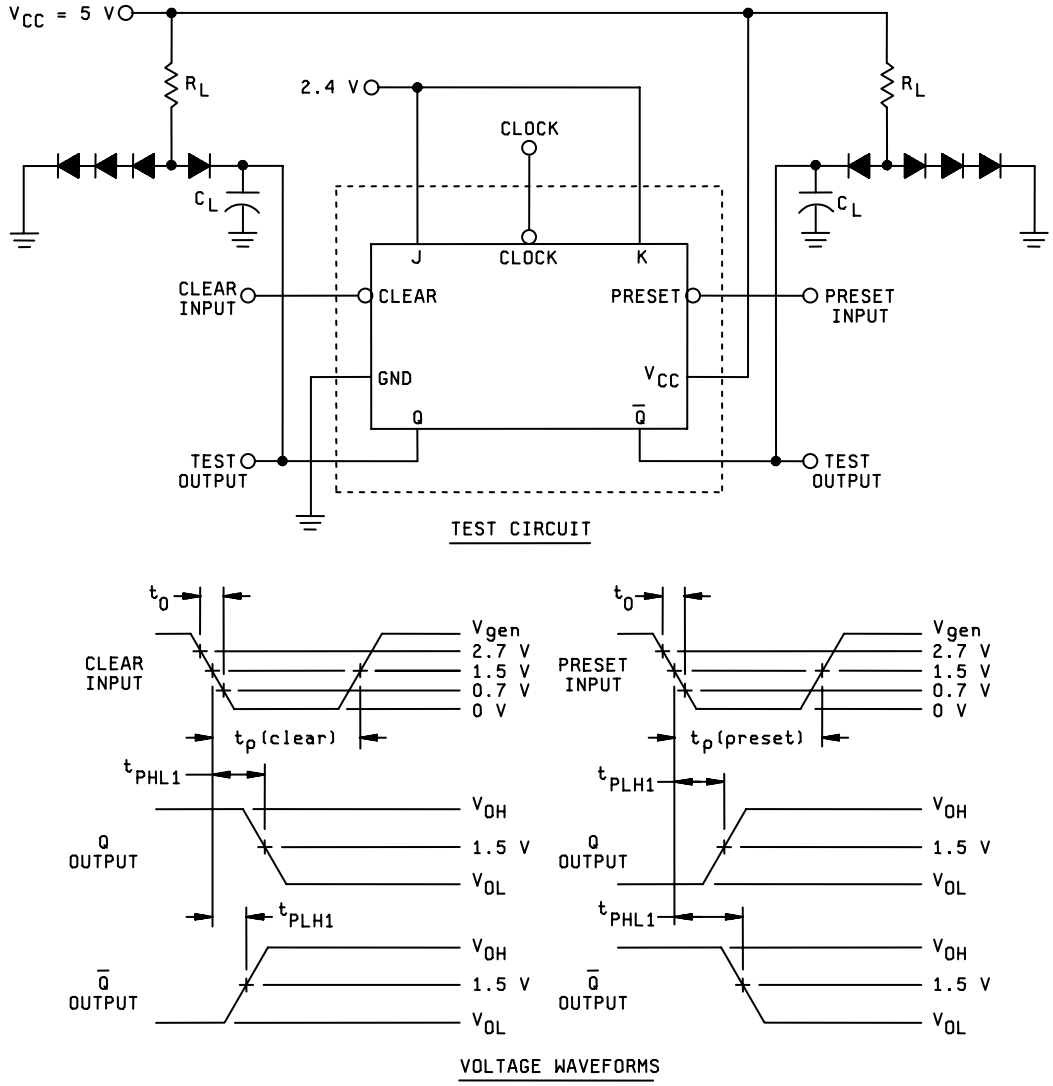


VOLTAGE WAVEFORMS

NOTES:

1. Clock input pulse has the following characteristics; Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clock) = 20 ns, and PRR = 1 MHz.
2. D input (pulse A) has the following characteristics: Vgen = 3 V, $t_0 = t_1 \leq 7$ns, t_{setup} = 15 ns, t_P = 60 ns, PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: Vgen = 3 V, $t_0 = t_1 \leq 7$ ns, $t_{(hold)}$ = 5 ns, t_P = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280 Ω ±5%.

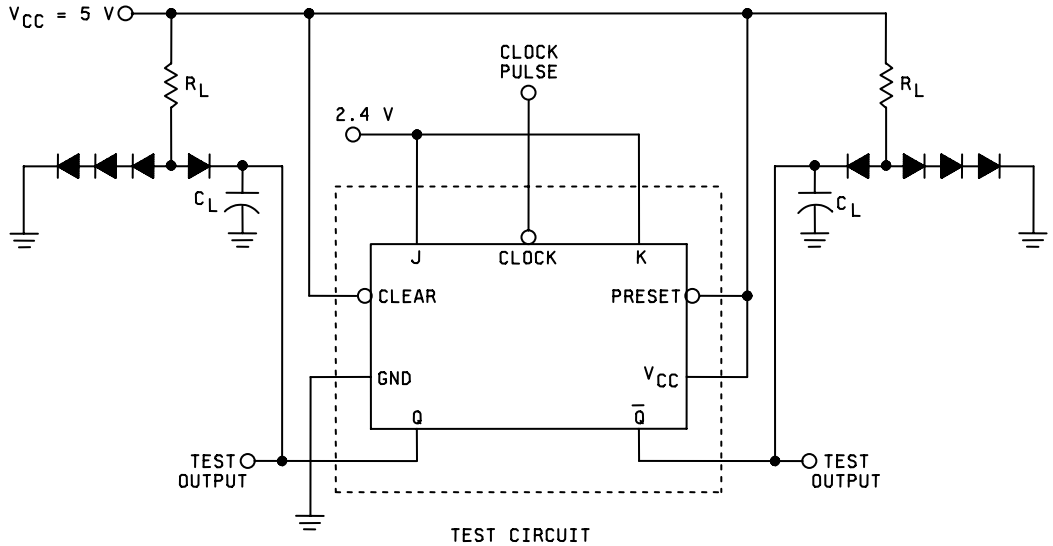
FIGURE 9. Synchronous switching test circuit (low level) for device type 03.



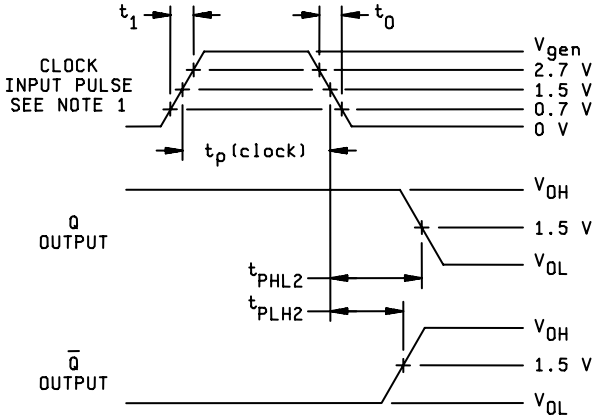
NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear or preset input pulse characteristics: Vgen = 3 V, $t_0 = t_1 \leq 7$ ns, t_P(clear) = t_P(preset) = 25 ns, PRR = 1 MHz and $Z_{OUT} \approx 50\Omega$.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280 Ω ±5%.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 10. Clear and preset switching test circuit and waveforms for device type 04.



TEST CIRCUIT

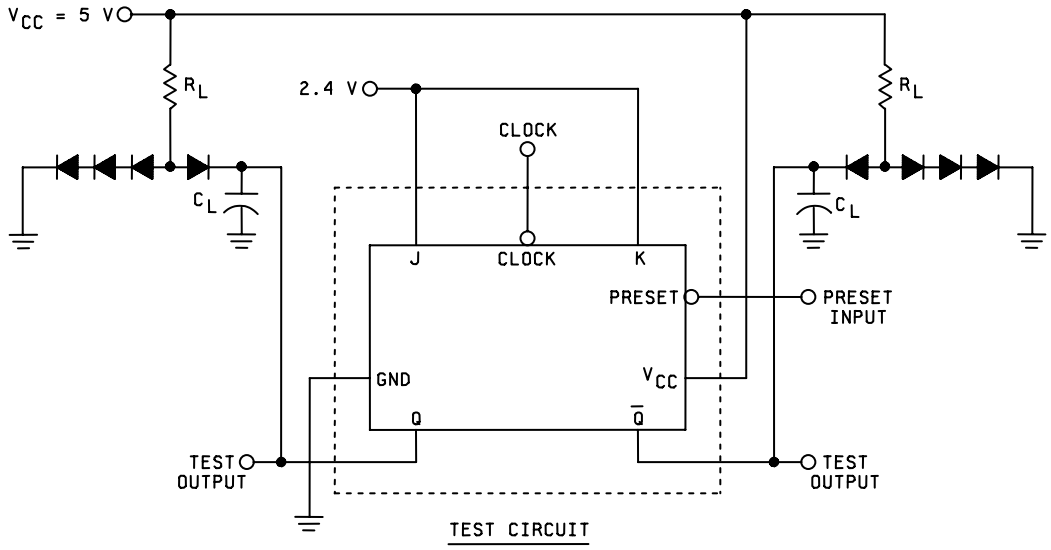


VOLTAGE WAVEFORMS

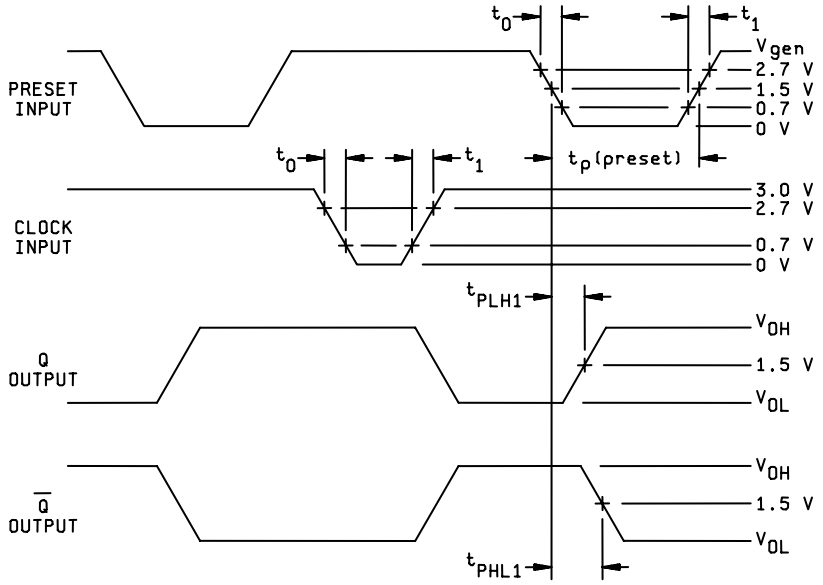
NOTES:

1. Clock input pulse characteristics for t_{PLH}, t_{PHL} (clock to output), Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clock) = 25 ns, PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are Vgen = 3 V, $t_1 = t_0 = 3$ ns, t_P(clock) = 25 ns, f = 23 MHz for subgroup 9 and f = 20 MHz for subgroups 10 and 11.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ±5% (including jig and probe capacitance).
4. R_L = 280 Ω ±5%.

FIGURE 11. Synchronous switching test circuit for device type 04.



TEST CIRCUIT

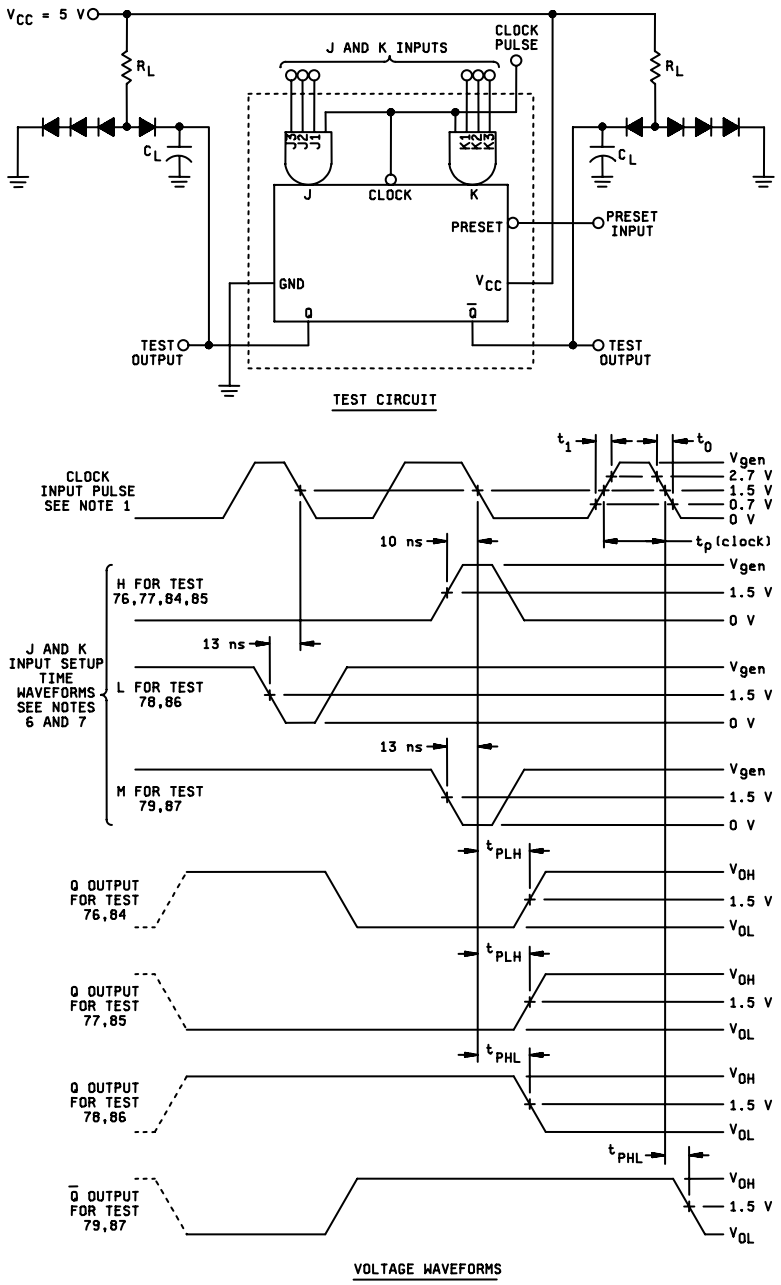


VOLTAGE WAVEFORMS

NOTES:

1. Preset inputs dominate regardless of the state of clock or J-K inputs.
2. Preset input pulse characteristics: Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(preset) = 16 ns, PRR = 1 MHz and $Z_{OUT} \approx 50\ \Omega$.
3. Clock input pulse characteristics: Vgen = 3 V, $t_0 = t_1 = 3$ ns, PRR = 1 MHz, $Z_{OUT} \approx 50\ \Omega$, and t_P(clock) = 20 ns.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280 Ω ±5%.
6. All diodes are 1N3064, or equivalent.

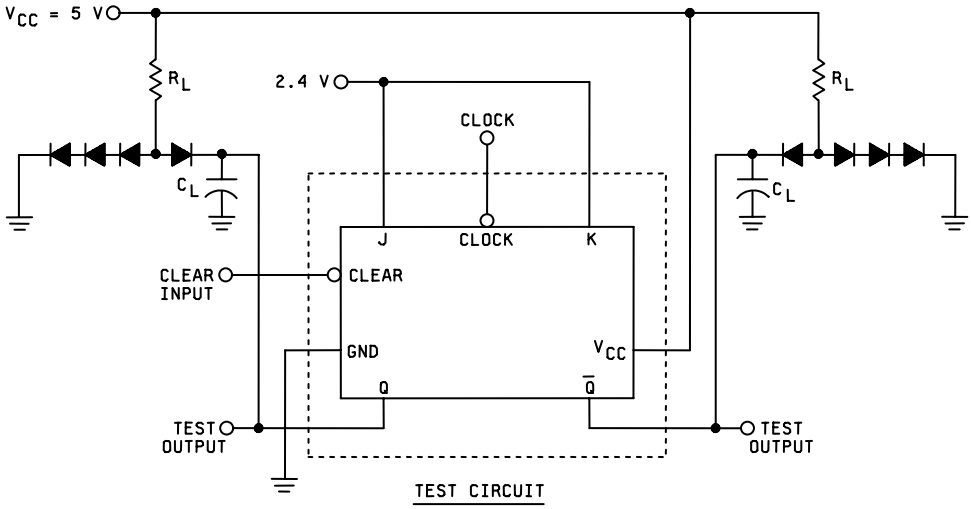
FIGURE 12. Preset switching test circuit and waveforms for device type 05.



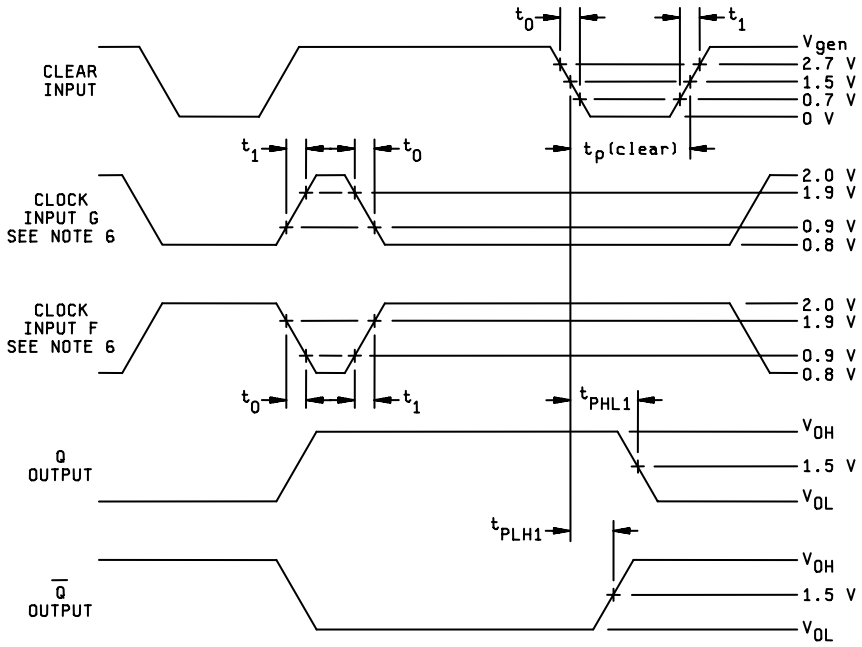
NOTES:

1. Clock input pulse characteristics for t_{PLH}, t_{PHL} (clock to output), Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clock) = 20 ns, PRR = 1 MHz. When testing f_{MAX} the clock input characteristics are Vgen = 3 V, $t_1 = t_0 = 3$ ns, t_P(clock) = 10 ns, f = 36 MHz for subgroup 9 and f = 30 MHz for subgroups 10 and 11. All J and K inputs are at 2.4 V.
2. J = (J1A · J1B) + (J2A · J2B) and K = (K1A · K1B) + (K2A · K2B).
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280 Ω ±5%.
6. J and K input characteristics for t_{PHL} and t_{PLH} are Vgen = 3 V, rise and fall times 10 ns maximum, and PW = 20 ns. See table III for which t_{setup} to use.
7. For test 84, 85, 86, and 87 (high low temperature) the t_{setup} value shown above should be increased from 10 and 13 ns to 15 and 20 ns respectively.

FIGURE 13. Synchronous switching test circuit for device type 05.



TEST CIRCUIT

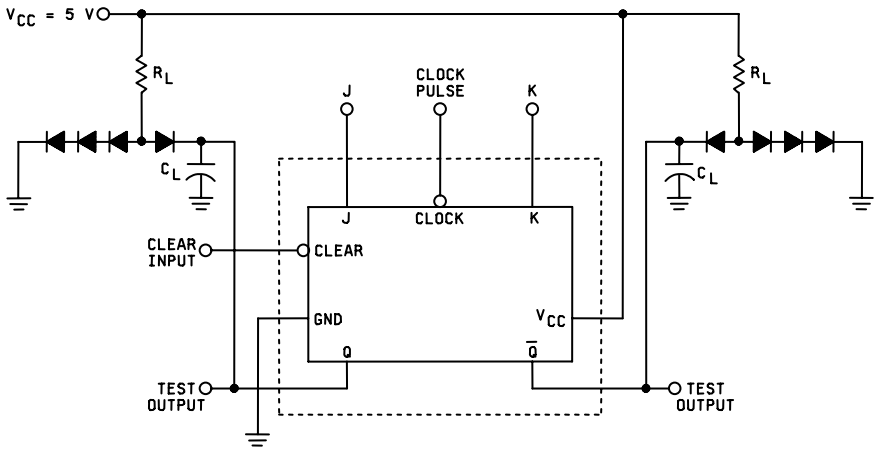


VOLTAGE WAVEFORMS

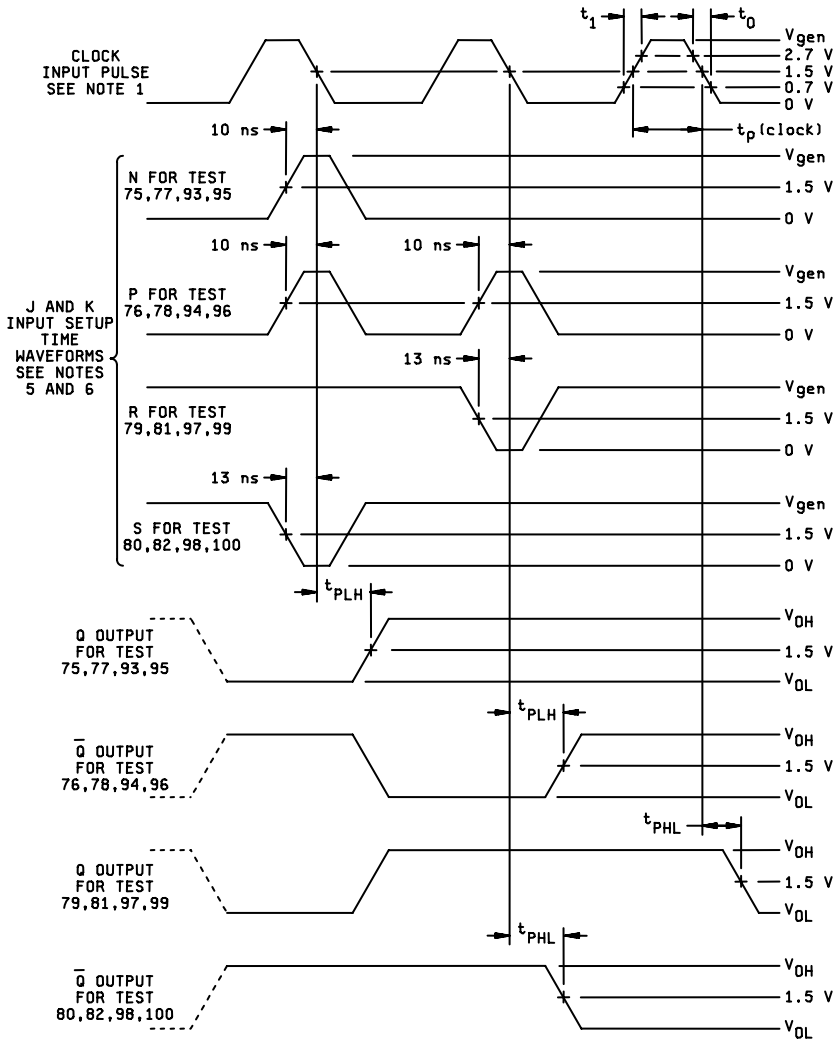
NOTES:

1. Clear inputs dominate regardless of the state of clock or J-K inputs.
2. Clear input pulse characteristics: Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clear) = 16 ns, PRR = 1 MHz and $Z_{OUT} \approx 50\ \Omega$.
3. Clock input pulse characteristics: Vgen = 3 V, $t_0 = t_1 = 3$ ns, PRR = 1 MHz and t_P(clock) = 20 ns minimum.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280 Ω ±5%.
6. Apply clock pulse F or G as required by table III.

FIGURE 14. Clear switching test circuit and waveforms for device type 06.



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 15. Synchronous switching test circuit for device type 06.

NOTES:

1. Clock input pulse characteristics for t_{PLH}, t_{PHL} (clock to output), Vgen = 3 V, $t_0 = t_1 = 7$ ns, t_P(clock) = 20 ns, PRR = 1 MHz. When testing f_{MAX} the clock input characteristics are Vgen = 3 V, $t_1 = t_0 = 3$ ns, t_P(clock) = 10 ns, f = 36 MHz for subgroup 9 and f = 30 MHz for subgroups 10 and 11. All J and K inputs are at 2.4 V.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ±5% (including jig and probe capacitance).
4. R_L = 280 Ω ±5%.
5. J and K input characteristics for t_{PHL} and t_{PLH} are Vgen = 3 V, rise and fall times 10 ns maximum, and PW = 20 ns. See table III for which t_{setup} to use.
6. For test 93 through 100 (high low temperature) the t_{setup} value shown above should be increased from 10 and 13 ns to 15 and 20 ns respectively.

FIGURE 15. Synchronous switching test circuit for device type 06 - Continued.

TABLE III. Group A inspection for device type 01. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max	
			Test no.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3				
1 T_C=25°C	V_{OH}	3006	1	0.8 V	A		4.5 V			2.0 V	2.0 V	2.0 V		GND	-0.5 mA	0.8 V	0.8 V	Q	2.4		V
			2	2.0 V	A		"			0.8 V	0.8 V	0.8 V	-0.5 mA	"		2.0 V	2.0 V	$\overline{Q}$	"		"
			3			0.8 V	"	2.0 V						"	-0.5 mA			Q	"		"
			4			2.0 V	"	0.8 V					-0.5 mA	"				$\overline{Q}$	"		"
	V_{OL}	3007	5	2.0 V	A		"			0.8 V	0.8 V	0.8 V		"	20 mA	2.0 V	2.0 V	Q		0.4	"
			6	0.8 V	A		"			2.0 V	2.0 V	2.0 V	20 mA	"		0.8 V	0.8 V	$\overline{Q}$		"	"
			7			0.8 V	"	2.0 V					20 mA	"				Q		"	"
			8			2.0 V	"	0.8 V						"	20 mA			$\overline{Q}$		"	"
	V_{IC}		9	-12 mA			"							"		-12 mA		K1		-1.5	"
			10				"							"			-12 mA	K2		"	"
			11				"							"				K3		"	"
			12				"			-12 mA				"				J1		"	"
			13				"				-12 mA			"				J2		"	"
			14				"					-12 mA		"				J3		"	"
			15				"	-12 mA						"				Clear		"	"
			16			-12 mA	"							"				Preset		"	"
			17		-12 mA		"							"				Clock		"	"
	I_{IL1}	3009	18	GND	4.5 V		5.5 V	B		0.4 V	4.5 V	4.5 V		"		GND	GND	J1	-1.0	-2.0	mA
			19	"	"		"	"		4.5 V	0.4 V	4.5 V		"		"	"	J2	"	"	"
			20	"	"		"	"		4.5 V	4.5 V	0.4 V		"		"	"	J3	"	"	"
			21	0.4 V	"	B	"			GND	GND	GND		"		4.5 V	4.5 V	K1	"	"	"
			22	4.5 V	"	"	"			"	"	"		"		0.4 V	4.5 V	K2	"	"	"
			23	"	"	"	"			"	"	"		"		4.5 V	0.4 V	K3	"	"	"
			24	"	0.4 V	"	"			4.5 V	4.5 V	4.5 V		"		"	4.5 V	Clock	"	"	"
			25	"	0.4 V		"	B		"	"	"		"		"	"	Clock	"	"	"
	I_{IL2}		26	"	4.5 V	0.4 V	"			"	"	"		"		"	"	Preset	-2.0	-4.0	"
			27	"	4.5 V		"	0.4 V		"	"	"		"		"	"	Clear	-2.0	-4.0	"
	I_{IH1}	3010	28		GND		"	GND		2.4 V	GND	GND		"				J1		50	µA
			29		"		"	"		GND	2.4 V	GND		"				J2		"	"
			30		"		"	"		GND	GND	2.4 V		"				J3		"	"
			31	2.4 V	"	GND	"							"		GND	GND	K1		"	"
			32	GND	"	"	"							"		2.4 V	GND	K2		"	"
			33	GND	"	"	"							"		GND	2.4 V	K3		"	"
	I_{IH2}		34		"		"	GND		5.5 V	GND	GND		"				J1		100	"
			35		"		"	"		GND	5.5 V	GND		"				J2		"	"
			36		"		"	"		GND	GND	5.5 V		"				J3		"	"
			37	5.5 V	"	GND	"							"		GND	GND	K1		"	"
			38	GND	"	"	"							"		5.5 V	GND	K2		"	"
			39	GND	"	"	"							"		GND	5.5 V	K3		"	"
	I_{IH3}		40		"		"	2.4 V		GND	GND	GND		"				Clear		"	"
			41	GND	"	2.4 V	"							"		GND	GND	Preset		"	"
	I_{IH4}		42	GND	"	5.5 V	"							"		GND	GND	Preset		200	"
			43		"		"	5.5 V		GND	GND	GND		"				Clear		200	"
	I_{IH5}		44	GND	2.4 V		"	GND		"	"	"		"		GND	GND	Clock		100	"
			45	"	2.4 V	GND	"			"	"	"		"		"	"	"		100	"
	I_{IH6}		46	"	5.5 V		"	GND		"	"	"		"		"	"	"		200	"
			47	"	5.5 V	GND	"			"	"	"		"		"	"	"		200	"

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max	
			Test no.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3				
1 T_C=+25°C	I_{OS}	3011	48	4.5 V	GND	GND	5.5 V			4.5 V	4.5 V	4.5 V		GND	GND	4.5 V	4.5 V	Q	-40	-100	mA
			49	4.5 V	"		"	GND		4.5 V	4.5 V	4.5 V	GND	"		4.5 V	4.5 V	$\overline{Q}$	-40	-100	"
	I_{CC}	3005	50	GND	"	GND	"			GND	GND	GND		"		GND	GND	V_{CC}		25	"
			51	GND	"		"	GND		GND	GND	GND		"		GND	GND	V_{CC}		25	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C=+25°C 2/ 3/			52	B	A	B	4.5 V	B	B	B	B	B	H	GND	H	B	B	All outputs	H or L as shown 4/		
			53	"	"	B	"	A	"	"	"	"	L	"	H	"	"				
			54	"	"	A	"	B	"	"	"	"	H	"	L	"	"				
			55	"	B	"	"	A	"	"	"	"	"	"	"	"	"				
			56	A	B	"	"	"	"	A	A	"	"	"	"	A	A				
			57	"	A	"	"	"	"	"	"	"	"	"	"	"	"				
			58	"	B	"	"	"	"	"	"	"	"	"	"	"	"				
			59	"	B	"	"	"	"	"	B	A	"	"	"	"	"				
			60	"	A	"	"	"	"	"	"	"	"	"	"	"	"				
			61	"	B	"	"	"	"	"	"	"	"	"	"	"	"				
			62	"	B	"	"	"	"	B	A	"	"	"	"	"	"				
			63	"	A	"	"	"	"	"	"	"	"	"	"	"	"				
			64	"	B	"	"	"	"	"	"	"	"	"	"	"	"				
			65	"	B	"	"	"	"	A	"	"	"	"	"	"	"				
			66	"	A	"	"	"	"	"	"	"	L	"	H	"	"				
			67	"	B	"	"	"	"	"	"	"	"	"	"	"	B				
			68	"	B	"	"	"	"	"	"	"	"	"	"	"	"				
			69	"	A	"	"	"	"	"	"	"	"	"	"	"	"				
			70	"	B	"	"	"	"	"	"	"	"	"	"	B	A				
			71	"	B	"	"	"	"	"	"	"	"	"	"	"	"				
			72	"	A	"	"	"	"	"	"	"	"	"	"	"	"				
			73	"	B	"	"	"	"	"	"	"	"	"	"	A	"				
			74	B	B	"	"	"	"	"	"	"	"	"	"	"	"				
			75	"	A	"	"	"	"	"	"	"	"	"	"	"	"				
			76	"	B	"	"	"	"	"	"	"	"	"	"	"	"				
			77	A	B	"	"	"	"	"	"	"	"	"	"	"	"				
			78	"	A	"	"	"	"	"	"	"	"	"	"	"	"				
			79	"	B	"	"	"	"	"	"	"	"	"	L	"	"				
8 2/ 3/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																				
9 T_C=+25°C	f_{MAX} 5/	(Fig. 4)	80	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	2.4 V		GND	OUT	2.4 V	2.4 V	Q	25		MHz
			81	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	$\overline{Q}$	25		MHz
	t_{PLH1}	3003 (Fig. 3)	82	"	2.4 V	J	"	IN		"	"	"	OUT	"		"	"	Clear to $\overline{Q}$	2	15	ns
			83	"	"	IN	"	J		"	"	"		"	OUT	"	"	Preset to Q	"	15	"
	t_{PHL1}		84	"	"	J	"	IN		"	"	"		"	OUT	"	"	Clear to $\overline{Q}$	"	26	"
			85	"	"	IN	"	J		"	"	"	OUT	"		"	"	Preset to Q	"	26	"
	t_{PLH2}	3003 (Fig. 3)	86	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	23	"
			87	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	23	"
	t_{PHL2}		88	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to $\overline{Q}$	"	29	"
			89	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to Q	"	29	"

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max	
			Test no.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3				
10 T_C=+125°C	f_{MAX}	(Fig. 4)	90 5/	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	2.4 V		GND	OUT	2.4 V	2.4 V	$\underline{Q}$	20		MHz
			91 5/	"	"	"	"	"		"	"	"	OUT	"		"	"	Q	20		MHz
	t_{PLH1}	3003 (Fig. 3)	92	"	2.4 V	J	"	IN		"	"	"	OUT	"		"	"	Clear to Q	2	20	ns
			93	"	"	IN	"	J		"	"	"		"	OUT	"	"	Preset to Q	"	20	"
	t_{PHL1}		94	"	"	J	"	IN		"	"	"		"	OUT	"	"	Clear to $\underline{Q}$	"	31	"
			95	"	"	IN	"	J		"	"	"	OUT	"		"	"	Preset to Q	"	31	"
	t_{PLH2}	(Fig. 3)	96	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	28	"
			97	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	28	"
	t_{PHL2}		98	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	37	"
			99	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	37	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C= -55°C.																				

A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
J = Input pulse $t_p \geq 100$ ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H > 2.0 V, or L ≤ 0.8 V, or open).
2/ Tests shall be performed in sequence.
3/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
4/ Output voltages shall be either: H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.
5/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	Q1	$\overline{Q1}$	J1				
1 T_C=+25°C	V_{OH}	3006	1	A		0.8 V	4.5 V							GND	-0.5 mA		2.0 V	$\underline{Q}1$	2.4		V
			2	A		2.0 V	"							"		-0.5 mA	0.8 V	$\underline{Q}1$	"		"
			3		0.8 V		"							"		-0.5 mA		Q1	"		"
			4				"	A		2.0 V		-0.5 mA	0.8 V	"				$\underline{Q}2$	"		"
			5				"	A		0.8 V	-0.5 mA		2.0 V	"				$\underline{Q}2$	"		"
			6				"		0.8 V		-0.5 mA			"				Q2	"		"
	V_{OL}	3007	7	A		2.0 V	"							"	20 mA		0.8 V	$\underline{Q}1$		0.4	"
			8	A		0.8 V	"							"		20 mA	2.0 V	Q1		"	"
			9		0.8 V		"							"	20 mA			Q1		"	"
			10				"	A		0.8 V		20 mA	2.0 V	"				$\underline{Q}2$		"	"
			11				"	A		2.0 V	20 mA		0.8 V	"				Q2		"	"
			12				"		0.8 V			20 mA		"				Q2		"	"
	V_{IC}		13				"							"				J1		-1.5	"
			14				"			-12 mA				"				J2		"	"
			15			-12 mA	"							"				K1		"	"
			16				"						-12 mA	"				K2		"	"
			17		-12 mA		"							"				Clear 1		"	"
			18	-12 mA			"							"				Clock 1		"	"
			19				"		-12 mA					"				Clear 2		"	"
			20				"	-12 mA						"				Clock 2		"	"
	I_{IL1}	3009	21	2/	4.5 V		5.5 V							"			0.4 V	J1	-1.0	-2.0	mA
			22	2/	4.5 V	0.4 V	"							"				K1	"	"	"
			23				"	2/	4.5 V	0.4 V				"				J2	"	"	"
			24				"	2/	4.5 V				0.4 V	"				K2	"	"	"
			25	0.4 V	B	4.5 V	"							"			4.5 V	Clock 1	"	"	"
			26				"		B	4.5 V			4.5 V	"				Clock 2	"	"	"
	I_{IL2}		27	4.5 V	0.4 V		"							"			4.5 V	Clear 1	-2.0	-4.0	"
			28				"	4.5 V	0.4 V	4.5 V				"				Clear 2	-2.0	-4.0	"
	I_{IH1}	3010	29	GND	GND		"							"			2.4 V	J1		50	µA
			30	GND	B	2.4 V	"							"				K1		"	"
			31				"	GND	GND	2.4 V				"				J2		"	"
			32				"	GND	B				2.4 V	"				K2		"	"
	I_{IH2}		33	GND	GND		"							"			5.5 V	J1		100	"
			34	GND	B	5.5 V	"							"				K1		"	"
			35				"	GND	GND	5.5 V				"				J2		"	"
			36				"	GND	B				5.5 V	"				K2		"	"
	I_{IH3}		37	GND	E		"							"			GND	Clear 1		100	"
			38				"	GND	E	GND				"				Clear 2		100	"
	I_{IH4}		39	GND	F		"							"			GND	Clear 1		200	"
			40				"	GND	F	GND				"				Clear 2		200	"
	I_{IH5}		41	2.4 V	GND	GND	"							"			GND	Clock 1		100	"
			42				"	2.4 V	GND	GND			GND	"				Clock 2		100	"
	I_{IH6}		43	5.5 V	GND	GND	"							"			GND	Clock 1		200	"
			44				"	5.5 V	GND	GND			GND	"				Clock 2		200	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}2$	Q2	K2	GND	Q1	$\overline{Q}1$	J1				
1 T_C=+25°C	I_{OS}	3011	45	2.4 V	GND	2.4 V	5.5 V							GND		GND	2.4 V	$\overline{Q}1$	-40	-100	mA
			46*		4.5 V		"							"	GND	GND		Q1	"	"	"
			47*				"		4.5 V		GND	GND		"				Q2	"	"	"
			48				"	2.4 V	GND	2.4 V	GND		2.4 V	"				Q2	"	"	"
	I_{CC}	3005	49	D	4.5 V	GND	"	D	4.5 V	4.5 V			GND	"			4.5 V	V_{CC}		50	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C=+25°C 3/ 4/			50	A	B	B	4.5 V	A	B	B	H	L	B	GND	L	H	B	All outputs	H or L as shown 5/		
			51	A	A	"	"	A	A	"	"	"	"	"	"	"	"	"			
			52	"	"	"	"	B	"	"	"	"	"	"	"	"	"	"			
			53	"	"	A	"	B	"	A	"	"	A	"	"	"	A	"			
			54	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"			
			55	B	"	"	"	B	"	"	L	H	"	"	H	L	"	"			
			56	A	"	"	"	A	"	"	L	H	"	"	H	L	"	"			
			57	"	B	"	"	"	B	"	H	L	"	"	L	H	"	"			
			58	"	A	"	"	"	A	"	H	L	"	"	L	H	"	"			
			59	B	A	"	"	B	A	"	L	H	"	"	H	L	"	"			
			60	"	B	"	"	"	B	"	H	L	"	"	L	H	"	"			
			61	"	A	"	"	"	A	"	"	"	"	"	"	"	"	"			
			62	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"			
			63	B	"	"	"	B	"	"	L	H	"	"	H	L	"	"			
			64	B	"	B	"	B	"	B	"	"	B	"	"	"	B	"			
			65	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"			
			66	B	"	"	"	B	"	"	"	"	"	"	"	"	"	"			
			67	B	"	A	"	B	"	A	"	"	A	"	"	"	A	"			
			68	A	"	"	"	A	"	"	"	"	"	"	"	"	"	"			
			69	B	"	"	"	B	"	"	H	L	"	"	"	"	"	"			
8 3/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C=-+125°C and -55°C.																				
9 T_C=+25°C	f_{MAX} 6/	(Fig. 6)	70	IN		2.4 V	5.0 V							GND	OUT		2.4 V	Q1	23		MHz
			71	IN		2.4 V	"							"		OUT	2.4 V	Q1	"		"
			72				"	IN		2.4 V		OUT	2.4 V	"				Q2	"		"
			73				"	IN		2.4 V	OUT		2.4 V	"				Q2	"		"
	t_{PLH1}	3003 (Fig. 5)	74	IN	IN	GND	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}1$	2	20	ns
			75				"	IN	IN	2.4 V	OUT		GND	"				Clear 2 to Q2	"	20	"
	t_{PHL1}		76	IN	IN	GND	"							"	OUT		2.4 V	Clear 1 to Q1	"	27	"
			77				"	IN	IN	2.4 V		OUT	GND	"				Clear 2 to Q2	"	27	"
	t_{PLH2}	3003 (Fig. 6)	78	IN		2.4 V	"							"	OUT		2.4 V	Clock 1 to Q1	"	26	"
			79	IN		2.4 V	"							"		OUT	2.4 V	Clock 1 to Q1	"	"	"
			80				"	IN		2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			81				"	IN		2.4 V	OUT		2.4 V	"				Clock 2 to Q2	"	"	"
	t_{PHL2}		82	IN		2.4 V	"							"	OUT		2.4 V	Clock 1 to Q1	"	34	"
			83	IN		2.4 V	"							"		OUT	2.4 V	Clock 1 to Q1	"	"	"
			84				"	IN		2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			85				"	IN		2.4 V	OUT		2.4 V	"				Clock 2 to Q2	"	"	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}2$	Q2	K2	GND	Q1	$\overline{Q}1$	J1				
10 T_C=+125°C	f_{MAX}	(Fig. 6)	86 87 88 89	IN IN		2.4 V 2.4 V	5.0 V “ “ “	 IN IN		 2.4 V 2.4 V	 OUT	 OUT	 2.4 V 2.4 V	GND “ “ “	OUT	 OUT	2.4 V 2.4 V	Q1 Q1 Q2 Q2	20 “ “ “		MHz “ “ “
	t_{PLH1}	3003 (Fig. 5)	90 91	IN	IN	GND	“ “	 IN	 IN	 2.4 V	 OUT		 GND	“ “		OUT	2.4 V	Clear 1 to Q1 Clear 2 to Q2	2 “	20 20	ns “
	t_{PHL1}		92 93	IN	IN	GND	“ “	 IN	 IN	 2.4 V		 OUT	 GND	“ “	OUT		2.4 V	Clear 1 to Q1 Clear 2 to Q2	“ “	31 31	“ “
	t_{PLH2}	3003 (Fig. 6)	94 95 96 97	IN IN		2.4 V 2.4 V	“ “ “ “	 IN IN		 2.4 V 2.4 V	 OUT	 OUT	 2.4 V 2.4 V	“ “ “ “	OUT	 OUT	2.4 V 2.4 V	Clock 1 to Q1 Clock 1 to Q1 Clock 2 to Q2 Clock 2 to Q2	“ “ “ “	35 “ “ “	“ “ “ “
	t_{PHL2}		98 99 100 101	IN IN		2.4 V 2.4 V	“ “ “ “	 IN IN		 2.4 V 2.4 V	 OUT	 OUT	 2.4 V 2.4 V	“ “ “ “	OUT	 OUT	2.4 V 2.4 V	Clock 1 to Q1 Clock 1 to Q1 Clock 2 to Q2 Clock 2 to Q2	“ “ “ “	42 “ “ “	“ “ “ “
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C.																				

A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
D = Momentary 4.5 V, then GND.
E = Momentary GND, then 2.4 V.
F = Momentary GND, then 5.5 V.
* = Test time limit ≥ 100 ns.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input shall be one normal clock pulse, then 4.5 V.
3/ Tests shall be performed in sequence.
4/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
5/ Output voltages shall be either: H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator, or H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.
6/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 03. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max	
			Test no.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q2}$	GND	$\overline{Q1}$	Q1	Preset 1				
1 T_C=+25°C	V_{OH}	3006	1	A	2.0 V		4.5 V							GND		-1mA		$\overline{Q1}$	2.4		V
			2	A	0.8 V		"							"	-1mA		2.0 V	$\overline{Q1}$	"		"
			3			0.8 V	"							"	-1mA		0.8 V	Q1	"		"
			4			2.0 V	"							"		-1mA		Q1	"		"
			5				"		2.0 V	A		-1mA		"				Q2	"		"
			6				"		0.8 V	A			-1mA	"				$\overline{Q2}$	"		"
			7				"	0.8 V			2.0 V		-1mA	"				$\overline{Q2}$	"		"
			8				"	2.0 V			0.8 V	-1mA		"				$\overline{Q2}$	"		"
	V_{OL}	3007	9	A	2.0 V		"							"	20 mA			$\overline{Q1}$		0.4	"
			10	A	0.8 V		"							"		20 mA		Q1		"	"
			11			0.8 V	"							"		20 mA	2.0 V	$\overline{Q1}$		"	"
			12			2.0 V	"							"	20 mA		0.8 V	Q1		"	"
			13				"		2.0 V	A			20 mA	"				Q2		"	"
			14				"		0.8 V	A		20 mA		"				Q2		"	"
			15				"	0.8 V			2.0 V	20 mA		"				$\overline{Q2}$		"	"
			16				"	2.0 V			0.8 V		20 mA	"				$\overline{Q2}$		"	"
	V_{IC}		17		-12 mA		"							"				D1		-1.5	"
			18	-12 mA			"							"				Clock 1		"	"
			19			-12 mA	"							"				Clear 1		"	"
			20				"							"			-12 mA	Preset 1		"	"
			21				"		-12 mA					"				D2		"	"
			22				"			-12 mA				"				Clock 2		"	"
			23				"	-12 mA						"				Clear 2		"	"
			24				"				-12 mA			"				Preset 2		"	"
	I_{IL1}	3009	25	4.5 V	0.4 V	4.5 V	5.5 V							"			GND	D1	-1.0	-2.0	mA
			26				"	4.5 V	0.4 V	4.5 V	GND			"				D2	"	"	"
			27	GND	GND	4.5 V	"							"			0.4 V	Preset 1	"	"	"
			28				"	4.5 V	GND	GND	0.4 V			"				Preset 2	"	"	"
	I_{IL2}		29	0.4 V	GND	4.5 V	"							"			GND	Clock 1	-2.0	-4.0	V
			30 CKT A,C	4.5 V	4.5 V	0.4 V	"							"			GND	Clear 1	-3.0	-6.0	"
			30 CKT B	0.8 V	4.5 V	0.4 V	"							"			4.5 V	Clear 1	-1.0	-4.0	"
			31				"	4.5 V	GND	0.4 V	GND			"				Clock 2	-2.0	-4.0	"
			32 CKT A,C				"	0.4 V	4.5 V	4.5 V	GND			"				Clear 2	-3.0	-6.0	"
			32 CKT B				"	0.4 V	4.5 V	0.8 V	4.5 V			"				Clear 2	-1.0	-4.0	"
	I_{IH1}	3010	33	4.5 V	2.4 V	GND	"							"			4.5 V	D1		50	µA
			34				"	GND	2.4 V	4.5 V	4.5 V			"				D2		50	"
	I_{IH2}		35	4.5 V	5.5 V	GND	"							"			4.5 V	D1		100	"
			36				"	GND	5.5 V	4.5 V	4.5 V			"				D2		"	"
	I_{IH3}		37	2.4 V	4.5 V	GND	"							"			4.5 V	Clock 1		"	"
			38	B	4.5 V	4.5 V	"							"			2.4 V	Preset 1		"	"
			39				"	GND	4.5 V	2.4 V	4.5 V			"				Clock 2		"	"
			40				"	4.5 V	4.5 V	B	2.4 V			"				Preset 2		"	"
	I_{IH4}		41	5.5 V	4.5 V	GND	"							"			4.5 V	Clock 1		200	"
			42	B	4.5 V	4.5 V	"							"			5.5 V	Preset 1		"	"
			43				"	GND	4.5 V	5.5 V	4.5 V			"				Clock 2		"	"
			44				"	4.5 V	4.5 V	B	5.5 V			"				Preset 2		"	"
	I_{IH5}		45	B	GND	2.4 V	"							"			4.5 V	Clear 1		150	"
			46				"	2.4 V	GND	B	4.5 V			"				Clear 2		150	"
	I_{IH6}		47	B	GND	5.5 V	"							"			4.5 V	Clear 1		300	"
			48				"	5.5 V	GND	B	4.5 V			"				Clear 2		300	"

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max	
			Test no.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q2}$	GND	$\overline{Q1}$	Q1	Preset 1				
1 T_C=+25°C	I_{OS}	3011	49				5.5 V							GND		GND	GND	Q1	-40	-100	mA
			50			GND	"							"	GND			$\overline{Q1}$	"	"	"
			51				"				GND	GND		"				Q2	"	"	"
			52				"	GND					GND	"				$\overline{Q2}$	"	"	"
	I_{CC}	3005	53	GND	GND	4.5 V	"	4.5 V	GND	GND	GND			"			GND	V_{CC}		50	"
			54	GND	GND	GND	"	GND	GND	GND	4.5 V			"			4.5 V	V_{CC}		50	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																				
7 T_C=+25°C 2/ 3/			55	B	B	B	4.5 V	B	B	B	B	H	H	GND	H	H	B	All outputs	H or L as shown 4/		
			56	"	"	B	"	B	"	"	A	L	"	"	"	L	A				
			57	"	"	A	"	A	"	"	A	L	"	"	"	L	A				
			58	"	"	"	"	"	"	"	B	H	L	"	L	H	B				
			59	A	"	"	"	"	"	A	"	"	L	"	L	"	"				
			60	"	"	B	"	B	"	"	"	"	H	"	H	"	"				
			61	"	A	"	"	B	A	"	"	"	"	"	"	"	"				
			62	"	"	"	"	A	"	"	A	L	"	"	"	L	A				
			63	"	"	A	"	"	"	"	A	L	"	"	"	L	A				
			64	"	"	"	"	"	"	"	B	H	L	"	L	H	B				
			65	"	"	"	"	"	"	"	A	"	"	"	"	"	A				
			66	B	"	"	"	"	"	B	"	"	"	"	"	"	"				
			67	B	B	"	"	"	B	B	"	"	"	"	"	"	"				
			68	A	"	"	"	"	"	A	"	L	H	"	H	L	"				
			69	"	"	"	"	"	"	"	B	H	L	"	L	H	B				
			70	"	A	B	"	B	A	"	"	"	H	"	H	"	"				
			71	"	B	"	"	"	B	"	"	"	"	"	"	"	"				
			72	"	"	"	"	"	"	"	A	L	"	"	"	L	A				
			73	"	"	A	"	A	"	"	"	"	"	"	"	"	"				
			74	B	A	"	"	"	A	B	"	"	"	"	"	"	"				
			75	A	"	"	"	"	"	A	"	H	L	"	L	H	"				
			76	"	"	"	"	"	"	"	B	"	"	"	"	"	B				
			77	"	"	"	"	"	"	"	A	"	"	"	"	"	A				
			78	"	"	B	"	B	"	"	"	L	H	"	H	L	"				
			79	"	"	A	"	A	"	"	"	L	H	"	H	L	"				
			80	"	B	"	"	"	B	"	B	H	L	"	L	H	B				
			81	"	B	"	"	"	B	"	A	H	L	"	L	H	A				
8 2/ 3/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																				
9 T_C=+25°C	f_{MAX} 5/	(Fig. 9)	82	IN	E		5.0 V							GND		OUT	5.0 V	Q1	35		MHz
			83	IN	E		"							"	OUT		5.0 V	$\overline{Q1}$	"		"
			84				"		E	IN	5.0 V	OUT		"				Q2	"		"
			85				"		E	IN	5.0 V		OUT	"				$\overline{Q2}$	"		"
	t_{PLH1}	3003 (Fig. 7)	86			IN	"							"	OUT		J	Clear 1 to $\overline{Q1}$	2	20	ns
			87			J	"							"		OUT	IN	Preset 1 to Q1	"	"	"
			88				"	IN			J		OUT	"				Clear 2 to Q2	"	"	"
			89				"	J			IN	OUT		"				Preset 2 to Q2	"	"	"
	t_{PHL1}		90			IN	"							"		OUT	J	Clear 1 to Q1	"	32	"
			91			J	"							"	OUT		IN	Preset 1 to Q1	"	"	"
			92				"	IN			J	OUT		"				Clear 2 to Q2	"	"	"
			93				"	J			IN		OUT	"				Preset 2 to Q2	"	"	"

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max	
			Test no.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q2}$	GND	$\overline{Q1}$	Q1	Preset 1				
9 T_C=+25°C	t_{PLH2}	3003 (Fig. 8)	94	IN	IN(A)	B	5.0 V							GND		OUT	5.0 V	Clock 1 to Q1	2	17	ns
		(Fig. 9)	95	IN	IN(A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 8)	96				"	B	IN(A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 9)	97				"	5.0 V	IN(A)	IN	B		OUT	"				Clock 2 to Q2	"	"	"
	t_{PHL2}	3003 (Fig. 9)	98	IN	IN(B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	22	"
		(Fig. 8)	99	IN	IN(B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 9)	100				"	5.0 V	IN(B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 8)	101				"	B	IN(B)	IN	5.0 V		OUT	"				Clock 2 to Q2	"	"	"
10 T_C=+125°C	f_{MAX}	(Fig. 8) 5/	102	IN	E		"							"		OUT	5.0 V	Q1	28	"	MHz
			103	IN	E		"							"	OUT		5.0 V	Q1	"	"	"
			104				"		E	IN	5.0 V	OUT		"				Q2	"	"	"
			105				"		E	IN	5.0 V		OUT	"				Q2	"	"	"
	t_{PLH1}	3003 (Fig. 7)	106			IN	"							"	OUT		J	Clear 1 to Q1	2	27	ns
			107			J	"							"		OUT	IN	Preset 1 to Q1	"	"	"
			108				"	IN			J		OUT	"				Clear 2 to Q2	"	"	"
			109				"	J			IN	OUT		"				Preset 2 to Q2	"	"	"
	t_{PHL1}		110			IN	"							"		OUT	J	Clear 1 to $\overline{Q1}$	"	38	"
			111			IN	"							"	OUT		IN	Preset 1 to Q1	"	"	"
			112				"	IN			J	OUT		"				Clear 2 to Q2	"	"	"
			113				"	J			IN		OUT	"				Preset 2 to Q2	"	"	"
	t_{PLH2}	3003 (Fig. 8)	114	IN	IN(A)	B	"							"		OUT	5.0 V	Clock 1 to Q1	"	22	"
		(Fig. 9)	115	IN	IN(A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 8)	116				"	B	IN(A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 9)	117				"	5.0 V	IN(A)	IN	B		OUT	"				Clock 2 to Q2	"	"	"
	t_{PHL2}	3003 (Fig. 9)	118	IN	IN(B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	28	"
		(Fig. 8)	119	IN	IN(B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q1}$	"	"	"
		(Fig. 9)	120				"	5.0 V	IN(B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
		(Fig. 8)	121				"	B	IN(B)	IN	5.0 V		OUT	"				Clock 2 to Q2	"	"	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C																				

A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
D = Momentary 4.5 V, then GND.
E = Input D connected to $\overline{Q}$.
J = Input pulse $t_p \geq 100$ ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Tests shall be performed in sequence.
3/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
4/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or b. H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.
5/ The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 04. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits		Unit
			Test no.	Clock 1	Preset 1	Clear 1	J1	V_{CC}	Clock 2	Preset 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	$\overline{Q1}$	Q1	K1		Min	Max	
1 T_C=+25°C	V_{OH}	3006	1	A			2.0 V	4.5 V								GND		-0.5 mA	0.8 V	Q1	2.4		V
			2	A			0.8 V	"								"	-0.5 mA		2.0 V	$\overline{Q1}$	"		"
			3		2.0 V	0.8 V		"								"	-0.5 mA			Q1	"		"
			4		0.8 V	2.0 V		"								"		-0.5 mA		Q1	"		"
			5					"	A			2.0 V		-0.5 mA	0.8 V	"				$\overline{Q2}$	"		"
			6					"	A			0.8 V	-0.5 mA		2.0 V	"				$\overline{Q2}$	"		"
			7					"		2.0 V	0.8 V		-0.5 mA			"				Q2	"		"
			8					"		0.8 V	2.0 V			-0.5 mA		"				Q2	"		"
	V_{OL}	3007	9	A			0.8 V	"								"		20 mA	2.0 V	Q1		0.4	"
			10	A			2.0 V	"								"	20 mA		0.8 V	$\overline{Q1}$		"	"
			11		0.8 V	2.0 V		"								"	20 mA			Q1		"	"
			12		2.0 V	0.8 V		"								"		20 mA		Q1		"	"
			13					"	A			0.8 V		20 mA	2.0 V	"				$\overline{Q2}$		"	"
			14					"	A			2.0 V	20 mA		0.8 V	"				$\overline{Q2}$		"	"
			15					"		0.8 V	2.0 V		20 mA			"				Q2		"	"
			16					"		2.0 V	0.8 V			20 mA		"				Q2		"	"
	V_{IC}		17				-12 mA	"								"			-12 mA	J1		-1.5	"
			18					"				-12 mA				"				K1		"	"
			19					"								"				J2		"	"
			20					"							-12 mA	"				K2		"	"
			21	-12 mA				"								"				Clock 1		"	"
			22		-12 mA			"								"				Preset 1		"	"
			23			-12 mA		"								"				Clear 1		"	"
			24					"	-12 mA							"				Clock 2		"	"
			25					"		-12 mA						"				Preset 2		"	"
			26					"			-12 mA					"				Clear 2		"	"
	I_{IL1}	3009	27	4.5 V	B	B	0.4 V	5.5 V			B	0.4 V				"				J1	-1.0	-2.0	mA
			28	4.5 V				"								"			0.4 V	K1	"	"	"
			29					"	4.5 V							"				J2	"	"	"
			30					"	4.5 V	B					0.4 V	"				K2	"	"	"
			31	0.4 V	B		4.5 V	"								"			4.5 V	Clock 1	"	"	"
			32	0.4 V		B	4.5 V	"								"			4.5 V	Clock 1	"	"	"
			33					"	0.4 V	B		4.5 V			4.5 V	"				Clock 2	"	"	"
			34					"	0.4 V		B	4.5 V			4.5 V	"				Clock 2	"	"	"
	I_{IL2}		35	4.5 V		0.4 V	4.5 V	"								"			4.5 V	Clear 1	-2.0	-4.0	"
			36	4.5 V	0.4 V		4.5 V	"								"			4.5 V	Preset 1	"	"	"
			37					"	4.5 V		0.4 V	4.5 V			4.5 V	"				Clear 2	"	"	"
			38					"	4.5 V	0.4 V		4.5 V			4.5 V	"				Preset 2	"	"	"
	I_{IH1}	3010	39	GND		GND	2.4 V	"								"				J1		50	µA
			40	GND	GND			"								"			2.4 V	K1		"	"
			41					"	GND		GND	2.4 V				"				J2		"	"
			42					"	GND	GND					2.4 V	"				K2		"	"
	I_{IH2}		43	GND		GND	5.5 V	"								"				J1		100	"
			44	GND	GND			"								"			5.5 V	K1		"	"
			45					"	GND		GND	5.5 V				"				J2		"	"
			46					"	GND	GND					5.5 V	"				K2		"	"
	I_{IH3}		47	2.4 V		GND	GND	"								"			GND	Clock 1		100	"
			48	GND		GND	GND	"								"				Clear 1		"	"
			49	GND	E	E		"								"			GND	Preset 1		"	"
			50					"	2.4 V		GND	GND			GND	"				Clock 2		"	"
			51					"	GND		E	GND				"				Clear 2		"	"
			52					"	GND	E					GND	"				Preset 2		"	"
	I_{IH4}		53	5.5 V		GND	GND	"								"			GND	Clock 1		200	"
			54	GND		GND	GND	"								"				Clear 1		"	"
			55	GND	F	F		"								"			GND	Preset 1		"	"
			56					"	5.5 V		GND	GND			GND	"				Clock 2		"	"
			57					"	GND		F	GND				"				Clear 2		"	"
			58					"	GND	F					GND	"				Preset 2		"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits		Unit
			Test no.	Clock 1	Preset 1	Clear 1	J1	V_{CC}	Clock 2	Preset 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	$\overline{Q1}$	Q1	K1		Min	Max	
1 T_C=+25°C	I_{OS}	3011	59**	2.4 V	GND	4.5 V	2.4 V	5.5 V								GND		GND	2.4 V	Q1	-40	-100	mA
			60	2.4 V	4.5 V	GND	2.4 V	"								"	GND		2.4 V	$\overline{Q1}$	"	"	"
			61**					"	2.4 V	GND	4.5 V	2.4 V		GND	2.4 V	"				Q2	"	"	"
			62					"	2.4 V	4.5 V	GND	2.4 V	GND		2.4 V	"				$\overline{Q2}$	"	"	"
	I_{CC}	3005	63	GND	4.5 V	GND	GND	"	GND	4.5 V	GND	GND			GND	"			GND	V_{CC}		50	"
			64	GND	GND	4.5 V	GND	"	GND	GND	4.5 V	GND			GND	"			GND	V_{CC}		50	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																						
7 T_C=+25°C 2/ 3/			65	A	B	B	B	4.5 V	A	B	B	B	H	H	B	GND	H	H	B	All outputs	H or L as shown 4/		
			66	"	B	A	"	"	"	B	A	"	L	H	"	"	L	H	"				
			67	"	A	B	"	"	"	A	B	"	H	L	"	"	H	L	"				
			68	B	"	A	"	"	B	"	A	"	"	"	"	"	"	"	"				
			69	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"				
			70	B	"	"	"	"	B	"	"	"	"	"	"	"	"	"	"				
			71	B	"	"	A	"	B	"	"	A	"	"	A	"	"	"	A				
			72	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"				
			73	B	"	"	"	"	B	"	"	"	L	H	"	"	L	H	"				
			74	B	"	"	B	"	B	"	"	B	"	"	B	"	"	"	B				
			75	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"				
			76	B	"	"	"	"	B	"	"	"	"	"	"	"	"	"	"				
			77	B	"	"	A	"	B	"	"	A	"	"	A	"	"	"	A				
			78	A	"	"	"	"	A	"	"	"	"	"	"	"	"	"	"				
			79	B	"	"	"	"	B	"	"	*A	H	L	"	"	H	L	"				
8 2/ 3/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C= +125°C and -55°C.																						
9 T_C=+25°C	f_{MAX} 5/	(Fig. 11)	80	IN	5.0 V	5.0 V	2.4 V	5.0 V								GND		OUT	2.4 V	Q1	25		MHz
			81	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	$\overline{Q1}$	"		"
			82					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
			83					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				$\overline{Q2}$	"		"
	t_{PLH1}	3003 (Fig. 10)	84	2.4 V		IN	2.4 V	"								"	OUT		2.4 V	Clear 1 to $\overline{Q1}$	2	16	ns
			85	2.4 V	IN		2.4 V	"								"		OUT	2.4 V	Preset 1 to Q1	"	"	"
			86					"	2.4 V		IN	2.4 V	OUT		2.4 V	"				Clear 2 to Q2	"	"	"
			87					"	2.4 V	IN		2.4 V		OUT	2.4 V	"				Preset 2 to Q2	"	"	"
	t_{PHL1}		88	2.4 V		IN	2.4 V	"								"		OUT	2.4 V	Clear 1 to Q1	"	27	"
			89	2.4 V	IN		2.4 V	"								"	OUT		2.4 V	Preset 1 to Q1	"	"	"
			90					"	2.4 V		IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q2	"	"	"
			91					"	2.4 V	IN		2.4 V	OUT		2.4 V	"				Preset 2 to Q2	"	"	"
	t_{PLH2}	3003 (Fig. 11)	92	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	24	"
			93	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to Q1	"	"	"
			94					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			95					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to Q2	"	"	"
	t_{PHL2}		96	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	30	"
			97	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to Q1	"	"	"
			98					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
			99					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to Q2	"	"	"

See footnotes at end of device 04.

TABLE III. Group A inspection for device type 04 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits		Unit
			Test no.	Clock 1	Preset 1	Clear 1	J1	V_{CC}	Clock 2	Preset 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	$\overline{Q1}$	Q1	K1		Min	Max	
10 T_C=+125°C	f_{MAX} 5/	(Fig. 11)	100 101 102 103	IN IN	5.0 V 5.0 V	5.0 V 5.0 V	2.4 V 2.4 V	5.0 V “ “ “	 IN IN	 5.0 V 5.0 V	 5.0 V 5.0 V	 2.4 V 2.4 V	 OUT	 OUT	 2.4 V 2.4 V	GND “ “ “	 OUT 	 	2.4 V 2.4 V	Q1 $\overline{Q1}$ Q2 $\overline{Q2}$	20 “ “ “	 	MHz “ “ “
	t_{PLH1}	3003 (Fig. 10)	104 105 106 107	2.4 V 2.4 V	 IN 	IN 	2.4 V 2.4 V 	“ “ “ “	 2.4 V 2.4 V	 IN	 IN 	 2.4 V 2.4 V	 OUT 	 OUT	 2.4 V 2.4 V	“ “ “ “	OUT 	 OUT 	2.4 V 2.4 V	Clear 1 to $\overline{Q1}$ Preset 1 to Q1 Clear 2 to Q2 Preset 2 to Q2	2 “ “ “	20 “ “ “	ns “ “ “
	t_{PHL1}		108 109 110 111	2.4 V 2.4 V	 IN 	IN 	2.4 V 2.4 V 	“ “ “ “	 2.4 V 2.4 V	 IN	 IN 	 2.4 V 2.4 V	 OUT 	 OUT	 2.4 V 2.4 V	“ “ “ “	 OUT 	OUT 	2.4 V 2.4 V	Clear 1 to Q1 Preset 1 to Q1 Clear 2 to Q2 Preset 2 to Q2	“ “ “ “	32 “ “ “	“ “ “ “
	t_{PLH2}	3003 (Fig. 11) “ “ “ “	112 113 114 115	IN IN	5.0 V 5.0 V	5.0 V 5.0 V	2.4 V 2.4 V	“ “ “ “	 IN IN	 5.0 V 5.0 V	 5.0 V 5.0 V	 2.4 V 2.4 V	 OUT	 OUT	 2.4 V 2.4 V	“ “ “ “	 OUT 	OUT 	2.4 V 2.4 V	Clock 1 to Q1 Clock 1 to Q1 Clock 2 to Q2 Clock 2 to Q2	“ “ “ “	28 “ “ “	“ “ “ “
	t_{PHL2}	“ “ “ “	116 117 118 119	IN IN	5.0 V 5.0 V	5.0 V 5.0 V	2.4 V 2.4 V	“ “ “ “	 IN IN	 5.0 V 5.0 V	 5.0 V 5.0 V	 2.4 V 2.4 V	 OUT	 OUT	 2.4 V 2.4 V	“ “ “ “	 OUT 	OUT 	2.4 V 2.4 V	Clock 1 to Q1 Clock 1 to Q1 Clock 2 to Q2 Clock 2 to Q2	“ “ “ “	36 “ “ “	“ “ “ “
11	Same tests, terminal conditions, and limits as for subgroup 10, except T_C= -55°C.																						

A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
E = Momentary GND, then 2.4 V.
F = Momentary GND, then 5.5 V.
** = Test time limit ≤ 100 ns.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Tests shall be performed in sequence.
3/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
4/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or b. H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.
5/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 05. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	10	13	14	1	2	3	4	5	6	7	8	11	11		Min	Max	
			Test no.	K1A	K1B	Clock	V_{CC}	J1A	J1B	J2A	J2B	Preset	Q	GND	$\overline{Q}$	K2A	K2B				
1 T_C=+25°C	V_{OH}	3006	1	0.8 V	0.8 V	A	4.5 V	2.0 V	2.0 V	2.0 V	2.0 V		-0.5 mA	GND		0.8 V	0.8 V	Q/$\overline{Q}$	2.4		V
			2	2.0 V	2.0 V	A	"	0.8 V	0.8 V	0.8 V	0.8 V			"	-0.5 mA	2.0 V	2.0 V	Q	"		"
			3	2.0 V	2.0 V	2.0 V	"	2.0 V	2.0 V	2.0 V			-0.5 mA	"		2.0 V	2.0 V	$\overline{Q}$	"		"
	V_{OL}	3007	4	0.8 V	0.8 V	A	"	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V		"	20 mA	0.8 V	0.8 V	Q/$\overline{Q}$		0.4	"
			5	2.0 V	2.0 V	A	"	0.8 V	0.8 V	0.8 V	0.8 V		20 mA	"		2.0 V	2.0 V	Q/$\overline{Q}$		"	"
			6	2.0 V	2.0 V	2.0 V	"	2.0 V	2.0 V	2.0 V		0.8 V		"	20 mA	2.0 V	2.0 V	$\overline{Q}$		"	"
	V_{IC}		7				"	-12 mA						"				J1A		-1.5	"
			8				"		-12 mA					"				J1B		"	"
			9				"			-12 mA				"				J2A		"	"
			10				"				-12 mA			"				J2B		"	"
			11	-12 mA			"							"				K1A		"	"
			12		-12 mA		"							"				K1B		"	"
			13				"							"		-12 mA		K2A		"	"
			14				"							"			-12 mA	K2B		"	"
			15			-12 mA	"							"				Clock		"	"
			16				"					-12 mA		"				Preset		"	"
	I_{IL1}	3009	17	4.5 V	4.5 V	4.5 V	5.5 V	4.5 V	4.5 V	4.5 V	4.5 V	0.4 V		"		4.5 V	4.5 V	Preset	-0.7	-2.0	mA
			18*	"	"	2/	"	0.4 V	4.5 V	GND	"	4.5 V		"		"	"	J1A	"	"	"
			19*	"	"	"	"	4.5 V	0.4 V	GND	"	"		"		"	"	J1B	"	"	"
			20*	"	"	"	"	GND	4.5 V	0.4 V	"	"		"		"	"	J2A	"	"	"
			21*	"	"	"	"	GND	"	4.5 V	0.4 V	"		"		"	"	J2B	"	"	"
			22	0.4 V	"	4.5 V	"	4.5 V	"	"	4.5 V	GND		"		"	"	K1A	"	"	"
			23	4.5 V	0.4 V	"	"	"	"	"	"	"		"		"	"	K1B	"	"	"
			24	"	4.5 V	"	"	"	"	"	"	"		"		0.4 V	"	K2A	"	"	"
			25	"	"	"	"	"	"	"	"	"		"		4.5 V	0.4 V	K2B	"	"	"
	I_{IL2}		26	"	"	0.4 V	"	"	"	"	"	"		"		"	4.5 V	Clock	-2.0	-4.8	"
	I_{IH1}	3010	27	"	"	GND	"	2.4 V	GND	GND	GND	"		"		"	"	J1A		50	µA
			28	"	"	"	"	GND	2.4 V	GND	GND	"		"		"	"	J1B		"	"
			29	"	"	"	"	"	GND	2.4 V	GND	"		"		"	"	J2A		"	"
			30	"	"	"	"	"	GND	GND	2.4 V	"		"		"	"	J2B		"	"
			31	2.4 V	GND	"	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V		"		GND	GND	K1A		"	"
			32	GND	2.4 V	"	"	"	"	"	"	"		"		GND	"	K1B		"	"
			33	"	GND	"	"	"	"	"	"	"		"		2.4 V	"	K2A		"	"
			34	"	GND	"	"	"	"	"	"	"		"		GND	2.4 V	K2B		"	"
	I_{IH2}		35	4.5 V	4.5 V	"	"	5.5 V	GND	GND	GND	GND		"		4.5 V	4.5 V	J1A		100	"
			36	"	"	"	"	GND	4.5 V	GND	GND	"		"		"	"	J1B		"	"
			37	"	"	"	"	"	GND	5.5 V	GND	"		"		"	"	J2A		"	"
			38	"	"	"	"	"	GND	GND	5.5 V	"		"		"	"	J2B		"	"
			39	5.5 V	GND	"	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V		"		GND	GND	K1A		"	"
			40	GND	5.5 V	"	"	"	"	"	"	"		"		GND	"	K1B		"	"
			41	"	GND	"	"	"	"	"	"	"		"		5.5 V	"	K2A		"	"
			42	"	"	"	"	"	"	"	"	"		"		GND	5.5 V	K2B		"	"
	I_{IH3}		43*	"	"	D	"	"	"	"	"	2.4 V		"		"	GND	Preset		"	"
	I_{IH4}		44*	"	"	D	"	"	"	"	"	5.5 V		"		"	"	Preset		200	"
	I_{IH5}		45	"	"	2.4 V	"	GND	GND	GND	GND	GND		"		"	"	Clock		-1	mA
	I_{IH6}		46	"	"	5.5 V	"	GND	GND	GND	GND	GND		"		"	"	Clock		1	mA

See footnotes at end of device type 05.

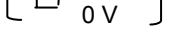
TABLE III. Group A inspection for device type 05. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	10	13	14	1	2	3	4	5	6	7	8	11	11		Min	Max	
			Test no.	K1A	K1B	Clock	V_{CC}	J1A	J1B	J2A	J2B	Preset	Q	GND	$\overline{Q}$	K2A	K2B				
1 T_C=+25°C	I_{OS}	3011	47	2.4 V	2.4 V	2.4 V	5.5 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	GND	GND		2.4 V	2.4 V	Q	-40	-100	mA
			48	2.4 V	2.4 V	2.4 V	"	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	GND	"	GND	2.4 V	2.4 V	Q	-40	-100	"
	I_{CC}	3005	49	GND	GND	GND	"	GND	GND	GND	GND	GND		"		GND	GND	V_{CC}		38	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C= +125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C= -55°C and V_{IC} tests are omitted.																				
7 T_C=+25°C 3/ 4/			50	B	A	A	4.5 V	B	A	B	A	B	H	GND	L	B	A	All outputs	H or L as shown 5/		
			51	"	"	A	"	"	"	"	"	A	"	"	"	"	"				
			52	"	"	B	"	"	"	"	"	"	"	"	"	"	"				
			53	"	"	A	"	"	"	"	"	"	"	"	"	A	"				
			54	"	"	B	"	"	"	"	"	"	L	"	H	"	"				
			55	"	"	A	"	"	"	"	"	"	L	"	H	"	"				
			56	"	"	A	"	"	"	"	"	B	H	"	L	"	"				
			57	"	"	B	"	"	"	"	"	B		"	"	"	"				
			58	A	B	A	"	"	"	"	"	A	"	"	"	"	B				
			59	"	B	B	"	"	"	"	"	"	"	"	"	"	"				
			60	"	A	A	"	A	"	"	"	"	"	"	"	"	"				
			61	"	A	B	"	A	"	"	"	"	L	"	H	"	"				
			62	"	B	A	"	B	"	"	"	"	"	"	"	"	"				
			63	"	"	B	"	B	"	"	"	"	"	"	"	"	"				
			64	"	"	A	"	A	B	A	B	"	"	"	"	"	"				
			65	"	"	B	"	"	B	"	"	"	"	"	"	"	"				
			66	"	A	A	"	"	A	"	"	"	"	"	"	"	"				
			67	"	A	B	"	"	A	"	"	"	H	"	L	"	"				
			68	"	B	A	"	"	B	"	A	"	H	"	L	"	A				
			69	"	"	B	"	"	"	"	"	"	L	"	H	"	"				
			70	"	"	A	"	"	"	"	"	"	L	"	H	"	"				
			71	"	"	B	"	"	"	"	"	"	H	"	L	"	"				
8 3/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C=+125°C and -55°C.																				
9 T_C=+25°C	f_{MAX} 6/	(Fig. 13)	72	2.4 V	2.4 V	IN	5.0 V	2.4 V	2.4 V	2.4 V	2.4 V	5.0 V	OUT	GND		2.4 V	2.4 V	$\overline{Q}$	36		MHz
			73	"	"	"	"	"	"	"	"	5.0 V		"	OUT	"	"	Q	36		MHz
	t_{PLH1}	3003 (Fig. 13)	74	"	"	"	"	"	"	"	"	IN	OUT	"		"	"	Preset to $\overline{Q}$	2	23	ns
			75	"	"	"	"	"	"	"	"	IN		"	OUT	"	"	Preset to Q	"	23	"
	t_{PLH2}	3003 (Fig. 13)	76	"	"	"	"	H	"	GND	GND		OUT	"		GND	GND	Clock $\overline{Q}$	"	18	"
			77	H	"	"	"	2.4 V	"	"	"			"	OUT	"	"	Clock Q	"	18	"
	t_{PHL2}		78	L	"	"	"	2.4 V	"	"	"		OUT	"		"	"	Clock $\overline{Q}$	"	23	"
			79	2.4 V	"	"	"	H	"	"	"			"	OUT	"	"	Clock Q	"	23	"

TABLE III. Group A inspection for device type 05. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	9	10	13	14	1	2	3	4	5	6	7	8	11	11		Min	Max	
			Test no.	K1A	K1B	Clock	V_{CC}	J1A	J1B	J2A	J2B	Preset	Q	GND	Q	K2A	K2B				
10 T_C=+125°C	f_{MAX} 6/	(Fig. 13)	80 81	2.4 V “	2.4 V “	IN “	5.0 V “	2.4 V “	2.4 V “	2.4 V “	2.4 V “	5.0 V 5.0 V	OUT	GND “	OUT	2.4 V “	2.4 V “	$\overline{Q}$ Q	30 30		MHz MHz
	t_{PLH1}	3003 (Fig. 13)	82 83	“ “	“ “	“ “	“ “	“ “	“ “	“ “	“ “	IN IN	OUT	“ “	OUT	“ “	“ “	Preset to $\overline{Q}$ Preset to Q	2 “	28 28	ns “
	t_{PLH2}	3003 (Fig. 13)	84 85	“ H	“ “	“ “	“ “	H 2.4 V	“ “	GND “	GND “		OUT	“ “	OUT	GND “	GND “	Clock $\overline{Q}$ Clock Q	“ “	23 23	“ “
	t_{PHL2}		86 87	L 2.4 V	“ “	“ “	“ “	2.4 V M	“ “	“ “	“ “		OUT	“ “	OUT	“ “	“ “	Clock $\overline{Q}$ Clock Q	“ “	28 28	“ “
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C=-55°C																				

A = Normal clock pulse.
D = Momentary 4.5 V, then GND.
H = t_{setup} waveform, see figure 13.
L = t_{setup} waveform, see figure 13.
M = t_{setup} waveform, see figure 13.
* = Duration of test should not exceed 1 second.
** = Limit duration of this test to 100 ns.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ The clock Input shall be 4.5 V with a momentary low pulse, then 4.5 V 

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3/ Tests shall be performed in sequence.
4/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
5/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or b. H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.
6/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 06. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	Q1	$\overline{Q1}$	J1				
1 T_C=+25°C	V_{OH}	3006	1 2 3 4 5 6	D D	0.8 V	0.8 V 2.0 V	4.5 V “ “ “ “ “	D D	0.8 V	2.0 V 0.8 V	-0.5 mA -0.5 mA	-0.5 mA	0.8 V 2.0 V	GND “ “ “ “ “	-0.5 mA	-0.5 mA -0.5 mA	2.0 V 0.8 V	Q1 Q1 Q1 Q2 Q2 Q2	2.4 “ “ “ “ “		V “ “ “ “ “
	V_{OL}	3007	7 8 9 10 11 12	D D	0.8 V	2.0 V 0.8 V	“ “ “ “ “ “	D D	0.8 V	0.8 V 2.0 V	20 mA	20 mA	2.0 V 0.8 V	“ “ “ “ “ “	20 mA 20 mA	20 mA	0.8 V 2.0 V	Q1 Q1 Q1 Q2 Q2 Q2		0.4 “ “ “ “ “	“ “ “ “ “ “
	V_{IC}		13 14 15 16 17 18 19 20	-12 mA	-12 mA	-12 mA	“ “ “ “ “ “ “ “	-12 mA	-12 mA	-12 mA			-12 mA	“ “ “ “ “ “ “ “			-12 mA	J1 J2 K1 K2 Clear 1 Clock 1 Clear 2 Clock 2		-1.5 “ “ “ “ “ “ “	“ “ “ “ “ “ “ “
	I_{IL1}	3009	21 22** 23 24** 25 26	4.5 V 2/ 4.5 V 	GND 4.5 V 0.4 V 	4.5 V 0.4 V 4.5 V 	5.5 V “ “ “ “ “	4.5 V 2/ 4.5 V	GND 4.5 V 0.4 V	0.4 V 4.5 V 4.5 V	GND		4.5 V 0.4 V 4.5 V	“ “ “ “ “ “		GND	0.4 V 4.5 V 4.5 V 	J1 K1 J2 K2 Clear 1 Clear 2	-0.7 “ “ “ “ “	-2.0 “ “ “ “ “	mA “ “ “ “ “
	I_{IL2}		27 28	0.4 V	GND	4.5 V	“ “	0.4 V	GND	4.5 V			4.5 V	“ “			4.5 V	Clock 1 Clock 2	-2.0 -2.0	-4.8 -4.8	“ “
	I_{IH1}	3010	29 30 31 32	D GND 	4.5 V GND 	GND 2.4 V 	“ “ “ “	D GND	4.5 V GND	2.4 V 4.5 V			GND 2.4 V	“ “ “ “			2.4 V 4.5 V 	J1 J2 K1 K2		50 “ “ “	µA “ “ “
	I_{IH2}		33 34 35 36	D GND 	4.5 V GND 	GND 5.5 V 	“ “ “ “	D GND	4.5 V GND	5.5 V 4.5 V			GND 5.5 V	“ “ “ “			5.5 V 4.5 V 	J1 J2 K1 K2		1 “ “ “	mA “ “ “
	I_{IH3}		37 38	2.4 V	GND	GND	“ “	2.4 V	GND	GND			GND	“ “			GND	Clock 1 Clock 2	-1 -1	“ “	“ “
	I_{IH4}		39 40	5.5 V	GND	GND	“ “	5.5 V	GND	GND			GND	“ “			GND	Clock 1 Clock 2		“ “	“ “
	I_{IH5}		41* 42*	2/	2.4 V	4.5 V	“ “	2/	2.4 V	GND			4.5 V	“ “			GND	Clear 1 Clear 2		100 100	µA µA
	I_{IH6}		43* 44*	2/	5.5 V	4.5 V	“ “	2/	5.5 V	GND			4.5 V	“ “			GND	Clear 1 Clear 2		1 1	mA mA

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	Q1	$\overline{Q1}$	J1				
1 T_C=+25°C	I_{OS}	3011	45**	2.4 V	2.4 V	2.4 V	5.5 V							GND	GND	GND	2.4 V	$\overline{Q}$1	-40	-100	mA
			46	2.4 V	GND	2.4 V	"							"		GND	24.V	Q1	"	"	"
			47**				"	2.4 V	2.4 V	2.4 V	GND	GND	2.4 V	"				Q2	"	"	"
			48				"	2.4 V	GND	2.4 V	GND		2.4 V	"				Q2	"	"	"
	I_{CC}	3005	49	GND	GND	GND	"	GND	GND	GND			GND	"			GND	V_{CC}		76	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C=+125°C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C=-55°C and V_{IC} tests are omitted.																				
7 T_C=+25°C 3/ 4/			50	A	B	B	4.5 V	A	B	B	H	L	B	GND	L	H	B	All outputs	H or L as shown 5/		
			51	A	A	"	"	A	A	"	"	"	"	"	"	"	"				
			52	B	"	"	"	B	"	"	"	"	"	"	"	"	"				
			53	A	"	"	"	A	"	A	"	"	"	"	"	"	A				
			54	B	"	"	"	B	"	"	L	H	"	"	H	L	"				
			55	A	"	"	"	A	"	"	L	H	"	"	H	L	"				
			56	A	B	"	"	A	B	"	H	L	"	"	L	H	"				
			57	B	B	"	"	B	B	"	"	"	"	"	"	"	"				
			58	A	A	A	"	A	A	"	"	"	A	"	"	"	"				
			59	B	"	A	"	B	"	"	L	H	A	"	H	L	"				
			60	A	"	B	"	A	"	B	"	"	B	"	"	"	B				
			61	B	"	B	"	B	"	B	"	"	B	"	"	"	B				
			62	A	"	A	"	A	"	A	"	"	A	"	"	"	A				
			63	B	"	A	"	B	"	A	H	L	A	"	L	H	A				
8 3/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C= +125°C and -55°C.																				
9 T_C=+25°C	f_{MAX} 6/	(Fig. 15)	64	IN	5.0 V	2.4 V	5.0 V							GND	OUT		2.4 V	$\overline{Q}$1	36		MHz
			65	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	Q1	"		"
			66				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				$\overline{Q}$2	"		"
			67				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				Q2	"		"
	t_{PLH1}	3003 (Fig. 14)	68	G	IN	2.4 V	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}$	2	15	ns
			69				"	B	IN	2.4 V	OUT		2.4 V	"				Clear 2 to Q	"	15	"
	t_{PHL1}		70	F	IN	2.4 V	"							"	OUT		2.4 V	Clear 1 to Q	"	38	"
			71				"	G	IN	2.4 V		OUT	2.4 V	"				Clock 2 to Q	"	38	"
			72	G	IN	2.4 V	"							"	OUT		2.4 V	Clock 1 to Q	"	23	"
			73				"	G	IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q	"	23	"
	t_{PLH2}	3003 (Fig. 15)	74	IN		2.4 V	"							"	OUT		N	Clock 1 to $\overline{Q}$	"	18	"
			75	IN		P	"							"		OUT	2.4 V	Clock 1 to Q	"	"	"
			76				"	IN		IN		OUT	2.4 V	"				Clock 2 to $\overline{Q}$	"	"	"
			77				"	IN		2.4 V	OUT		P	"				Clock 2 to Q	"	"	"
	t_{PHL2}		78	IN		R	"							"	OUT		2.4 V	Clock 1 to $\overline{Q}$	"	23	"
			79	IN		2.4 V	"							"		OUT	S	Clock 1 to Q	"	"	"
			80				"	IN		2.4 V		OUT	R	"				Clock 2 to $\overline{Q}$	"	"	"
			81				"	IN		S	OUT		2.4 V	"				Clock 2 to Q	"	"	"

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
			Test no.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q2}$	Q2	K2	GND	Q1	$\overline{Q1}$	J1				
10 T_C=+125°C	f_{MAX} 6/	(Fig. 15)	82	IN	5.0 V	2.4 V	5.0 V							GND	OUT		2.4 V	Q1	30		MHz
			83	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	$\overline{Q1}$	"		"
			84				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
			85				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				$\overline{Q2}$	"		"
	t_{PLH1}	3003 (Fig. 14)	86	G	IN	2.4 V	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}$	2	18	ns
			87				"	G	IN	2.4 V	OUT		2.4 V	"				Clear 2 to Q	"	18	"
	t_{PHL1}		88	F	IN	2.4 V	"							"	OUT		2.4 V	Clear 1 to Q	"	46	"
			89				"	F	IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q	"	46	"
			90	G	IN	2.4 V	"							"	OUT		2.4 V	Clock 1 to Q	"	28	"
			91				"	G	IN	2.4 V		OUT	2.4 V	"				Clock 2 to Q	"	28	"
	t_{PLH2}	3003 (Fig. 15)	92	IN		2.4 V	"							"	OUT		N	Clock 1 to Q	"	23	"
			93	IN		P	"							"		OUT	2.4 V	Clock 1 to Q	"	"	"
			94				"	IN		N		OUT	2.4 V	"				Clock 2 to Q	"	"	"
			95				"	IN		2.4 V	OUT		P	"				Clock 2 to Q	"	"	"
	t_{PHL2}		96	IN		R	"							"	OUT		2.4 V	Clock 1 to Q	"	28	"
			97	IN		2.4 V	"							"		OUT	S	Clock 1 to Q	"	"	"
			98				"	IN		2.4 V		OUT	R	"				Clock 2 to Q	"	"	"
			99				"	IN		S	OUT		2.4 V	"				Clock 2 to Q	"	"	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T_C = -55°C.																				

A = Normal clock pulse.
D = Momentary 4.5 V, then GND.
F = Momentary 0 V, then Vgen, see figure 14.
G = Momentary Vgen, then 0 V, see figure 14.
N = t_{setup} waveform, see figure 15.
P = t_{setup} waveform, see figure 15.
R = t_{setup} waveform, see figure 15.
S = t_{setup} waveform, see figure 15.
* = Duration of test should not exceed 1 second.
** = Limit duration of this test to 100 ns.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input shall be 4.5 V with a momentary ground, then 4.5 V 4.5 V / 0 V.
3/ Tests shall be performed in sequence.
4/ Input voltages shown are: A = 2.0 volts minimum and B = 0.8 volts maximum.
5/ Output voltages shall be either: a. H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or b. H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.
6/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirements for "JAN" marking.

j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND ..... Ground zero voltage potential
V_{IN} ..... Voltage level at an input terminal
I_{IN} ..... Current flowing into an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	54H72 (circuit A)
01	S54H72 (circuit B)
02	54H73 (circuit A)
02	MC54H73 (circuit B)
02	S54H73 (circuit C)
03	54H74 (circuit A)
03	MC54H74 (circuit B)
03	S54H74 (circuit C)
04	54H76 (circuit A)
04	S54H76 (circuit B)
05	54H101 (circuit A)
05	MC54H101 (circuit B)
05	S54H101 (circuit C)
06	54H103 (circuit A)
06	54H103 (circuit B)
06	S54H103 (circuit C)

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

(Project 5962-2113)

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force - 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.