

74AC/ACT11245

Octal Transceiver with Direction Pin; 3-State

Product Specification

ACL Products

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11245 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11245 device is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable (\overline{OE}) input for easy cascading and a Direction (DIR) input for direction control.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS		TYPICAL		UNIT
		$T_A = 25^\circ\text{C}; \text{GND} = 0\text{V}; V_{CC} = 5.0\text{V}$		AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n , or B_n to A_n	$C_L = 50\text{pF}$		4.5	5.8	ns
C_{PD}	Power dissipation capacitance per transceiver ¹	$f = 1\text{MHz}; C_L = 50\text{pF}$	Enabled	64	66	pF
			Disabled	16	19	
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	$V_I = 0\text{V}$ or V_{CC} ; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17		500	500	mA

Note:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

where:

f_i = input frequency in MHz, C_L = output load capacitance in pF,

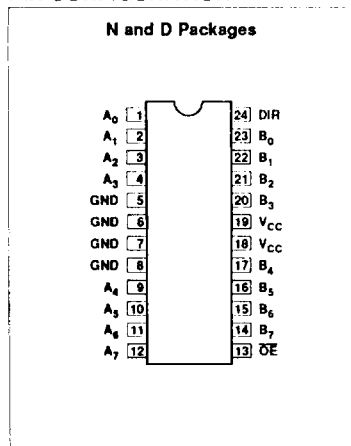
f_o = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

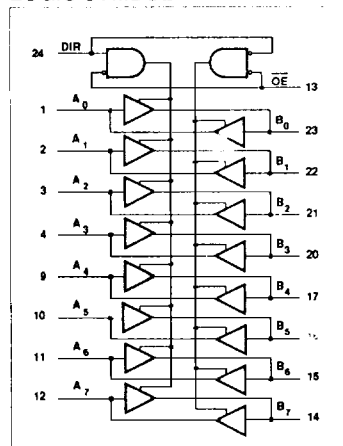
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11245N 74ACT11245N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11245D 74ACT11245D

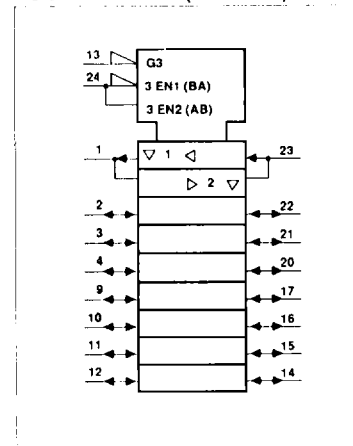
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	$A_0 - A_7$	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	$B_0 - B_7$	Data inputs/outputs (B side)
13	\overline{OE}	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{OE}	DIR	A_n	B_n
L	L	$A = B$	inputs
L	H	inputs	$B = A$
H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11245			74ACT11245			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta t$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±150	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11245				74ACT11245				UNIT														
				T _A = +25°C		T _A = -40°C to +85°C		T _A = +25°C		T _A = -40°C to +85°C																
				Min	Max	Min	Max	Min	Max	Min	Max															
V _{IH}	High-level input voltage		3.0	2.10		2.10						V														
			4.5	3.15		3.15		2.0		2.0																
			5.5	3.85		3.85		2.0		2.0																
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V														
			4.5		1.35		1.35		0.8		0.8															
			5.5		1.65		1.65		0.8		0.8															
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}			I _{OH} = -50μA	3.0	2.9		2.9				V													
						4.5	4.4		4.4		4.4			4.4												
						5.5	5.4		5.4		5.4			5.4												
						3.0	2.58	2.48		I _{OH} = -4mA																
																			4.5	3.94		3.8		3.94		3.8
																			5.5	4.94		4.8		4.94		4.8
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}			I _{OL} = 50μA	3.0		0.1		0.1			V													
						4.5		0.1		0.1		0.1			0.1											
						5.5		0.1		0.1		0.1			0.1											
						3.0	0.36	0.44		I _{OL} = 12mA																
																			4.5	0.36		0.44		0.36		0.44
																			5.5	0.36		0.44		0.36		0.44
5.5		1.65		I _{OL} = 24mA																						
												5.5			1.65				1.65							
5.5		3.85		I _{OL} = 75mA ¹																						
												5.5			3.85				3.85							
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA														
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		±5.0		±0.5		±5.0	μA														
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		8.0		80		8.0		80	μA														
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA														

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11245					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to B _n , B _n to A _n	1	1.5 1.5	6.5 5.7	11.2 8.5	1.5 1.5	12.5 9.7	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.6 8.2	14.2 11.5	1.5 1.5	15.9 12.7	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.7 8.5	10.5 12.0	1.5 1.5	11.3 13.0	ns

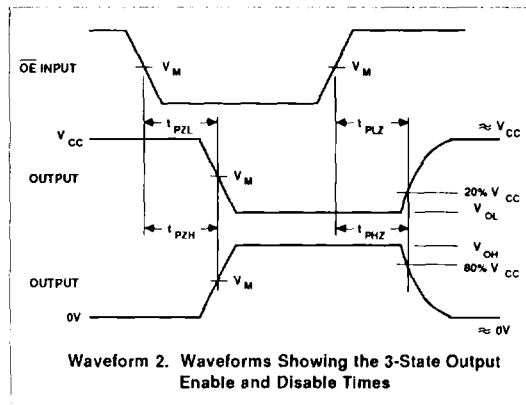
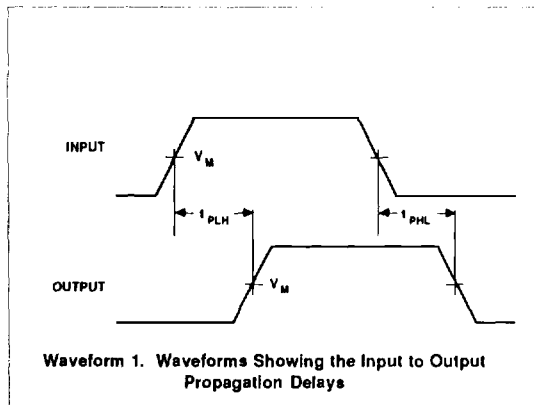
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11245					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to B _n , B _n to A _n	1	1.5 1.5	4.8 4.1	8.5 6.3	1.5 1.5	9.5 6.9	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.2 5.9	10.2 8.6	1.5 1.5	11.4 9.5	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	6.4 7.0	8.8 9.6	1.5 1.5	9.5 10.4	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11245					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to B _n , B _n to A _n	1	1.5 1.5	6.2 5.4	9.2 8.6	1.5 1.5	10.0 9.1	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.1 8.2	12.0 11.7	1.5 1.5	13.2 12.9	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.3 9.8	11.8 12.9	1.5 1.5	12.9 13.9	ns

AC WAVEFORMS



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WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$, $V_M = 1.5V$	$V_M = 50\% V_{CC}$

TEST CIRCUIT

