

## Phase-Aligned Clock Multiplier

### Features

- 4-multiplier configuration
- Single phase-locked loop architecture
- Phase Alignment
- Low jitter, high accuracy outputs
- Output enable pin
- 3.3V operation
- 5V Tolerant input
- Internal loop filter
- 8-pin 150-mil SOIC package
- Commercial and Industrial Temperature available

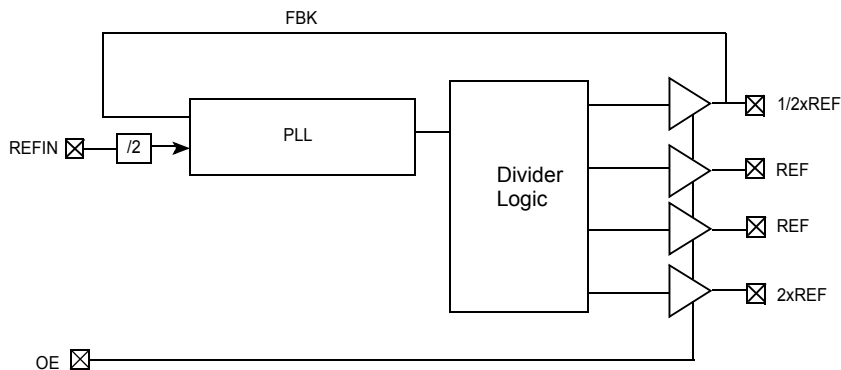
### Benefits

- 1/2x, 1x, 1x, 2x Ref
- 10 MHz to 166.67 MHz operating range (reference input from 20 MHz to 83.33 MHz)
- All outputs will have a consistent phase relationship with each other and the reference input
- Meets critical timing requirements
- Enables design flexibility and lower power consumption
- Supports industry standard design platforms
- Allows flexibility on Reference input
- Alleviates the need for external components
- Industry standard packaging saves on board space
- Suitable for wide spectrum of applications

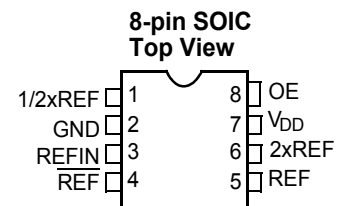
### Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2300SC	4	20 MHz–83.33 MHz	10 MHz–166.67 MHz	Commercial Temperature
CY2300SI	4	20 MHz–83.33 MHz	10 MHz–166.67 MHz	Industrial Temperature

### Block Diagram



### Pin Configuration



**Pin Definitions**

Pin	Signal <sup>[1]</sup>	Description
1	1/2xREF	Clock output, 1/2x Reference
2	GND	Ground
3	REFIN	Input Reference frequency, 5V tolerant input
4	$\overline{\text{REF}}$	Clock output $\overline{\text{Reference}}$
5	REF	Clock output Reference
6	2xREF	Clock output, 2x Reference
7	VDD	3.3V Supply
8	OE	Output Enable (weak pull-up)

**Functional Description**

The CY2300 is a 4-output 3.3V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part allows the user to obtain 1/2x, 1x,  $\overline{1x}$  and 2x REFIN output frequencies on respective output pins.

The part has an on-chip PLL which locks to an input clock presented on the REFIN pin. The input-to-output skew is guaranteed to be less than  $\pm 200$  ps, and output-to-output skew is guaranteed to be less than 200 ps.

Multiple CY2300 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.

The CY2300 is available in commercial and industrial temperature ranges.

**Maximum Ratings**

Supply Voltage to Ground Potential .....	-0.5V to +7.0V
DC Input Voltage (Except Ref) .....	-0.5V to $V_{DD} + 0.5V$
DC Input Voltage REF .....	-0.5 to 7V
Storage Temperature .....	-65°C to +150°C
Junction Temperature .....	150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015) .....	>2000V

**Operating Conditions for CY2300SC Commercial Temperature Devices**

Parameter	Description	Min.	Max.	Unit
$V_{DD}$	Supply Voltage	3.0	3.6	V
$T_A$	Operating Temperature (Ambient Temperature)	0	70	°C
$C_L$	Load Capacitance, $F_{out} < 133.33$ MHz		18	pF
	Load Capacitance, $133.33$ MHz $< F_{out} < 166.67$ MHz		12	pF
$C_{IN}$	Input Capacitance		7	pF
$t_{PU}$	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

**Electrical Characteristics for CY2300SC Commercial Temperature Devices**

Parameter	Description		Min.	Max.	Unit
$V_{IL}$	Input LOW Voltage			0.8	V
$V_{IH}$	Input HIGH Voltage		2.0		V
$I_{IL}$	Input LOW Current	$V_{IN} = 0V$		100	$\mu A$
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{DD}$		50	$\mu A$
$V_{OL}$	Output LOW Voltage <sup>[2]</sup>	$I_{OL} = 8$ mA		0.4	V
$V_{OH}$	Output HIGH Voltage <sup>[2]</sup>	$I_{OH} = -8$ mA	2.4		V
$I_{DD}$	Supply Current	Unloaded outputs, REFIN = 66 MHz		45	mA
		Unloaded outputs, REFIN = 33 MHz		32	mA
		Unloaded outputs, REFIN = 20 MHz		18	mA

**Notes:**

- Weak pull-down on all outputs.
- Parameter is guaranteed by design and characterization. It is not 100% tested in production.

**Switching Characteristics for CY2300SC Commercial Temperature Devices**

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
1/t <sub>1</sub>	Output Frequency	18-pF load	10		133.33	MHz
		12-pF load			166.67	MHz
	Duty Cycle <sup>[3]</sup> = t <sub>2</sub> ÷ t <sub>1</sub>	Measured at V <sub>DD</sub> /2	40	50	60	%
t <sub>3</sub>	Rise Time <sup>[3]</sup>	Measured between 0.8V and 2.0V			1.20	ns
t <sub>4</sub>	Fall Time <sup>[3]</sup>	Measured between 0.8V and 2.0V			1.20	ns
t <sub>5</sub>	Output to Output Skew on rising edges <sup>[3]</sup>	All outputs equally loaded Measured at V <sub>DD</sub> /2			200	ps
t <sub>6</sub>	Delay, REFIN Rising Edge to Output Rising Edge <sup>[3]</sup>	Measured at V <sub>DD</sub> /2 from REFIN to any output			±200	ps
t <sub>7</sub>	Device to Device Skew <sup>[3]</sup>	Measured at V <sub>DD</sub> /2 on the 1/2xREF pin of devices (pin 1)			400	ps
t <sub>J</sub>	Period Jitter <sup>[3]</sup>	Measured at F <sub>out</sub> =133.33 MHz, loaded outputs, 18-pF load			±175	ps
t <sub>LOCK</sub>	PLL Lock Time <sup>[3]</sup>	Stable power supply, valid clocks presented on REFIN			1.0	ms

**Operating Conditions for CY2300SI Industrial Temperature Devices**

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	3.0	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	-40	85	°C
C <sub>L</sub>	Load Capacitance, F <sub>out</sub> < 133.33 MHz		15	pF
	Load Capacitance, 133.33 MHz < F <sub>out</sub> < 166.67MHz		10	pF
C <sub>IN</sub>	Input Capacitance		7	pF
t <sub>PU</sub>	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

**Electrical Characteristics for CY2300SI Industrial Temperature Devices**

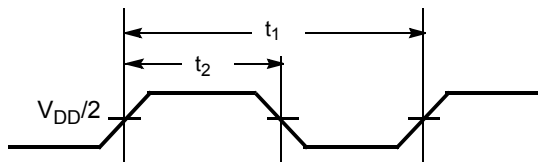
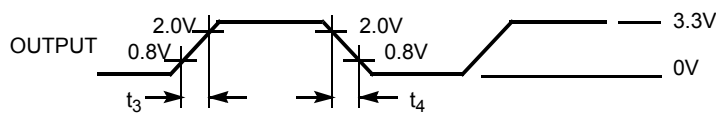
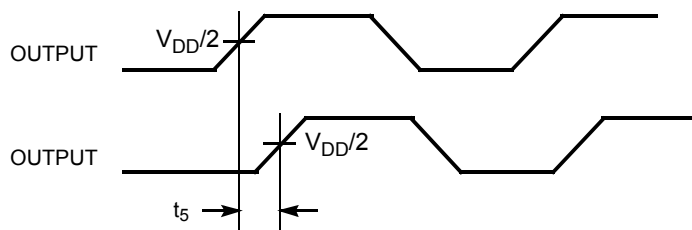
Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>IL</sub>	Input LOW Voltage			0.8	V
V <sub>IH</sub>	Input HIGH Voltage		2.0		V
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0V		100	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = V <sub>DD</sub>		50	μA
V <sub>OL</sub>	Output LOW Voltage <sup>[2]</sup>	I <sub>OL</sub> = 8 mA		0.4	V
V <sub>OH</sub>	Output HIGH Voltage <sup>[2]</sup>	I <sub>OH</sub> = -8 mA	2.4		V
I <sub>DD</sub>	Supply Current	Unloaded outputs, REFIN = 66 MHz		48	mA
		Unloaded outputs, REFIN = 33 MHz		35	mA
		Unloaded outputs, REFIN = 20 MHz		20	mA

**Note:**

3. All parameters are specified with equally loaded outputs.

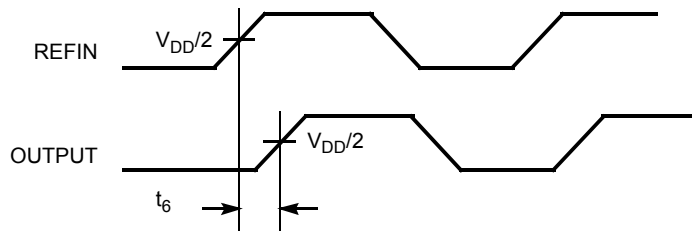
**Switching Characteristics for CY2300SI Industrial Temperature Devices**

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
1/t <sub>1</sub>	Output Frequency	15-pF load	10		133.33	MHz
		10-pF load			166.67	MHz
	Duty Cycle <sup>[3]</sup> = t <sub>2</sub> ÷ t <sub>1</sub>	Measured at V <sub>DD</sub> /2	40	50	60	%
t <sub>3</sub>	Rise Time <sup>[3]</sup>	Measured between 0.8V and 2.0V			1.20	ns
t <sub>4</sub>	Fall Time <sup>[3]</sup>	Measured between 0.8V and 2.0V			1.20	ns
t <sub>5</sub>	Output to Output Skew on rising edges <sup>[3]</sup>	All outputs equally loaded Measured at V <sub>DD</sub> /2			200	ps
t <sub>6</sub>	Delay, REFIN Rising Edge to Output Rising Edge <sup>[3]</sup>	Measured at V <sub>DD</sub> /2 from REFIN to any output			±200	ps
t <sub>7</sub>	Device to Device Skew <sup>[3]</sup>	Measured at V <sub>DD</sub> /2 on the 1/2xREF pin of devices (pin 1)			400	ps
t <sub>J</sub>	Period Jitter <sup>[3]</sup>	Measured at F <sub>out</sub> =133.33 MHz, loaded outputs, 15-pF load			±175	ps
t <sub>LOCK</sub>	PLL Lock Time <sup>[3]</sup>	Stable power supply, valid clocks present on REFIN			1.0	ms

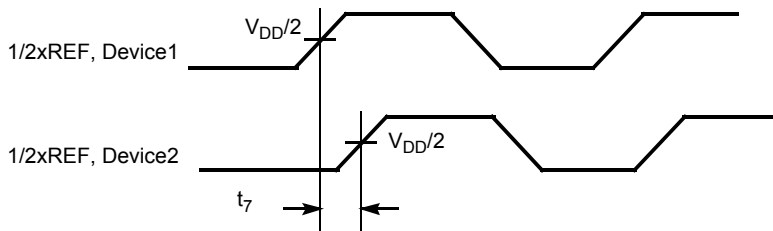
**Switching Waveforms**
**Duty Cycle Timing**

**All Outputs Rise/Fall Time**

**Output-Output Skew**


## Switching Waveforms

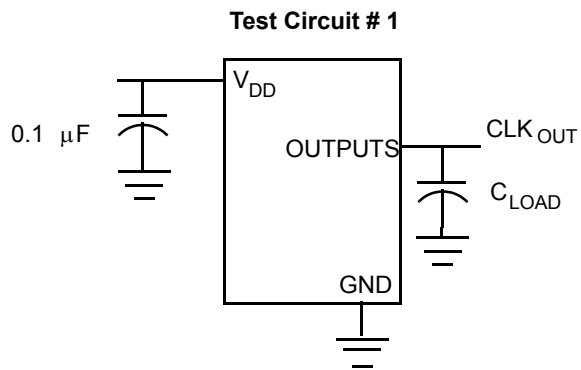
### Input-Output Propagation Delay



### Device-Device Skew

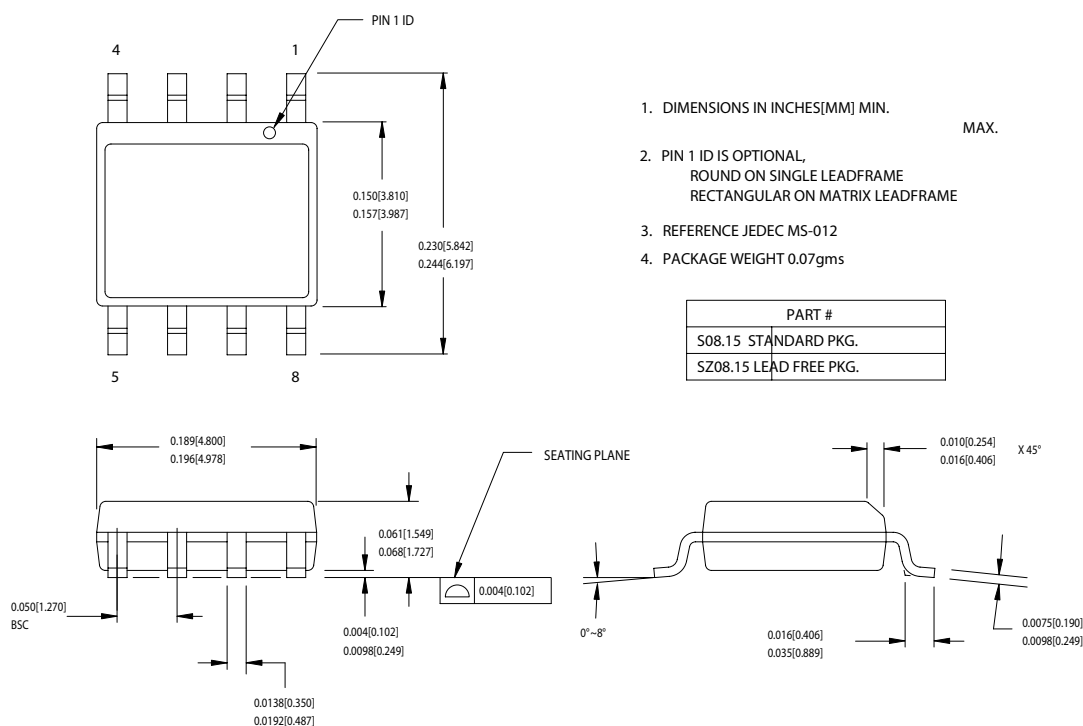


## Test Circuits



**Ordering Information**

Ordering Code	Package Type	Operating Range
CY2300SC	8-pin 150-mil SOIC	Commercial
CY2300SC	8-pin 150-mil SOIC - Tape and Reel	Commercial
CY2300SI	8-pin 150-mil SOIC	Industrial
CY2300SI	8-pin 150-mil SOIC - Tape and Reel	Industrial
<b>Lead Free</b>		
CY2300SXC	8-pin 150-mil SOIC	Commercial
CY2300SXCT	8-pin 150-mil SOIC - Tape and Reel	Commercial
CY2300SXI	8-pin 150-mil SOIC	Industrial
CY2300SXIT	8-pin 150-mil SOIC - Tape and Reel	Industrial

**Package Drawing and Dimensions**
**8-lead (150-Mil) SOIC S8**


51-85066-C

Document Title: CY2300 Phase-Aligned Clock Multiplier  
Document Number: 38-07252

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110517	01/07/02	SZV	Change from Spec number: 38-01039 to 38-07252
*A	121854	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*B	246829	See ECN	RGL	Added Lead Free Devices