

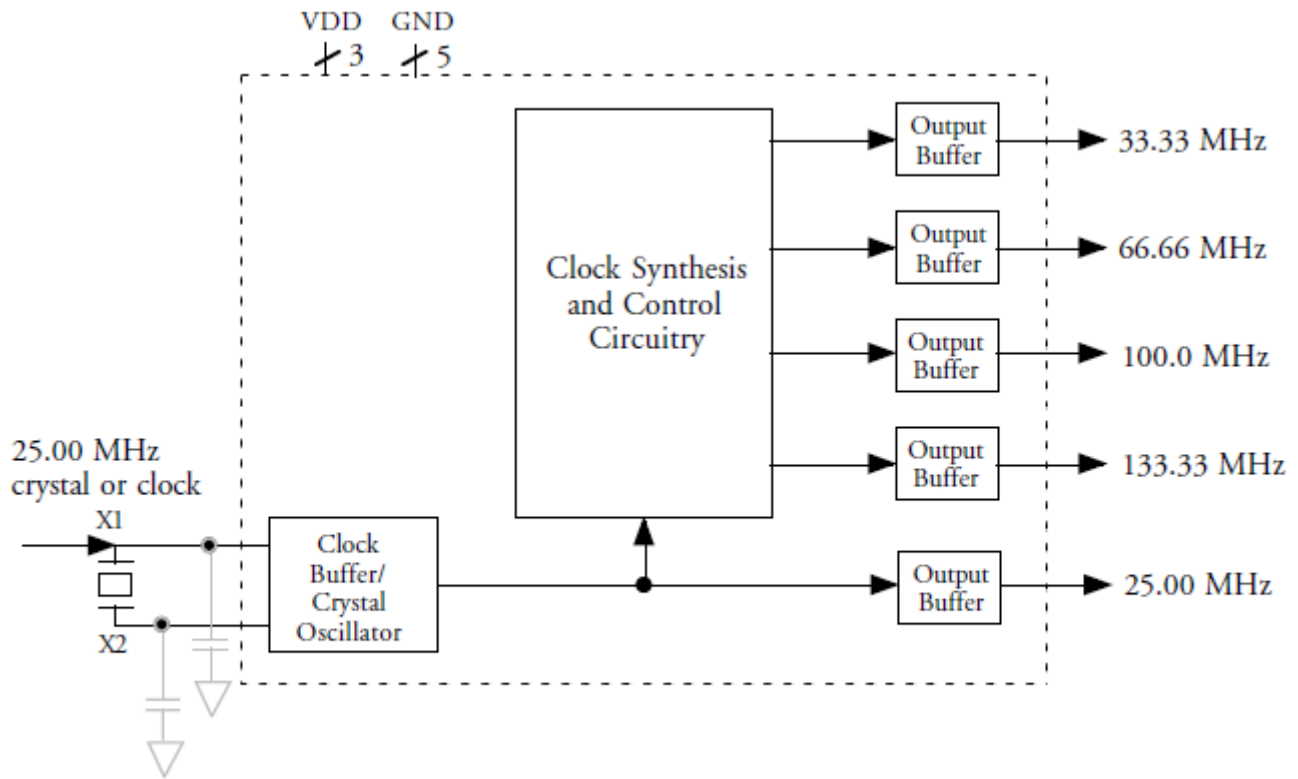
Description

The ICS650-11 is a low cost, low jitter, high performance clock synthesizer customized for BroadCom. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 25.0MHz clock or fundamental mode crystal input to produce multiple output clocks of 25.0MHz, 33.33MHz, 66.66MHz, 100.0MHz, and 133.33MHz. All output clocks are frequency locked together. The ICS650-11 outputs all have 0 ppm synthesis error.

Features

- Packaged in 20-pin narrow SSOP, Pb-free
- 25.00 MHz fundamental crystal or clock input
- Five fixed output clocks of 25.0 MHz, 33.33MHz, 66.66MHz, 100.0MHz, and 133.33MHz
- Zero ppm synthesis error in all clocks
- Ideal for BroadCom BCM5600/BCM5400 chipset
- Full CMOS output swing
- Advanced, low power, sub-micron CMOS process
- 3.0V to 5.5V operating voltage
- Industrial temperature range

Block Diagram



Pin Assignment

| | | | | | |
|------|---|----|----|---|---------|
| GND | □ | 1 | 20 | □ | DC |
| X2 | □ | 2 | 19 | □ | DC |
| X1 | □ | 3 | 18 | □ | 133.33M |
| VDD | □ | 4 | 17 | □ | 33.33M |
| GND | □ | 5 | 16 | □ | VDD |
| GND | □ | 6 | 15 | □ | VDD |
| DC | □ | 7 | 14 | □ | GND |
| DC | □ | 8 | 13 | □ | 25M |
| DC | □ | 9 | 12 | □ | 66.66M |
| 100M | □ | 10 | 11 | □ | GND |

20 pin (150 mil) SSOP

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | GND | Power | Connect to ground |
| 2 | X2 | XO | Crystal connection. Connect to a 25MHz crystal or leave unconnected for a clock input. |
| 3 | X1 | XI | Crystal connection. Connect to a 25MHz fundamental crystal or clock input. |
| 4 | VDD | Power | Connect to +3.3V or +5V. Must be same as other VDDs. |
| 5 | GND | Power | Connect to ground |
| 6 | GND | Power | Connect to ground |
| 7 | DC | — | Don't connect. Do not connect this pin to anything. |
| 8 | DC | — | Don't connect. Do not connect this pin to anything. |
| 9 | DC | — | Don't connect. Do not connect this pin to anything. |
| 10 | 100M | Output | 100.0MHz clock output. |
| 11 | GND | Power | Connect to ground |
| 12 | 66.66M | Output | 66.66MHz clock output. |
| 13 | 25M | Output | 25.0MHz clock output. |
| 14 | GND | Power | Connect to ground |
| 15 | VDD | Power | Connect to +3.3V or +5V. Must be same as other VDDs. |
| 16 | VDD | Power | Connect to +3.3V or +5V. Must be same as other VDDs. |
| 17 | 33.33M | Output | 33.33MHz clock output. |
| 18 | 133.33M | Output | 133.33MHz clock output. |
| 19 | DC | — | Don't connect. Do not connect this pin to anything. |
| 20 | DC | — | Don't connect. Do not connect this pin to anything. |

External Components

The ICS650-11 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between each VDD and GND on Pins 4 and 6, and Pins 16 and 14, as close to the ICS650-11 as possible. A series termination resistor of 33Ω may be used for each clock output. The 25.00 MHz crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = $(C_L - 6) \times 2$. So for a crystal with 16 pF load capacitance, two 20 pF caps should be used.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-11. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD (referenced to GND) | 7 V |
| All Inputs and Outputs (referenced to GND) | -0.5 V to VDD+0.5 V |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature (max. of 20 seconds) | 260°C |
| Ambient Operating Temperature | -40° to +85°C |

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|-----------------|--------------------------|---------|-------|---------|-------|
| Operating Voltage | VDD | | 3 | | 5.5 | V |
| Input High Voltage | V _{IH} | X1 pin only | VDD/2+1 | VDD/2 | | V |
| Input Low Voltage | V _{IL} | X1 pin only | | VDD/2 | VDD/2-1 | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | | 0.4 | V |
| Output High Voltage, CMOS level | V _{OH} | I _{OH} = -8 mA | VDD-0.4 | | | V |
| Operating Supply Current | IDD | No load | | 35 | | mA |
| Short Circuit Current | | Each output | | ±50 | | mA |

AC Electrical Characteristics

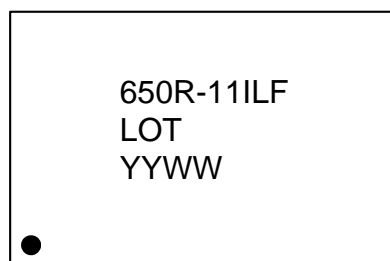
Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------|------------------------|------|--------|------|-------|
| Input Frequency | f _{IN} | | | 25.000 | | MHz |
| Output Clock Rise Time | | 0.8 to 2.0V | | | 1.5 | ns |
| Output Clock Fall Time | | 2.0 to 0.8V | | | 1.5 | ns |
| Output Clock Duty Cycle | | At VDD/2, except 25MHz | 45 | 50 | 55 | % |
| Frequency Error | | All clocks | | | 0 | ppm |
| Absolute Jitter, Short-Term | | Variation from mean | | 175 | | ps |

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 135 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 93 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 78 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 60 | | °C/W |

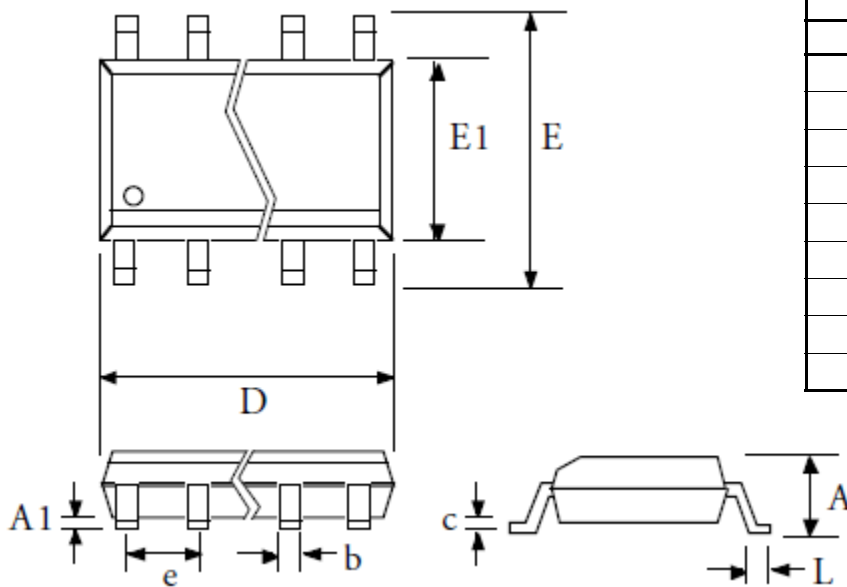
Marking Diagram



Notes:

1. "LOT" denotes lot number.
2. "YYWW" denotes the date code.
3. "I" denotes industrial grade.
4. "LF" denotes RoHS compliant package.
5. Bottom marking: country of origin.

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)



| Symbol | Millimeters | | Inches | |
|--------|-------------|-------|-------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.102 | 0.254 | 0.004 | 0.010 |
| b | 0.203 | 0.305 | 0.008 | 0.012 |
| c | 0.191 | 0.254 | 0.007 | 0.010 |
| D | 8.560 | 8.738 | 0.337 | 0.344 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| E | 5.791 | 6.198 | 0.228 | 0.244 |
| E1 | 3.810 | 3.988 | 0.150 | 0.157 |
| L | 0.406 | 1.270 | 0.016 | 0.050 |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|-------------|---------------|
| 650R-11ILF | see page 5 | Tubes | 20-pin SSOP | -40 to +85° C |
| 650R-11ILFT | | Tape and Reel | 20-pin SSOP | -40 to +85° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|--|
| D | 01/23/13 | D. Chan | 1. Updated datasheet to current IDT template. 2. Added marking diagram. |
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