



**FEATURES:**

- 5Ω bi-directional switches connect inputs to outputs
- Pin Compatibility with QS3245
- 250ps Propagation Delay
- Undershoot Clamp Diodes on all Switch and Control Inputs
- LVTTTL-Compatible Control Inputs
- Available in SOIC and QSOP Packages

**APPLICATIONS:**

- 3.3V to 2.5V Voltage Translation
- 2.5V to 1.8V Voltage Translation
- PCI Bus Isolation Hot Swap

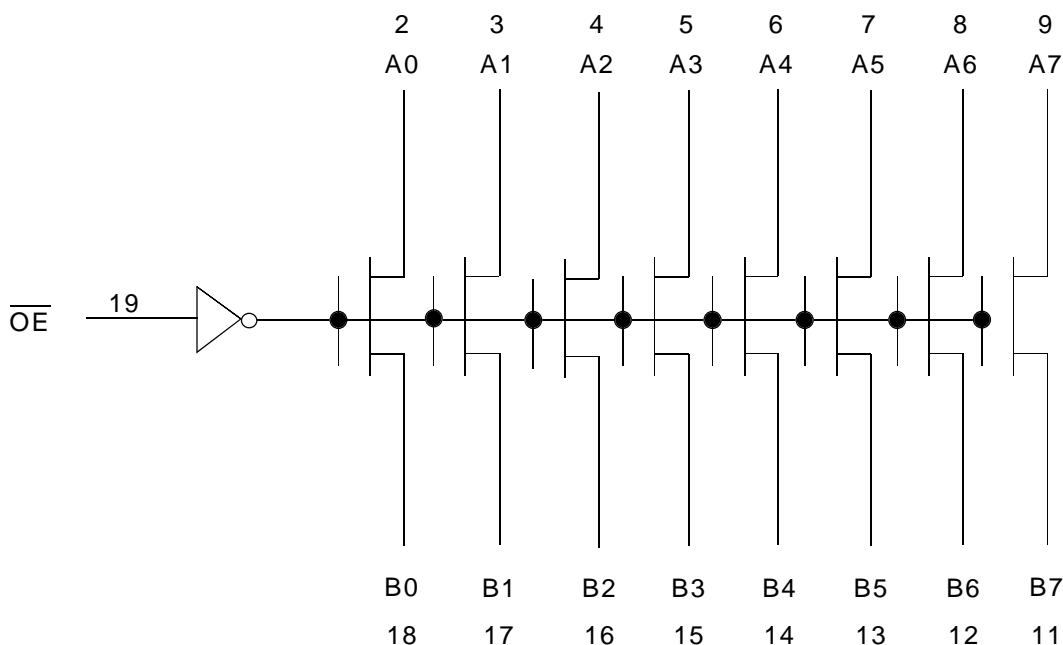
**DESCRIPTION:**

The QS3V245 is an 8-bit high speed bus switch controlled by LVTTTL-compatible active low enable signal. When closed, the switches exhibit near zero propagation delay without generating additional ground bounce or switching noise.

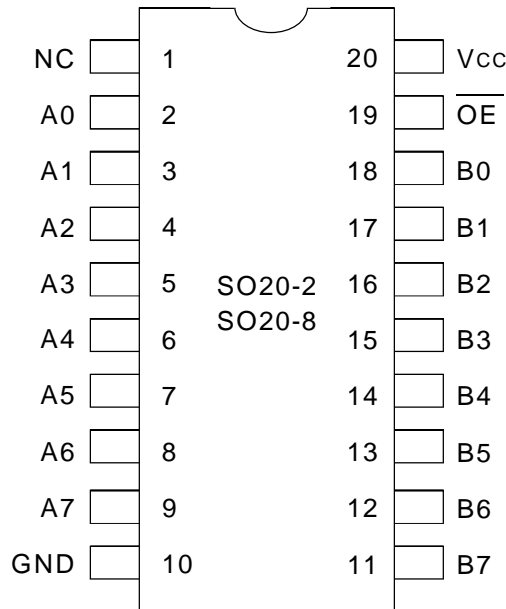
The QS3V245 is specially designed for direct interface between 3.3V and 2.5V devices without any external components. When operating from a 3.3V supply, the logic high level at the switch output is clamped to 2.5V when the switch input signal exceeds 2.5V. This device can be used for switching 2.5V buses without signal attenuation. The ON resistance at 3.3V Vcc is less than 5Ω typical, providing near zero propagation delay through the switch. Absence of DC path from switch I/O pins to Vcc or ground makes QS3V245 an ideal device for hot swapping applications.

The QS3V245 is characterized for operation from -40°C to +85°C.

**FUNCTIONAL BLOCK DIAGRAM**



## PIN CONFIGURATION



SOIC/ QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Supply Voltage to Ground	- 0.5 to 4.6	V
$V_S$	DC Switch Voltage	- 0.5 to 4.6	V
$V_{IN}$	DC Input Voltage	- 0.5 to 4.6	V
	AC Input Voltage (For a pulse width $\leq 20$ ns)	- 3	V
	DC Output Current Max. Sink Current/Pin	120	mA
	Maximum Power Dissipation	0.5	W
TSTG	Storage Temperature	-65 to 150	$^{\circ}C$

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.

## CAPACITANCE (TA = +25 $^{\circ}C$ , f = 1MHz, VIN = 0V, VOUT = 0V)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
$C_{IN}$	Control Inputs		4	6	pF
$C_{I/O}$	Quickswitch Channels	Switch OFF	5	7	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable
An	Data I/Os
Bn	Data I/Os

## FUNCTION TABLE (1)

$\overline{OE}$	Outputs
H	Disconnected
L	An = Bn

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

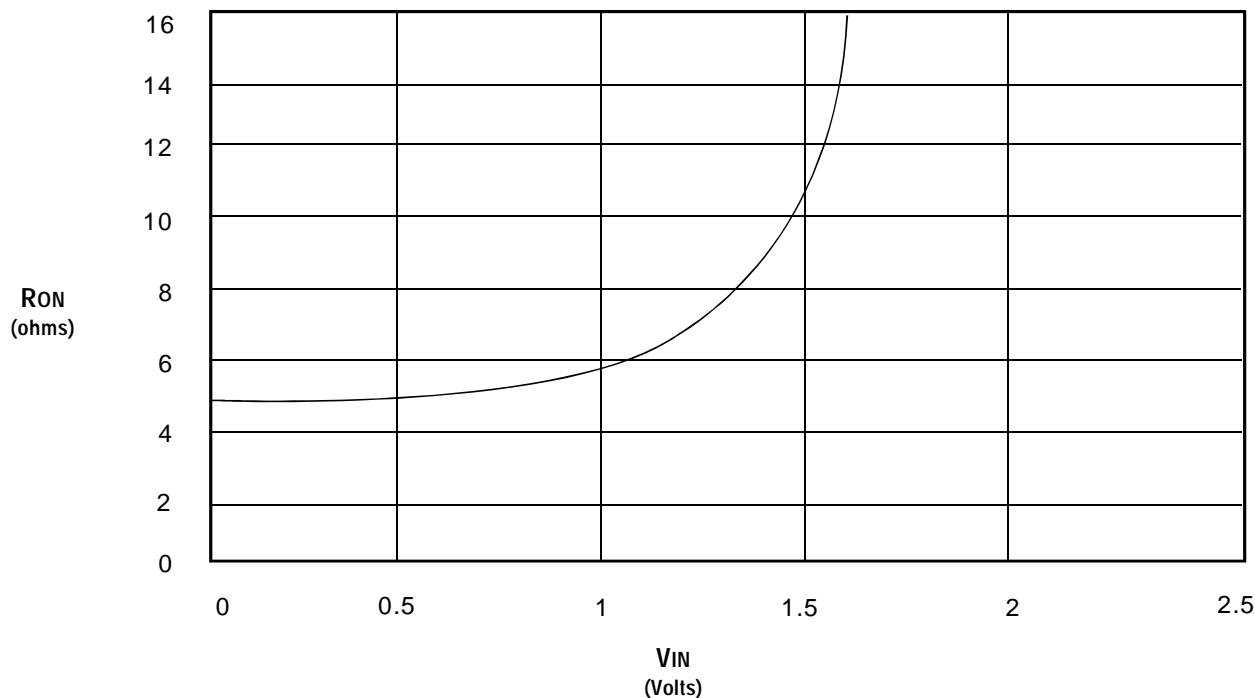
Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
$V_{IL}$	Input LOW Voltage Level	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$I_{IN}$	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	—	1	$\mu\text{A}$
$I_{OZ}$	Off-State Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$ , Switches OFF	—	0.001	1	$\mu\text{A}$
$R_{ON}$	Switch ON Resistance	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 8\text{mA}$	—	5	7	$\Omega$
		$V_{CC} = \text{Min.}, V_{IN} = 1.7\text{V}, I_{ON} = 8\text{mA}$	—	15	20	$\Omega$
		$V_{CC} = 2.3\text{V}, V_{IN} = 0\text{V}, I_{ON} = 8\text{mA}$	—	7	—	$\Omega$
		$V_{CC} = 2.3\text{V}, V_{IN} = 1.3\text{V}, I_{ON} = 8\text{mA}$	—	25	—	$\Omega$
$V_P$	Pass Voltage <sup>(2)</sup>	$V_{IN} = V_{CC} = 3.3\text{V}, I_{OUT} = -5\mu\text{A}$	2.5	2.7	2.9	V
		$V_{IN} = V_{CC} = 2.5\text{V}, I_{OUT} = -5\mu\text{A}$	—	1.8	—	V

OSlink

**NOTES:**

1. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
2. Pass voltage is guaranteed, but not production tested.

### TYPICAL ON RESISTANCE vs $V_{IN}$ AT $V_{CC} = 3.3\text{V}$



## OUTPUT DRIVE CHARACTERISTICS

TA = - 40°C to +85°C, VCC = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Max.	Unit
I <sub>CCQ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub> , f = 0	—	3	μA
ΔI <sub>CC</sub>	Power Supply Current <sup>(2)</sup> per Input HIGH	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3V or V <sub>CC</sub> , f = 0 per Control Input	—	50	μA
I <sub>CCD</sub>	Dynamic Power Supply Current per MHz <sup>(3)</sup>	V <sub>CC</sub> = Max., A and B Pins Open, Control Input Toggling @ 50% Duty Cycle	—	0.15	mA/MHz

OSlink

### NOTES:

- For conditions shown in Min. and Max., use the appropriate values specified under DC Specifications.
- Per TTL driven input (V<sub>IN</sub> = 3V, Control Inputs only). A and B pins do not contribute to I<sub>CC</sub>.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed, but not production tested.

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

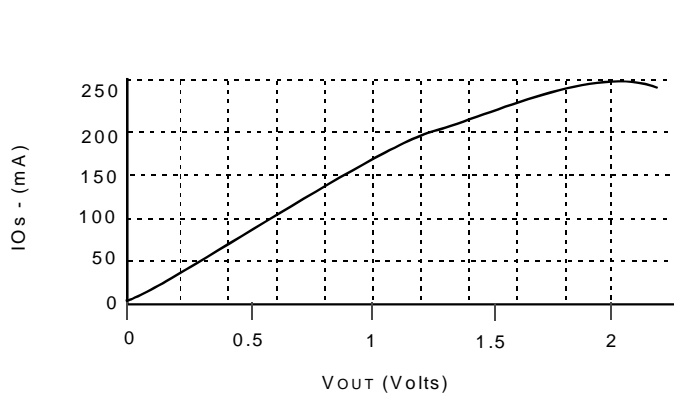
TA = - 40°C to +85°C, VCC = 3.3V ± 0.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Data Propagation Delay <sup>(2, 3)</sup> An to/from Bn	—	—	0.25	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Switch Turn-On Delay $\overline{OE}$ to An/Bn	0.5	—	6.5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Switch Turn-Off Delay <sup>(2)</sup> $\overline{OE}$ to An/Bn	0.5	—	4	ns

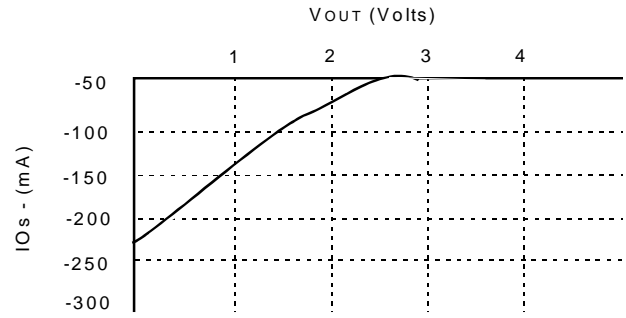
### NOTES:

- See test circuits and waveforms. Minimums guaranteed, but not production tested.
- This parameter is guaranteed, but not production tested.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance, of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C<sub>L</sub> = 30pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## OUTPUT VI CHARACTERISTICS

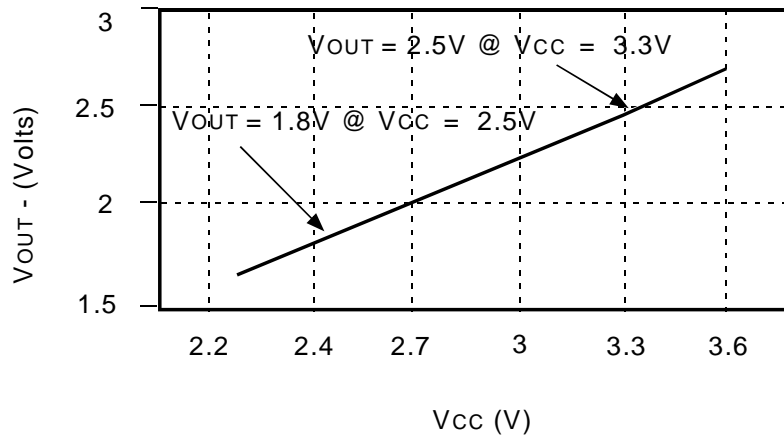


Outputs Low Characteristic

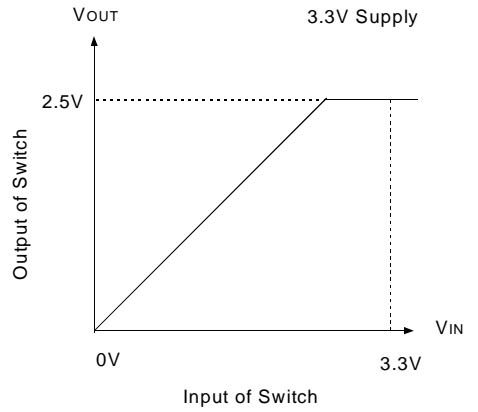
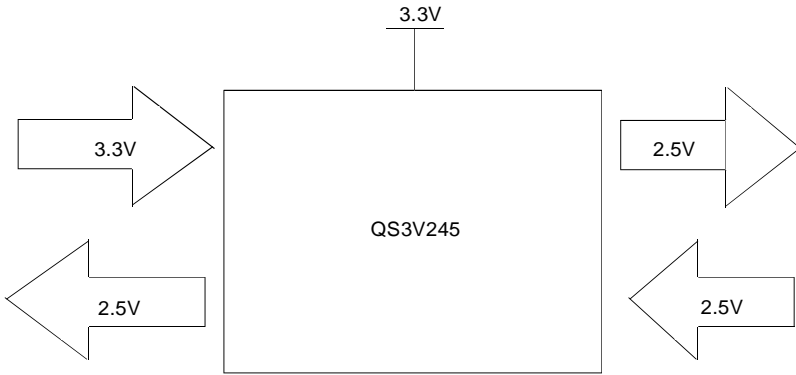


Outputs High Characteristic

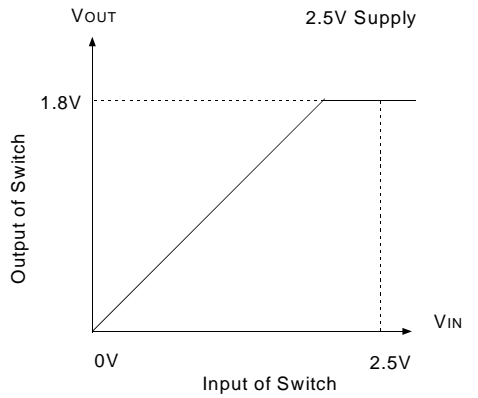
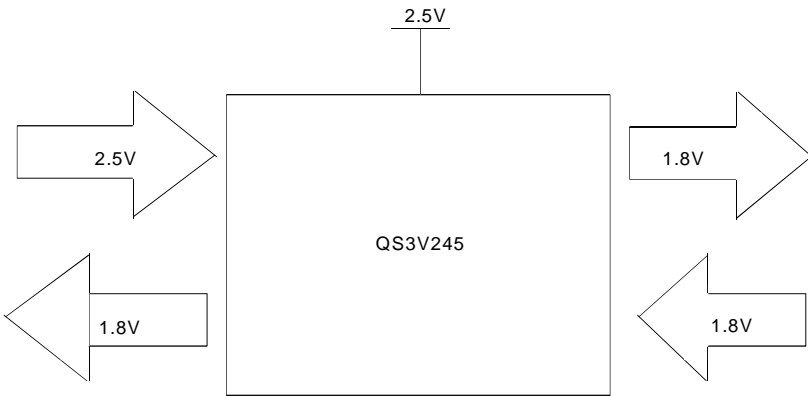
## PASS VOLTAGE vs $V_{CC}$



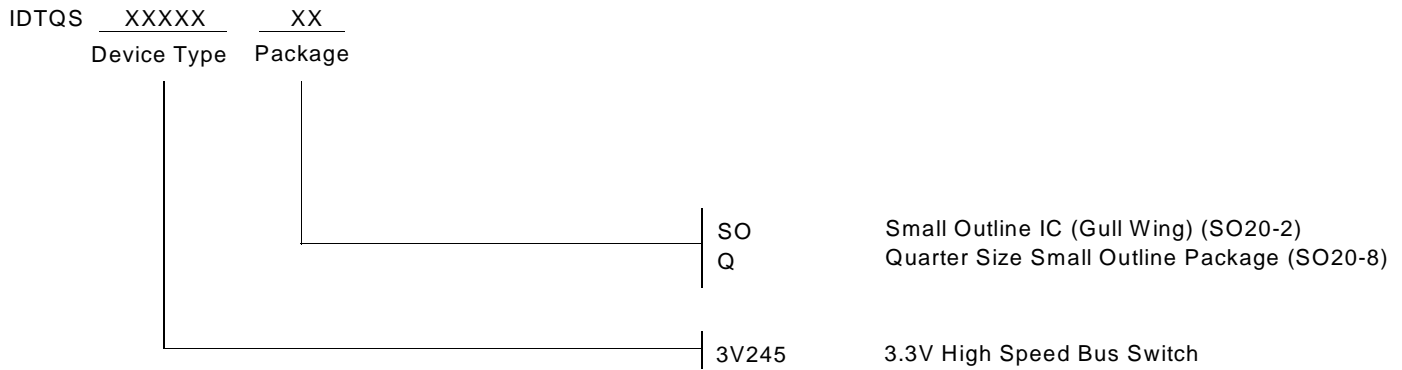
### 3.3V TO 2.5V VOLTAGE TRANSLATION



### 2.5V TO 1.8V VOLTAGE TRANSLATION



## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**

2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**

800-345-7015 or 408-727-6116  
fax: 408-492-8674  
[www.idt.com](http://www.idt.com)\*

*\*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*

The IDT logo is a registered trademark of Integrated Device Technology, Inc.  
QUICKSWITCH is a registered trademark of Integrated Device Technology, Inc.