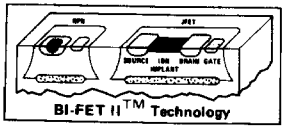
National Semiconductor



LF400A/LF400
Fast-Settling JFET-Input Operational Amplifier

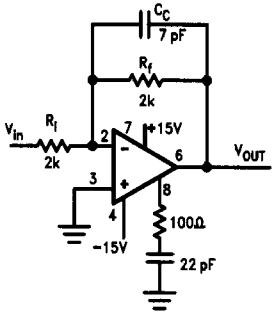
General Description

The LF400 is a fast-settling (under 400 ns to 0.01% for a 10V output step) Bi-FET operational amplifier. Features include 16 MHz bandwidth, 60V/μs inverting slew rate, low input offset voltage (0.5 mV for the LF400A at 25°C), and adjustable output current limit, enabling the amplifier to drive 600Ω loads.

Applications

- DAC output amplifiers
- High speed ramp generators
- Fast buffers
- Sample-and-holds
- Fast integrators
- Piezoelectric transducer signal conditioners

Typical Connection



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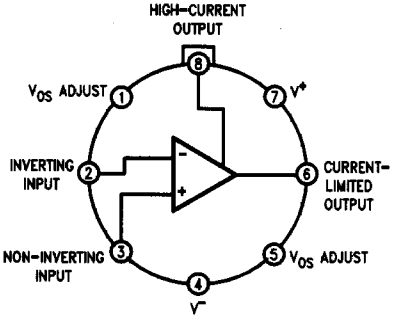
Connection Diagram



Note: Pin 4 connected to case.

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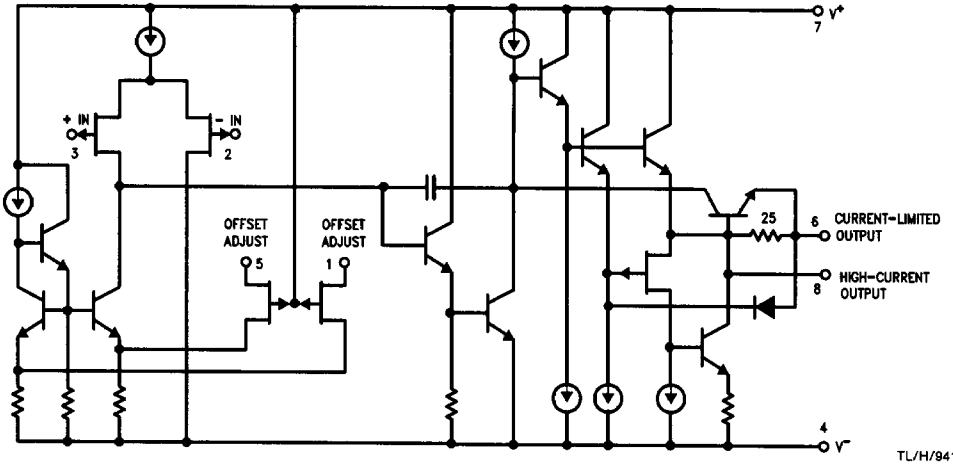
Top View

Order Number LF400ACH, LF400CH, LF400AMH or LF400MH
See NS Package Number H08B

Simplified Schematic



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±32V
Input Voltage Range (Note 3)	±16V
Output Short Circuit Duration (Pin 6)	Continuous
Power Dissipation (Note 4) H package	500 mW
Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Susceptibility (Note 9)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF400AMH, LF400MH	$-55°C \le T_A \le +125°C$
LF400ACH, LF400CH	$0°C \le T_A \le +70°C$
Positive Supply Voltage	+10V to +16V
Negative Supply Voltage	−10V to −16V

AC Electrical Characteristics (LF400ACH, LF400CH)

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified.
Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX}; other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter	Conditions	LF400ACH			LF400CH			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
t_s	Settling Time to 0.01% to 0.10%	See *Figure 1* See *Figure 1*	365 200			365 200			ns ns
GBW	Minimum Gain Bandwidth Product	$A_V = +1$, C_L = 10 pF	16	14		16	14		MHz
SR	Minimum Slew Rate	$A_V = +1$, C_L = 10 pF	30	27		30	27		V/μs
		$A_V = -1$, C_L = 10 pF	60			60			V/μs
ϕ	Phase Margin	$A_V = +1$, C_L = 10 pF	60			60			Degrees
e_n	Input Noise Voltage	f = 1 kHz, R_S = 100Ω Broadband, R_S = 100Ω, 10 Hz to 10 kHz	23 2.3			23 2.3			$nV/\sqrt{Hz}$ μV rms
i_n	Input Noise Current	f = 1 kHz Broadband 10 Hz to 10 kHz	0.01 1.0			0.01 1.0			$pA/\sqrt{Hz}$ pA rms
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = -1$, R_L = 10k	0.002			0.002			%
C_{IN}	Input Capacitance		7			7			pF

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DC Electrical Characteristics (LF400ACH, LF400CH)

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified.
Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX}; other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter		Conditions		LF400ACH Typical (Note 6)	LF400ACH Tested Limit (Note 7)	LF400ACH Design Limit (Note 8)	LF400CH Typical (Note 6)	LF400CH Tested Limit (Note 7)	LF400CH Design Limit (Note 8)	Units
V_{OS}	Maximum Input Offset Voltage		V_{CM} = 0V,	T_J = 25°C		±0.5			±3.0		mV
			R_S = 0, R_L = ∞	T_J = 70°C		±2.0			±5.0		mV
I_{OS}	Maximum Input Offset Current		V_{CM} = 0V (Note 5)		±50	±100 **±2.5**		±50	±100 **±2.5**		pA nA
I_B	Maximum Input Bias Current		V_{CM} = 0V (Note 5)		100	200 **26**		100	200 **26**		pA nA
R_{IN}	Input Resistance				10^{11}			10^{11}			Ω
V_{CM}	Input Common-Mode Voltage Range				−12 to +14	±11		−12 to +14	±11		V
A_{VOL}	Minimum Large Signal Voltage Gain	Using Pin 6	V_O = ±10V, R_L = 2 kΩ		300	100		300	100		V/mV
		Using Pin 8	V_O = ±10V, R_L = 600Ω		280	100		280	100		V/mV
V_O	Minimum Output Voltage Swing	Using Pin 6	R_L = 2 kΩ		±12.5	±12.0		±12.5	±12.0		V
		Using Pin 8	R_L = 600Ω		±12.0	±11.0		±12.0	±11.0		V
I_{SC}	Output Short Circuit Current	MIN Using Pin 6 MAX Using Pin 6 MIN Using Pin 8	Pulse Test		25	 15 45 100		25	 15 45 100		mA mA mA mA
R_O	Output Resistance	Using Pin 6	Open Loop, DC		75			75			Ω
		Using Pin 8	Open Loop, DC		50			50			Ω
CMRR	Minimum DC Common Mode Rejection Ratio		−11V ≤ V_{IN} ≤ +11V		100	90		100	80		dB
PSRR	Minimum DC Power Supply Rejection Ratio		+10V ≤ V^+ ≤ +15V, −15V ≤ V^- ≤ −10V, V_{CM} = 0V		100	90		100	80		dB
I_S	Maximum Supply Current		V_O = 0V, R_L = ∞		11.0	13.0		11.0	13.0		mA

AC Electrical Characteristics (LF400AMH, LF400MH)

The following specifications apply for $V^+ = +15V$, $V^- = -15V$, and $T_J = 25°C$ unless otherwise specified.
Tested Limits in Boldface apply for $T_J = -55°C$ to $+125°C$

Symbol	Parameter	Conditions	LF400AMH			LF400MH			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
t_s	Settling Time to 0.01% to 0.10%	See *Figure 1* See *Figure 1*	365 200			365 200			ns ns
GBW	Minimum Gain Bandwidth Product	$A_V = +1$, $C_L = 10$ pF	16	14 **10**		16	14 **10**		MHz MHz
SR	Minimum Slew Rate	$A_V = +1$, $C_L = 10$ pF	30	**27**		30	**27**		V/μs
		$A_V = -1$, $C_L = 10$ pF	60			60			V/μs
ϕ	Phase Margin	$A_V = +1$, $C_L = 10$ pF	60			60			Degrees
e_n	Input Noise Voltage	f = 1 kHz, $R_S = 100\Omega$ Broadband, $R_S = 100\Omega$, 10 Hz to 10 kHz	23 2.3			23 2.3			nV/√Hz μV rms
i_n	Input Noise Current	f = 1 kHz Broadband 10 Hz to 10 kHz	0.01 1.0			0.01 1.0			pA/√Hz pA rms
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = -1$, $R_L = 10k$	0.002			0.002			%
C_{IN}	Input Capacitance		7			7			pF

DC Electrical Characteristics (LF400AMH, LF400MH)

The following specifications apply for $V^+ = +15V$, $V^- = -15V$, and $T_J = 25°C$ unless otherwise specified.
Tested Limits in Boldface apply for $T_J = -55°C$ to $+125°C$.

Symbol	Parameter		Conditions		LF400AMH			LF400MH			Unit
					Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage		$V_{CM} = 0V$, $R_S = 0$, $R_L = \infty$	$T_J = 25°C$		±0.5			±3.0		mV
						±2.0			**±5.0**		mV
I_{OS}	Maximum Input Offset Current		$V_{CM} = 0V$ (Note 5)		±50	±100 **±15**		±50	±100 **±25**		pA nA
I_B	Maximum Input Bias Current		$V_{CM} = 0V$ (Note 5)		100	200 **35**		100	200 **50**		pA nA
R_{IN}	Input Resistance				10^{11}			10^{11}			Ω
V_{CM}	Input Common-Mode Voltage Range				−12 to +14	**±11**		−12 to +14	**±11**		V
A_{VOL}	Minimum Large Signal Voltage Gain	Using Pin 6	$V_O = \pm 10V$, $R_L = 2k\Omega$		300	**100**		300	**50**		V/mV
		Using Pin 8	$V_O = \pm 10V$, $R_L = 600\Omega$		280	**100**		280	**50**		V/mV

DC Electrical Characteristics (LF400AMH, LF400MH)

The following specifications apply for $V^+ = +15V$, $V^- = -15V$, and $T_J = 25°C$ unless otherwise specified.
Tested Limits in Boldface apply for $T_J = -55°C$ to $+125°C$. (Continued)

Symbol	Parameter		Conditions	LF400AMH			LF400MH			Units
				Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_O	Minimum Output Voltage Swing	Using Pin 6	$R_L = 2\,k\Omega$	±12.5	±12.0 **±11.5**		±12.5	±12.0 **±11.5**		V V
		Using Pin 8	$R_L = 600\Omega$	±12.0	**±11.0**		±12.0	**±11.0**		V
I_{SC}	Output Short Circuit Current	MIN Using Pin 6 MAX Using Pin 6 MIN Using Pin 8	Pulse Test	25	**15** **45** **100**		25	**15** **45** **100**		mA mA mA mA
R_O	Output Resistance	Using Pin 6	Open Loop, DC	75			75			Ω
		Using Pin 8	Open Loop, DC	50			50			Ω
CMRR	Minimum DC Common Mode Rejection Ratio		$-11V \le V_{IN} \le +11V$	100	90 **80**		100	80 **75**		dB dB
PSRR	Minimum DC Power Supply Rejection Ratio		$+10V \le V^+ \le +15V$, $-15V \le V^- \le -10V$, $V_{CM} = 0V$	100	90 **85**		100	80 **75**		dB dB
I_S	Maximum Supply Current		$V_O = 0V$, $R_L = \infty$	11.0	13.0 **13.0**		11.0	13.0 **15.0**		mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to ground.

Note 3: Unless otherwise specified, the Absolute Minimum Input Voltage is equal to the negative power supply voltage.

Note 4: The maximum power dissipation must be derated at elevated temperatures as is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. θ_{JA} for the LF400H is 150°C/W in free air, so a heat sink will generally be required when T_A is greater than about 70°C. θ_{JC} for the LF400H is 17°C/W, which dictates the use of a heat sink with θ_{CA} less than about 35°C/W when $T_A = +125°C$.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, input bias currents are measured at $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation P_D. Use of a heat sink is recommended when input bias current must be minimized.

Note 6: Typicals represent the most likely parametric norm.

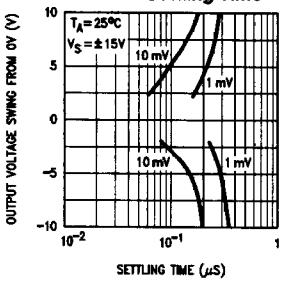
Note 7: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

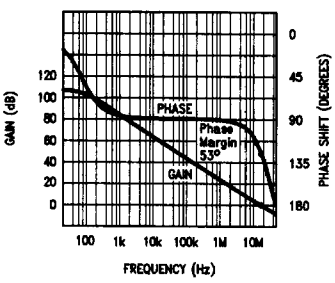
Note 9: Human body model, 100 pF discharged through a 1500Ω resistor.

Typical Performance Characteristics

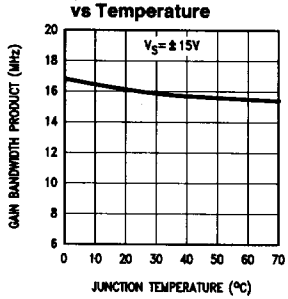
Inverter Settling Time



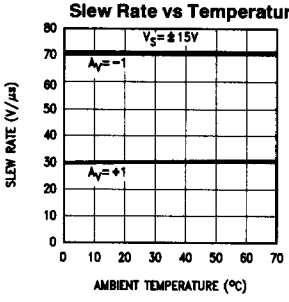
Bode Plot



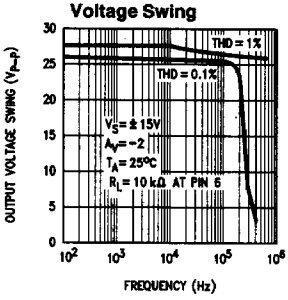
Gain Bandwidth vs Temperature



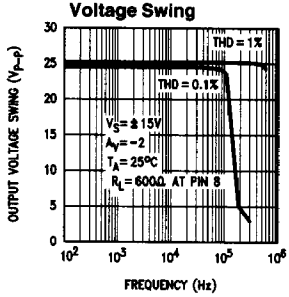
Slew Rate vs Temperature



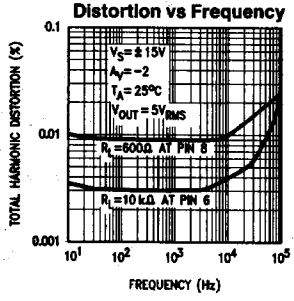
Undistorted Output Voltage Swing



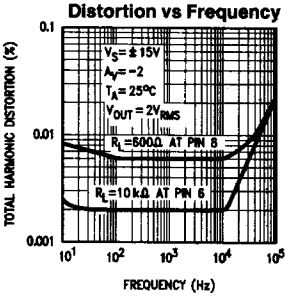
Undistorted Output Voltage Swing



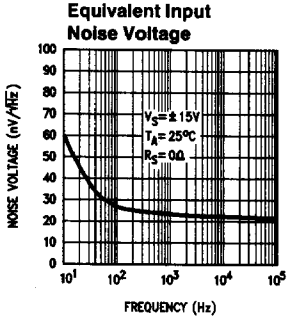
Distortion vs Frequency



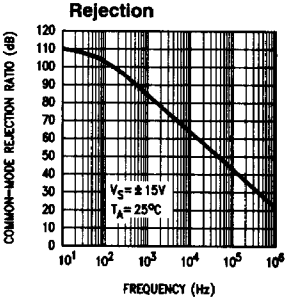
Distortion vs Frequency



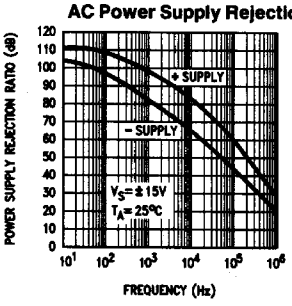
Equivalent Input Noise Voltage



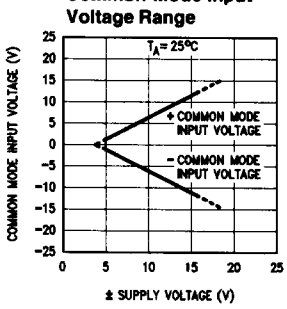
AC Common-Mode Rejection



AC Power Supply Rejection



Common-Mode Input Voltage Range



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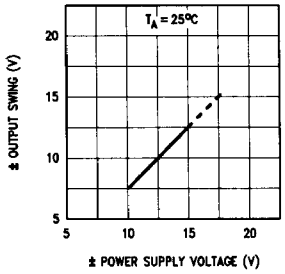
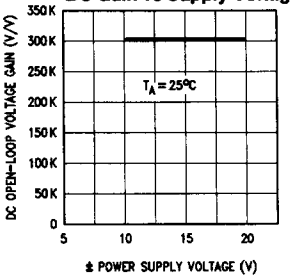
Typical Performance Characteristics (Continued)

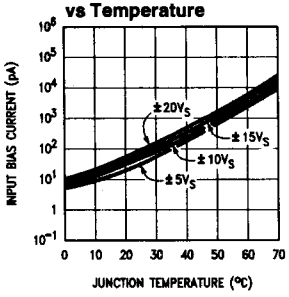
Output Voltage Swing vs Supply Voltage



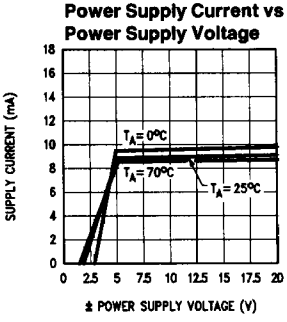
DC Gain vs Supply Voltage



Input Bias Current vs Temperature



Power Supply Current vs Power Supply Voltage



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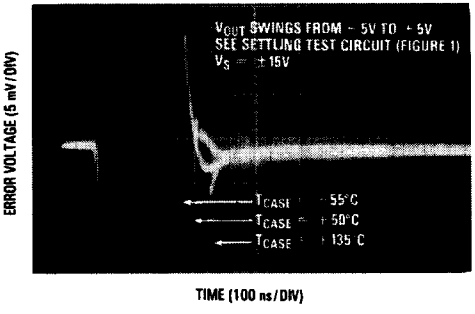
Settling Time—Positive Output Swing



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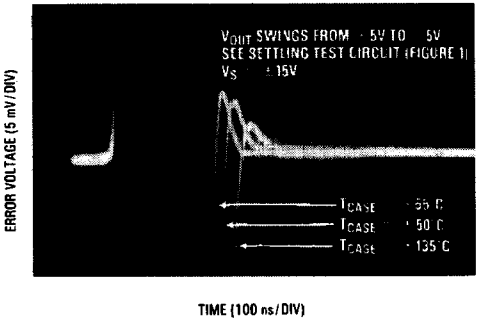
Settling Time—Negative Output Swing



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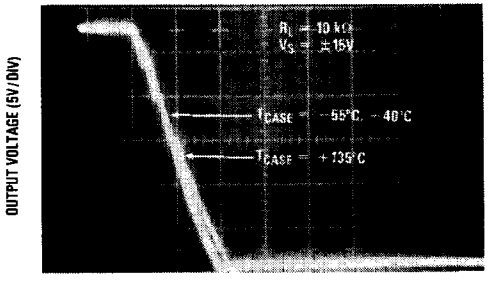
Step Response



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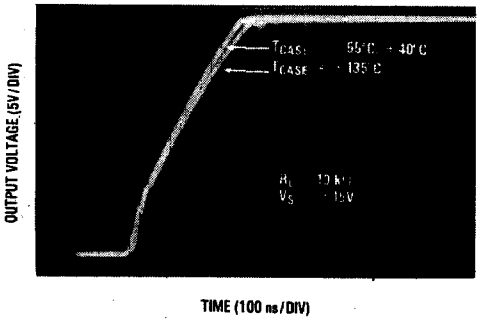
Typical Performance Characteristics (Continued)

Step Response



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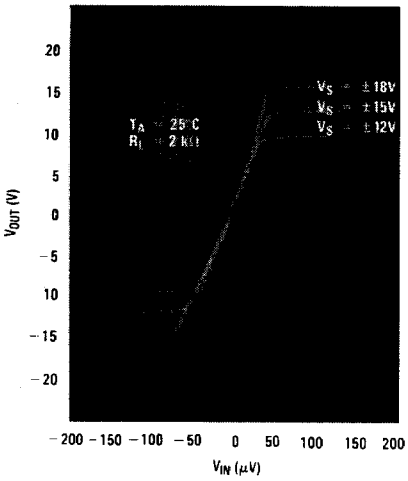
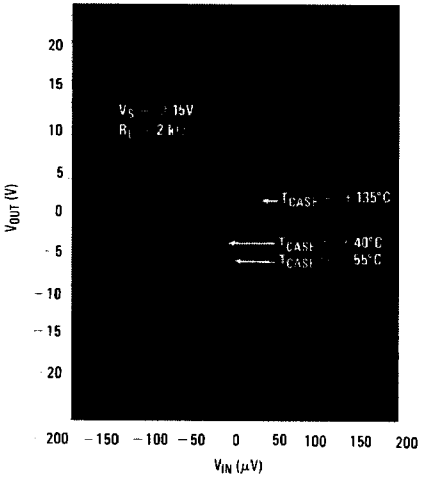
Voltage Transfer Characteristic



TL/H/9414–16

Voltage Transfer Characteristic



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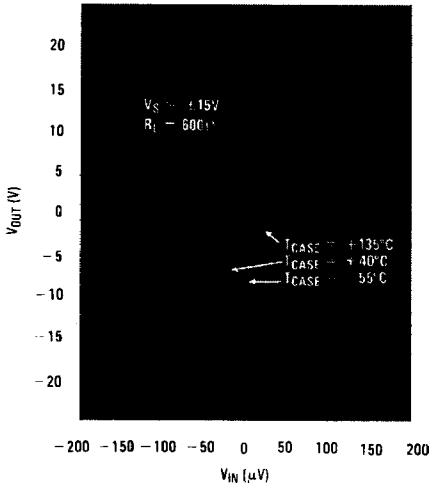

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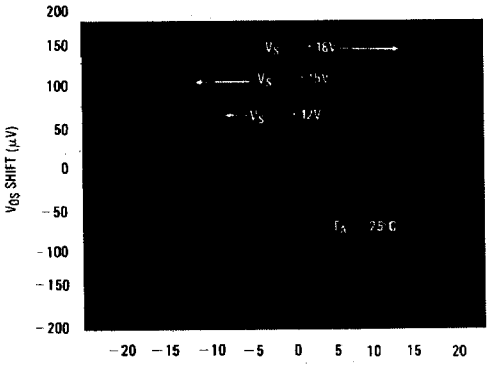
Typical Performance Characteristics (Continued)

Common—Mode Voltage Transfer Characteristic



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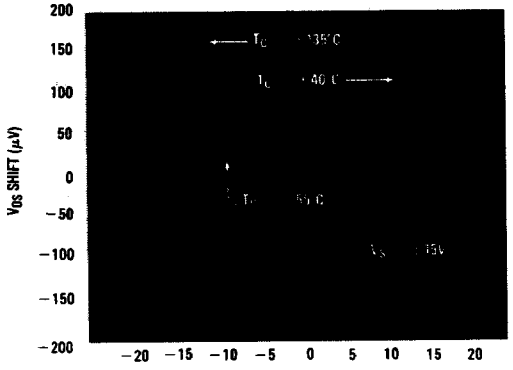

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Application Hints

The LF400 is a high-speed, low input bias current Bi-FET operational amplifier capable of settling to 0.01% of a 10V output swing in less than 400 ns. The rugged JFET inputs allow differential input voltages as high as 32V without a large increase in input current. However, the inputs should never be driven to voltages lower than the negative supply, as this can result in input currents large enough to damage the device. To prevent this from occurring when power is first applied, always turn the positive and negative power supplies on simultaneously, or turn the negative supply on first.

Exceeding the common-mode input range will not damage the device as long as the Absolute Maximum Ratings are not violated, but it will result in a high output voltage. Latching will not occur, however, and when the offending signal is removed the LF400 will recover quickly.

The nominal power supply voltage is ±15V, but the LF400 will operate satisfactorily from ±10V to ±16V. The LF400 is functional down to ±5V, but performance will be degraded. (See Typical Performance curves.)

Settling Time Considerations

The settling performance of any high-speed operational amplifier is highly dependent on the external components and circuit board layout. Capacitance between the amplifier summing junction and ground affects the closed-loop transfer function and should be minimized. The compensation capacitor C_C between the output and the inverting input should be carefully chosen to counteract the effect of the input capacitance. Since input capacitance is made up of several stray capacitances that are difficult to predict, the compensation capacitor will generally have to be determined empirically for best settling time. A good starting point is around 10 pF for $A_V = -1$.

Settling time may be verified using a circuit similar to the one in *Figure 1*. The LF400 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LF400's output voltage is equal to the input voltage, the voltage on the gate of Q1 will be zero. Any voltage appearing at this point will represent an error. The FET source follower output is observed on an oscilloscope, and the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (see oscilloscope photos of "Settling Time—Positive Output Swing" and "Settling Time—Negative Output Swing"). For a 10V input signal, settling time to 0.01% (1 mV) will occur when the displayed error is less than ½ mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LF400's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier will be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. Very few oscilloscopes are suitable for this sort of measurement. The signal generator used for set-

Application Hints (Continued)

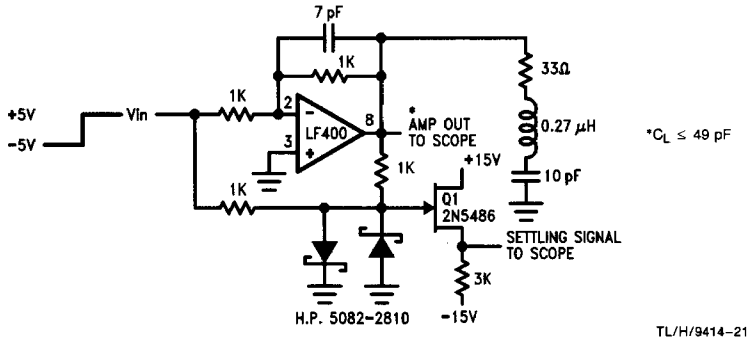

FIGURE 1. Simplified Settling Time Test Circuit (see Text)

tling time testing must be able to drive 50Ω with a very clean ±5V square wave. For more information on measuring settling time, see Application Note AN-428.

Output Compensation

When operating at very low temperatures, a compensation network should be added to the LF400's output. The 100Ω/22 pF network shown on the first page of this data sheet should be used when the junction temperature might reach 25°C (roughly 0°C ambient when the LF400 is "warmed up"). In applications where the device will be operating with a junction temperature near 0°C, the output RLC network in *Figure 1* should be used. This network will provide a small (about 20 ns) improvement in settling time at higher temperatures, as well.

Supply Bypassing

Power supply bypassing is extremely important for good high-speed performance. Ideally, multiple bypass capacitors as in *Figure 2* should be used. A 10 μF tantalum, a 2.2 μF ceramic, and a 0.47 μF ceramic work well. All bypass capacitor leads should be very short. For best results, the ground leads of the capacitors should be separated to reduce the inductance to ground. A ground plane layout approach will give the best results. For simplicity, bypass capacitors have been omitted from some of the schematics in this data sheet, but they should always be used.

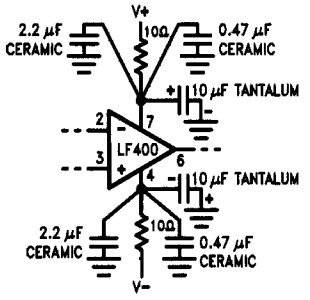

FIGURE 2. Power Supply Bypassing (see Text)

Output Drive and Current Limit

The LF400 can drive heavier resistive loads than most operational amplifiers. The output at pin 6 is internally current-limited when the voltage drop across the 25Ω output resistor reaches about 0.55V (I_{OUT} = 22 mA). When more output current is needed, pin 8 provides a means of increasing the maximum output current up to about 100 mA. A resistor may be connected from pin 8 to pin 6, paralleling the internal sense resistor and increasing the current limit threshold (*Figure 3*). Pins 6 and 8 may be shorted together to completely bypass the current limiting circuit. To avoid damaging the LF400, observe the power dissipation limitations mentioned in the Absolute Maximum Ratings and in Note 4.

The effective load impedance (including feedback resistance) should be kept above 500Ω for fastest settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1 kΩ to 2 kΩ range wherever practical. Avoid the use of inductive feedback resistors (some wirewounds for example) as these will degrade settling time.

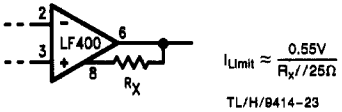

FIGURE 3. Increasing the current limit using pin 8. Current limit is now determined by R_X in parallel with the internal 25Ω sense resistor.

V_{OS} Adjustment

Offset voltage can be nulled using a 27k resistor and a 10k potentiometer connected to pins 1 and 5 as shown in *Figure 4a*. Bypassing the V_{OS} adjust pins with 0.1 μF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 1 and 5 can often be left open, but to minimize the possibility of noise pickup the unused V_{OS} trim pins should be connected to ground or V⁻.

Application Hints (Continued)

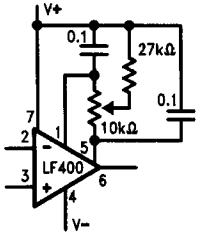

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FIGURE 4a. V_{OS} Adjust Circuit

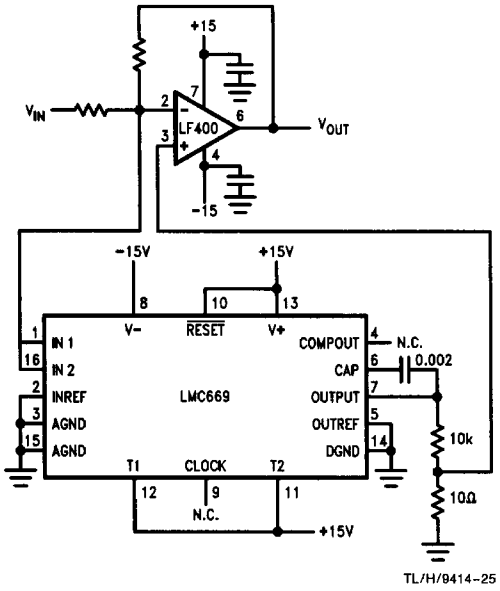

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FIGURE 4b. Automatic Offset Adjustment Using LMC669

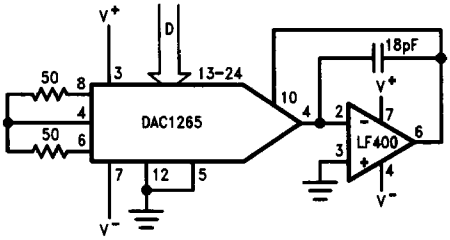
In very critical applications where a manual adjustment is impractical, the LMC669 Auto Zero circuit may be used to reduce the effective input offset voltage to around 5 μV as in *Figure 4b*. The LF400 will perform better than slower amplifiers in an auto zero loop, because its fast settling capability keeps its summing node voltage more stable. Therefore, the LMC669 is able to more accurately sample the summing node voltage before making an offset correction.

Input Bias Current

The JFET input stage of the LF400 ensures low input bias current (200 pA maximum) when the die is at room temperature, but this current approximately doubles for every 10°C increase in temperature. In applications that demand the lowest possible input bias current, a heat sink should be used with the LF400. "Press on" heat sinks from manufacturers such as Thermalloy and AAVID can reduce junction temperature by roughly 10°C to 40°C.

Typical Applications

High-Speed DAC with Voltage Output



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