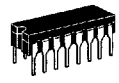
Quad Latch

MC10153

The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

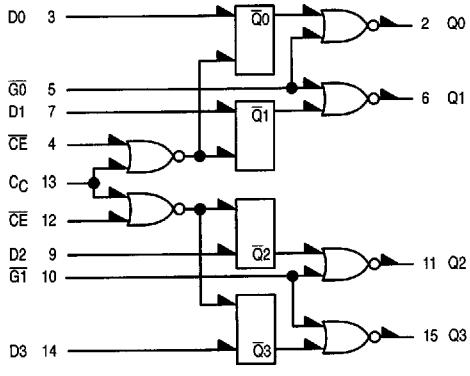


L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

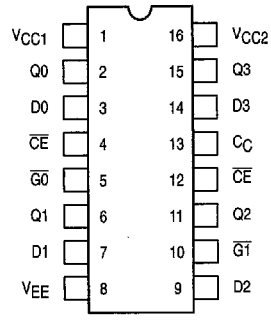
FN SUFFIX
PLCC
CASE 775–02

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	X	X	L
L	H	X	Q_n
L	L	L	L
L	L	H	H

$C = C_C + \overline{CE}$

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		83			75		83	mAdc
Input Current	I_{inH}	3		390			245		245	µAdc
		4		390			245		245	
		5		560			350		350	
		13		460			290		290	
	I_{inL}	3	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
		2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	
Output Voltage Logic 0	V_{OL}	2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
		2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	
		2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	
Threshold Voltage Logic 1	V_{OHA}	2	−1.080		−0.980			−0.910		Vdc
		2	−1.080		−0.980			−0.910		
		2	−1.080		−0.980			−0.910		
		2†	−1.080		−0.980			−0.910		
		2‡	−1.080		−0.980			−0.910		
		2‡	−1.080		−0.980			−0.910		
		2	−1.080		−0.980			−0.910		
		2	−1.080		−0.980			−0.910		
Threshold Voltage Logic 0	V_{OLA}	2		−1.655			−1.630		−1.595	Vdc
		2		−1.655			−1.630		−1.595	
		2		−1.655			−1.630		−1.595	
		2†		−1.655			−1.630		−1.595	
		2‡		−1.655			−1.630		−1.595	
		2‡		−1.655			−1.630		−1.595	
Switching Times (50Ω Load)										ns
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	
	t_{4-2+}	2	1.0	5.6	1.0	4.0	5.6	1.2	6.2	
	t_{5-2+}	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	
	t_{setup}	3	2.5		2.5	0.7		2.5		
	t_{hold}	3	1.5		1.5	0.7		1.5		
Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
Fall Time (20 to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)

‡ Data input at proper high/low level while clock pulse is high so that device latches ar proper high/low level for test. Levels are measured after device has latched.

* Latch set to zero state before test.

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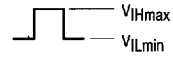
ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8		13			8	1, 16
Input Current		I_{inH}	3	3				8	1, 16
			4	4				8	1, 16
			5	5				8	1, 16
			13	13				8	1, 16
		I_{inL}	3		3			8	1, 16
Output Voltage	Logic 1	V_{OH}	2	3	4			8	1, 16
			2	3	13			8	1, 16
Output Voltage	Logic 0	V_{OL}	2		3,13			8	1, 16
			2	3,5	13			8	1, 16
			2		3,4			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2	3	4		5	8	1, 16
			2		4	3		8	1, 16
			2	3	4			8	1, 16
			2†	3				8	1, 16
			2‡					8	1, 16
			2‡					8	1, 16
			2	3			4	8	1, 16
			2	3			13	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2	3	4	5		8	1, 16
			2		4		3	8	1, 16
			2		4			8	1, 16
			2†					8	1, 16
			2‡	3				8	1, 16
			2‡	3			13	8	1, 16
Switching Times	(50Ω Load)			+1.11 V		Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay		t_{3+2+}	2			3	2	8	1, 16
		t_{4-2+}	2	3*		4	2	8	1, 16
		t_{5-2+}	2			5	2	8	1, 16
		t_{setup}	3			3	2	8	1, 16
		t_{hold}	3			3	2	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			3	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			3	2	8	1, 16

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)



‡ Data input at proper high/low level while clock pulse is high so that device latches ar proper high/low level for test. Levels are measured after device has latched.

* Latch set to zero state before test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.