National Semiconductor

# 54F/74F377
# Octal D Flip-Flop with Clock Enable

## General Description

The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

## Features

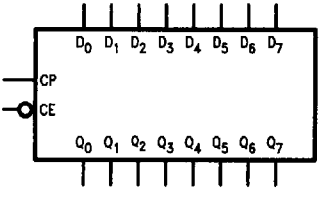
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'F273 for master reset version
- See 'F373 for transparent latch version
- See 'F374 for TRI-STATE® version
- Guaranteed 4000V minimum ESD protection

## Ordering Code: See Section 11

| Commercial | Military | Package Number | Package Description |
|---|---|---|---|
| 74F377PC | | N20A | 20-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F377DM (QB) | J20A | 20-Lead Ceramic Dual-In-Line |
| 74F377SC (Note 1) | | M20B | 20-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74F377SJ (Note 1) | | M20D | 20-Lead (0.300" Wide) Molded Small Outline, EIAJ |
| | 54F377FM (QB) | W20A | 20-Lead Cerpack |
| | 54F377LM (QB) | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

## Logic Symbols

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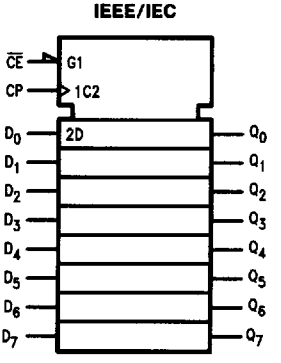


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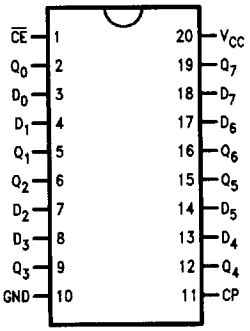
## Connection Diagrams

**Pin Assignment for DIP, SOIC and Flatpak**

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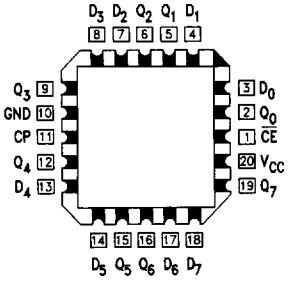
**Pin Assignment for LCC**

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## Unit Loading/Fan Out: See Section 2 for U.L. definitions

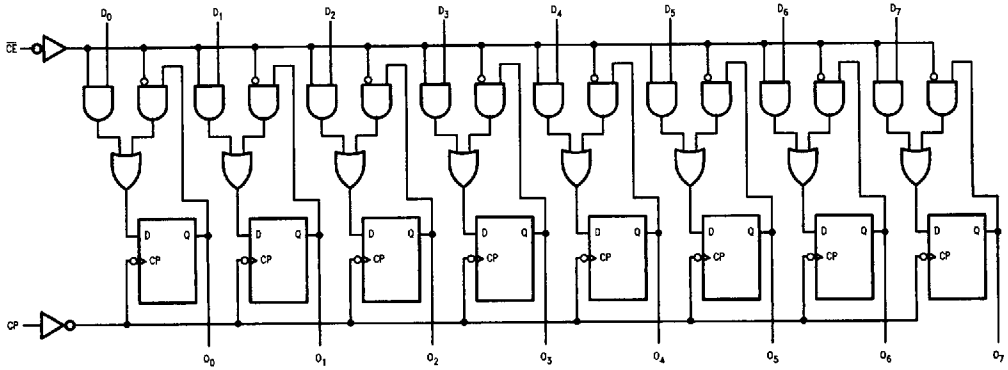
| Pin Names | Description | 54F/74F | |
|---|---|---|---|
| | | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
| $D_0$–$D_7$ | Data Inputs | 1.0/1.0 | 20 μA/−0.6 mA |
| $\overline{CE}$ | Clock Enable (Active LOW) | 1.0/1.0 | 20 μA/−0.6 mA |
| CP | Clock Pulse Input | 1.0/1.0 | 20 μA/−0.6 mA |
| $Q_0$–$Q_7$ | Data Outputs | 50/33.3 | −1 mA/20 mA |

**Mode Select-Function Table**

| Operating Mode | Inputs | | | Output |
|---|---|---|---|---|
| | CP | $\overline{CE}$ | $D_n$ | $Q_n$ |
| Load "1" | ⌐‾ | l | h | H |
| Load "0" | ⌐‾ | l | l | L |
| Hold | ⌐‾ | h | X | No Change |
| (Do Nothing) | X | H | X | No Change |

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
⌐‾ = LOW-to-HIGH Clock Transition

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +175°C |
| Plastic | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| TRI-STATE Output | −0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Military | −55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

## DC Electrical Characteristics

| Symbol | Parameter | | 54F/74F Min | 54F/74F Typ | 54F/74F Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 54F 10% $V_{CC}$ | 2.5 | | | V | Min | $I_{OH}$ = −1 mA |
| | | 74F 10% $V_{CC}$ | 2.5 | | | | | $I_{OH}$ = −1 mA |
| | | 74F 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −1 mA |
| $V_{OL}$ | Output LOW Voltage | 54F 10% $V_{CC}$ | | | 0.5 | V | Min | $I_{OL}$ = 20 mA |
| | | 74F 10% $V_{CC}$ | | | 0.5 | | | $I_{OL}$ = 20 mA |
| $I_{IH}$ | Input HIGH Current | | | | 5.0 | μA | Max | $V_{IN}$ = 2.7V |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | | 7.0 | μA | Max | $V_{IN}$ = 7.0V |
| $I_{IL}$ | Input LOW Current | | | | −0.6 | mA | Max | $V_{IN}$ = 0.5V |
| $I_{OS}$ | Output Short-Circuit Current | | −60 | | −150 | mA | Max | $V_{OUT}$ = 0V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | | 50 | μA | Max | $V_{OUT}$ = $V_{CC}$ |
| $V_{ID}$ | Input Leakage Test | | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 μA All Other Pins Grounded |
| $I_{OD}$ | Output Leakage Circuit Current | | | | 3.75 | μA | 0.0 | $V_{IOD}$ = 150 mV All Other Pins Grounded |
| $I_{CCH}$ | Power Supply Current | | | 35 | 46 | mA | Max | CP = ⎍ |
| $I_{CCL}$ | | | | 44 | 56 | | | $D_n$ = $\overline{MR}$ = HIGH |

## AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| Symbol | Parameter | 74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | | 54F $T_A$, $V_{CC}$ = Mil, $C_L = 50$ pF | | 74F $T_A$, $V_{CC}$ = Com, $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $f_{Max}$ | Maximum Clock Frequency | 130 | | | 85 | | 105 | | MHz | 2-1 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to $Q_n$ | 3.0<br>4.0 | | 7.0<br>9.0 | 2.0<br>3.0 | 8.5<br>10.5 | 2.5<br>3.5 | 7.5<br>9.0 | ns | 2-4 |

## AC Operating Requirements: See Section 2 for Waveforms

| Symbol | Parameter | 74F $T_A = +25°C$, $V_{CC} = +5.0V$ | | 54F $T_A$, $V_{CC}$ = Mil | | 74F $T_A$, $V_{CC}$ = Com | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_s(H)$<br>$t_s(L)$ | Setup Time, HIGH or LOW<br>$D_n$ to CP | 3.0<br>3.5 | | 3.5<br>4.0 | | 3.0<br>3.5 | | ns | 2-6 |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH or LOW<br>$D_n$ to CP | 0.5<br>1.0 | | 1.0<br>1.0 | | 0.5<br>1.0 | | ns | 2-6 |
| $t_s(H)$<br>$t_s(L)$ | Setup Time, HIGH or LOW<br>$\overline{CE}$ to CP | 4.1<br>3.5 | | 4.0<br>5.0 | | 4.1<br>4.0 | | ns | 2-6 |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH to LOW<br>$\overline{CE}$ to CP | 0.5<br>2.0 | | 1.5<br>2.5 | | 0.5<br>2.0 | | ns | 2-6 |
| $t_w(H)$<br>$t_w(L)$ | Clock Pulse Width,<br>HIGH or LOW | 6.0<br>6.0 | | 5.0<br>5.0 | | 6.0<br>6.0 | | ns | 2-4 |