SGS-THOMSON MICROELECTRONICS

M54HC245/640/643
M74HC245/640/643

OCTAL BUS TRANSCEIVER (3-STATE) HC245 NON INVERTING, HC640 INVERTING, HC643 INVERTING/NON INVERTING

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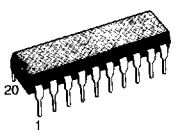
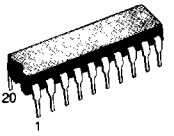
PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS245/640/643



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1	M74HCXXX C1
M74HCXXX B1N	M74HCXXX M1
M74HCXXX F1	

DESCRIPTION

The M54/74HC245, M54HC640 and M54HC643 utilise silicon gate C²MOS technology to achieve operating speed equivalent to LSTTL devices. Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it posseses the driving capability of 15 LSTTL loads. These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

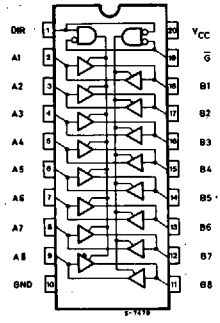
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

NOTICE FOR APPLICATION

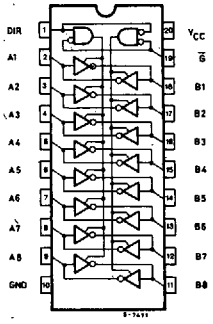
IT IS PROHIBITED TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN OUTPUT MODE. AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION (top view)

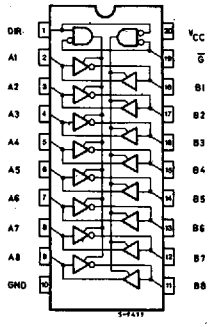
HC245



HC640



HC643



CHIP CARRIER

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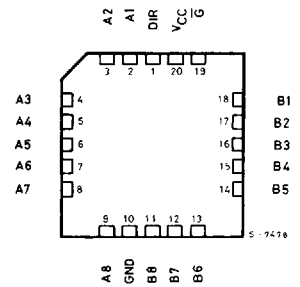
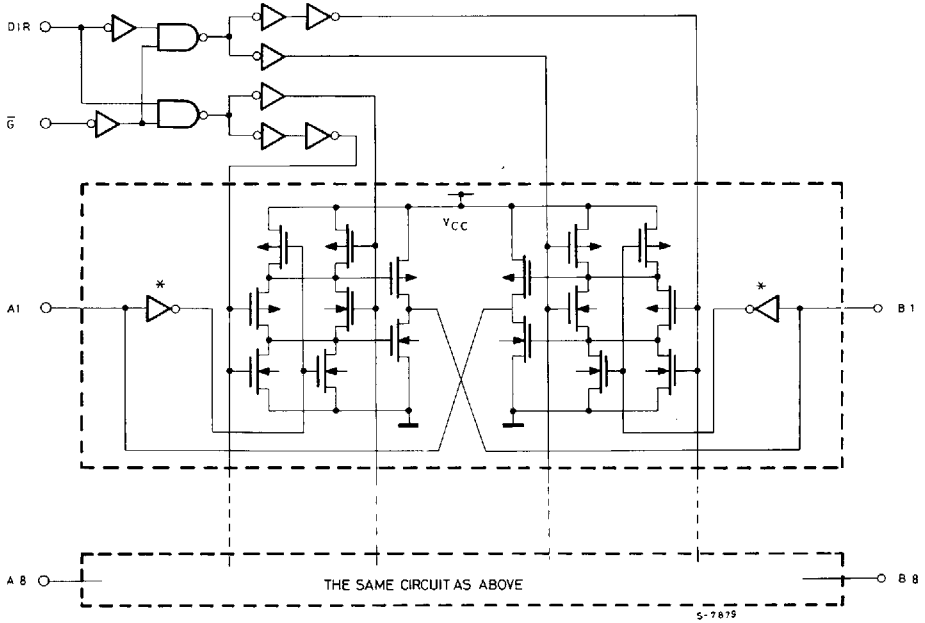


LOGIC DIAGRAM (HC640)



NOTE: IN CASE OF HC245 OR HC643, INPUT INVERTERS MARKED* AT A BUS AND B BUS OR AT B BUS ARE ELIMINATED RESPECTIVELY

TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HC245	HC640	HC643
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$	A=B
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$	B=$\overline{A}$
H	X	Z	Z	Z	Z	Z

X: "H" or "L" Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		-6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	$20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current*	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	± 0.5	—	± 5.0	—	± 10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

* Applicable only to DIR, G, $\overline{G}$ input

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transitio Time	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (for HC245)	2.0		—	48	90	—	115	—	135	ns
		4.5		—	12	18	—	23	—	27	
		6.0		—	10	15	—	20	—	23	
t_{PLH} t_{PHL}	Propagation Delay Time (for HC640/643)	2.0		—	52	110	—	140	—	165	ns
		4.5		—	13	22	—	28	—	33	
		6.0		—	11	19	—	24	—	28	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	$R_L = 1k\Omega$	—	80	160	—	200	—	240	ns
		4.5		—	20	32	—	40	—	48	
		6.0		—	17	27	—	34	—	41	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	$R_L = 1k\Omega$	—	80	190	—	240	—	285	ns
		4.5		—	25	38	—	48	—	57	
		6.0		—	21	32	—	41	—	48	

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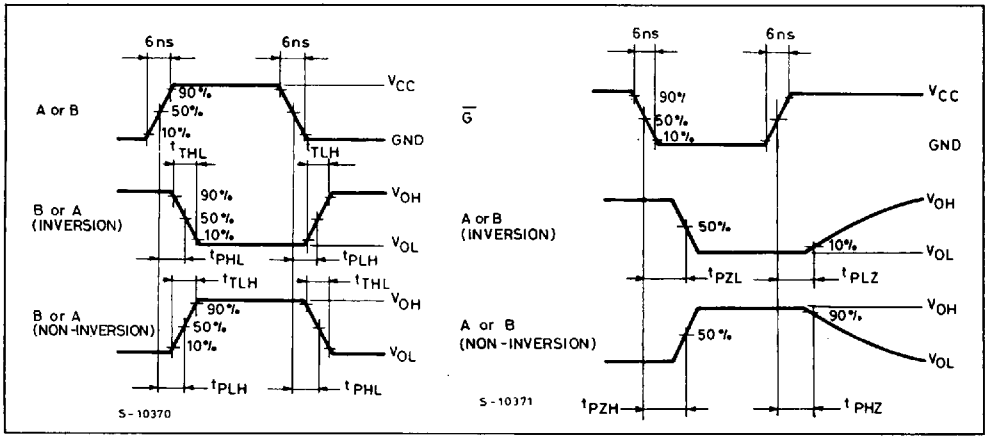
AC ELECTRICAL CHARACTERISTICS (Continued)

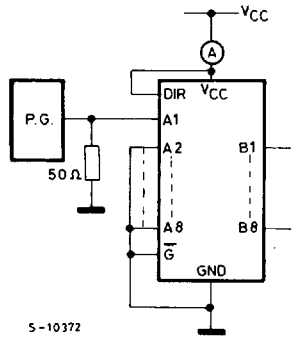
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		DIR, G, $\overline{G}$	—	5	10	—	10	—	10	pF
$C_{I/O}$	Bus Input Capacitance		A_n, B_n	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		HC245 HC640/643	— —	33 40	— —	— —	— —	— —	— —	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Circuit).

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$