

SN54ACT244, SN74ACT244 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS517B – JUNE 1995 – REVISED MAY 1996

- Inputs Are TTL Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Flat (W) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

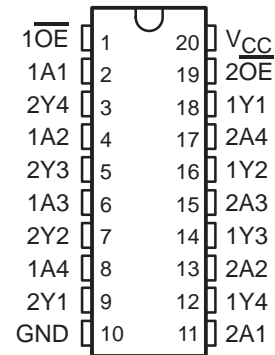
description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

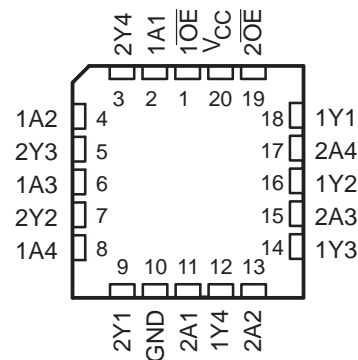
The 'ACT244 are organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN54ACT244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ACT244 is characterized for operation from -40°C to 85°C .

SN54ACT244 . . . J OR W PACKAGE
SN74ACT244 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ACT244 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

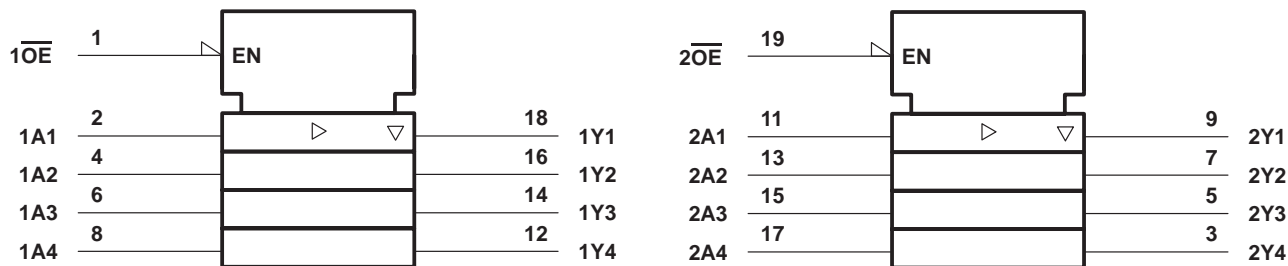
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SN54ACT244, SN74ACT244 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

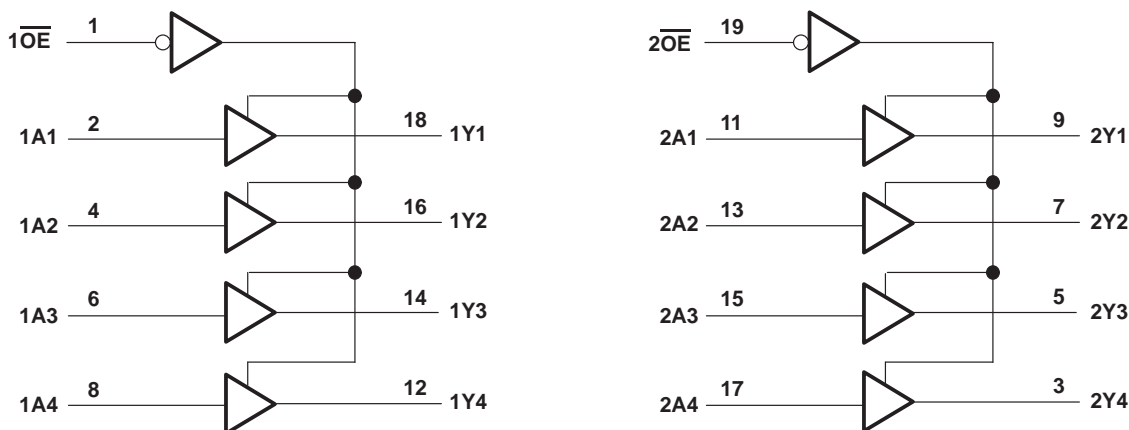
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ACT244		SN74ACT244		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	8	0	8	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT244		SN74ACT244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.49		4.4		4.4	V	
		5.5 V	5.4	5.49		5.4		5.4		
	I _{OL} = -24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I _{OH} = -50 mA†	5.5 V				3.85				
I _{OH} = -75 mA†	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	4.5 V		0.001	0.1		0.1	0.1	V	
		5.5 V		0.001	0.1		0.1	0.1		
	I _{OL} = 24 mA	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I _{OL} = 50 mA†	5.5 V					1.65			
I _{OL} = 75 mA†	5.5 V						1.65			
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±5	±2.5	μA	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80	40	μA	
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.6			1.6	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		2.5					pF	
C _o	V _I = V _{CC} or GND	5 V		8					pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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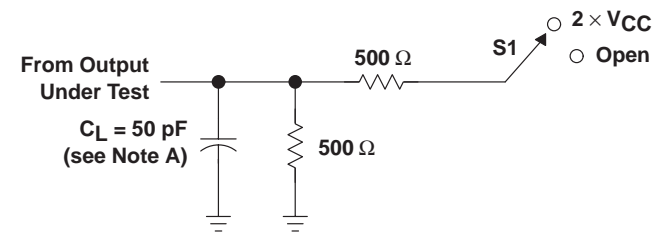
switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54ACT244		SN74ACT244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	6.5	9	1	10	1.5	10	ns
t_{PHL}			2	7	9	1	10	1.5	10	
t_{PZH}	$\overline{\text{OE}}$	Y	1.5	7	8.5	1	9.5	1	9.5	ns
t_{PZL}			2	7	9.5	1	11	1.5	10.5	
t_{PHZ}	$\overline{\text{OE}}$	Y	2	8	9.5	1	11	1.5	10.5	ns
t_{PLZ}			2.5	7.5	10	1	11.5	2	10.5	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

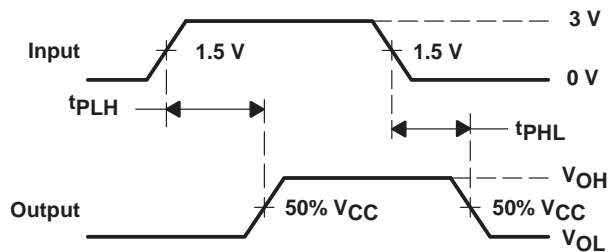
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	45	pF

PARAMETER MEASUREMENT INFORMATION

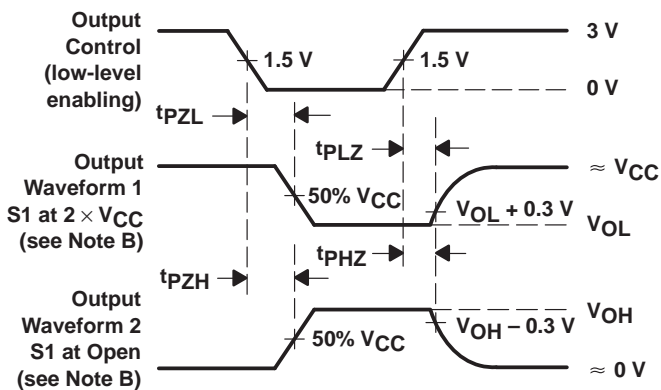


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN74ACT244, Octal Buffers/Drivers With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ACT244	SN74ACT244
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	CMOS	CMOS
Output Drive (mA)		-24/24
tpd max (ns)		10
Static Current		0.04

FEATURES

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DESCRIPTION

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TECHNICAL DOCUMENTS

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To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Full datasheet in Acrobat PDF: [sn74act244.pdf](#) (82 KB, Rev.B) (Updated: 05/01/1996)

APPLICATION NOTES

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- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Timing Differences of 10-pF Versus 50pF Loading](#) (SCEA004 - Updated: 11/01/1996)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ACT244DBR	SSOP (DB)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT244DW	SOP (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT244N	PDIP (N)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT244PWR	TSSOP (PW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74ACT244DBLE	OBSOLETE	SSOP (DB) 20	-40 TO 85	View Contents	1KU		N/A*		Not Available			
SN74ACT244DBR	ACTIVE	SSOP (DB) 20	-40 TO 85	View Contents	1KU 0.32	2000	N/A*	> 10k 11 Nov	8 WKS	DigiKey AMERICA	> 1k	BUY NOW
SN74ACT244DW	ACTIVE	SOP (DW) 20	-40 TO 85	View Contents	1KU 0.32	25	N/A*	1000 21 Oct	8 WKS	Avnet AMERICA	> 1k	BUY NOW
								1725 01 Nov		DigiKey AMERICA	> 1k	BUY NOW
								> 10k 11 Nov				
SN74ACT244DWR	ACTIVE	SOP (DW) 20	-40 TO 85	View Contents	1KU 0.32	2000	N/A*	> 10k 08 Nov	8 WKS	Avnet AMERICA	> 1k	BUY NOW
										DigiKey AMERICA	> 1k	BUY NOW

SN74ACT244N	ACTIVE	PDIP (N) 20	-40 TO 85	View Contents	1KU 0.32	20	720	48 23 Sep	8 WKS	Avnet AMERICA	> 1k	BUY NOW
								2920 26 Sep		DigiKey AMERICA	171	BUY NOW
								> 10k 11 Nov				
SN74ACT244NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 0.45	2000	N/A*	1 14 Oct	3 WKS			
								> 10k 11 Nov				
SN74ACT244PWLE	OBSOLETE	TSSOP (PW) 20	-40 TO 85	View Contents	1KU		N/A*		Not Available			
SN74ACT244PWR	ACTIVE	TSSOP (PW) 20	-40 TO 85	View Contents	1KU 0.32	2000	N/A*	> 10k 07 Nov	2 WKS			
								> 10k 13 Nov				
								> 10k 14 Nov				


MODELS

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- [IBIS Model of SN74ACT244](#) (SCAM015, 76 KB - Updated: 06/06/2002)
[IBIS Model of SN74ACT244](#) (SCAM015, 14 KB, ZIP - Updated: 06/06/2002)

Table Data Updated on: 9/26/2002

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