M5M4V18160BJ,TP,RT-6,-7,-8,-6S,-7S,-8S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18160BXX-6,-6S	60	15	30	15	110	450
M5M4V18160BXX-7,-7S	70	20	35	20	130	390
M5M4V18160BXX-8,-8S	80	20	40	20	150	330

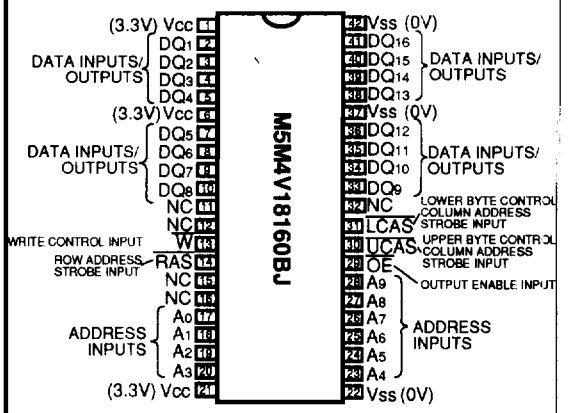
XX=J,TP,RT

- Standard 42pin SOJ, 50pin TSOP
- Single 3.3V ± 0.3V supply
- Low stand-by power dissipation
  3.6mW (Max) ..... CMOS Input level
- Low operating power dissipation
  M5M4V18160Bxx -6, -6S..... 540.0mW (Max)
  M5M4V18160Bxx -7, -7S..... 470.0mW (Max)
  M5M4V18160Bxx -8, -8S..... 400.0mW (Max)
- Fast-page mode, Read-modify-write,$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0 ~A_9)

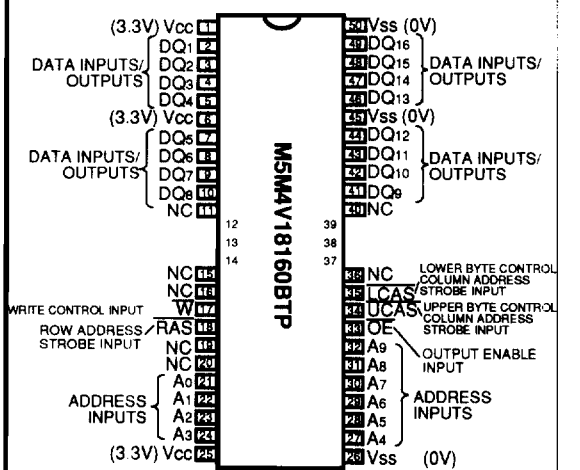
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

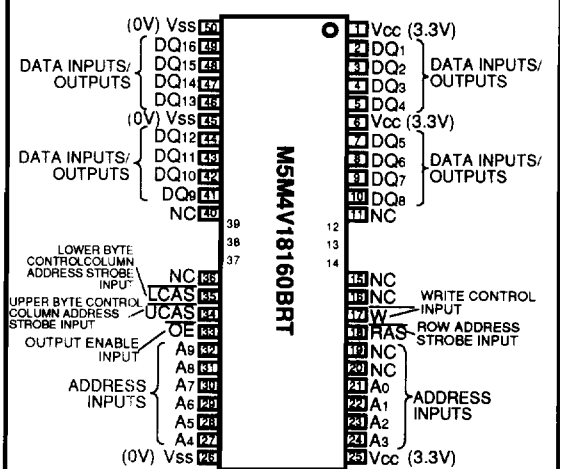
PIN CONFIGURATION (TOP VIEW)



Outline 42P0K (400mil SOJ)



Outline 50P3W-L (400mil TSOP)



Outline 50P3W-M (400mil TSOP)

NC : NO CONNECTION

MITSUBISHI ELECTRIC

FUNCTION

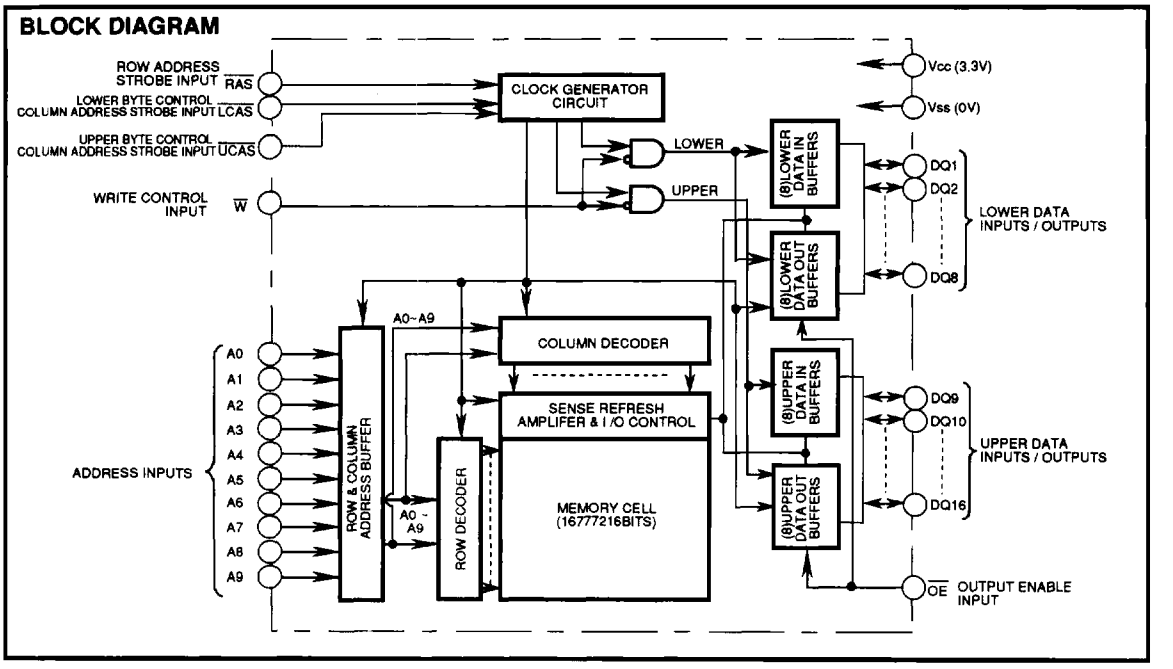
The M5M4V18160BJ, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.3	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦Vcc+0.3V,Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M4V18160B-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			150	mA
		M5M4V18160B-7,-7S				130	
		M5M4V18160B-8,-8S				110	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc-0.2V			0.5	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M4V18160B-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			150	mA
		M5M4V18160B-7,-7S				130	
		M5M4V18160B-8,-8S				110	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	M5M4V18160B-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			70	mA
		M5M4V18160B-7,-7S				60	
		M5M4V18160B-8,-8S				50	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V18160B-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			150	mA
		M5M4V18160B-7,-7S				130	
		M5M4V18160B-8,-8S				110	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

CAPACITANCE (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz Vi=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, $\overline{W}$ input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		M5M4V18160B-8,-8S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note7,8)		15		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note7,9)		60		70		80	ns
t_{AA}	Column address access time	(Note 7,10)		30		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 2TTL loads and 100pF. The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL})
8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$
11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leq \pm 10\ \mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits						Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		M5M4V18160B-8,-8S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4		16.4	ms
t_{RP}	$\overline{RAS}$ high pulse width		40		50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note15)	20	45	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note16)	15	30	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note17)	0	10	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note18)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note18)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note19)	15		15		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note19)	15		15		15		ns
t_T	Transition time	(Note20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T =5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
18: Either t_{DZC} or t_{DZO} must be satisfied.
19: Either t_{CDD} or t_{ODD} must be satisfied.
20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		M5M4V18160B-8,-8S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		ns
tRCS	Read Setup time after $\overline{CAS}$ high		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ low	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ low	(Note 21)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		30		35		40		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		M5M4V18160B-8,-8S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		10		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		20		ns
tWP	Write pulse width		10		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		M5M4V18160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note22)	155		180		200		ns
t_{RAS}	$\overline{RAS}$ low pulse width	105	10000	120	10000	130	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	60	10000	70	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	105		120		130		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	60		70		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note23)	40		45		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note23)	85		95		105		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note23)	55		60		65		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		20		ns
t_{WP}	Write pulse width	10		10		15		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	10		15		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.
23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		M5M4V18160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	85		95		105		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note25)	100	125000	115	125000	130	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note26)	10	15	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note23)	60		65		70		ns

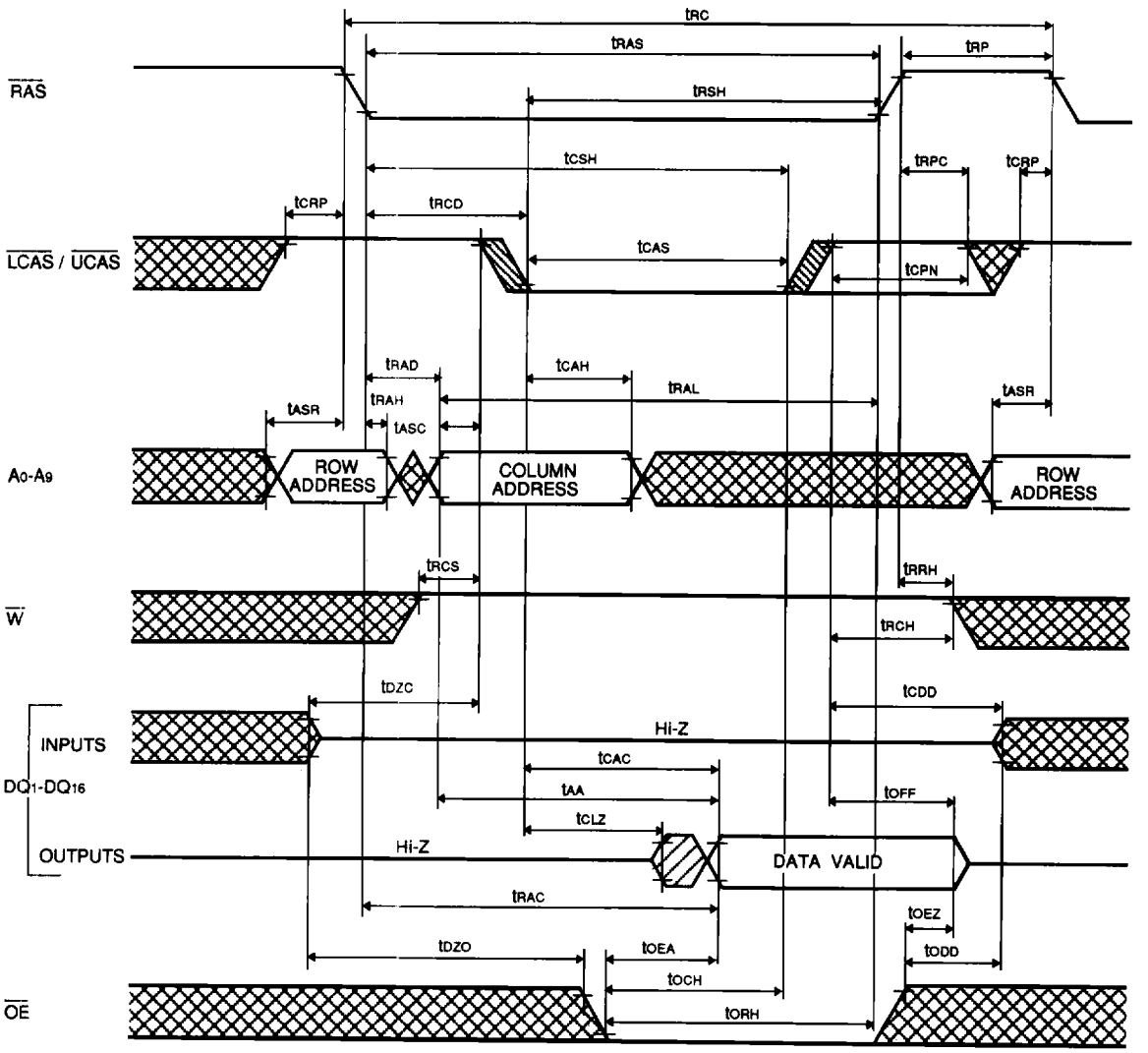
Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M4V18160B-6,-6S		M5M4V18160B-7,-7S		M5M4V18160B-8,-8S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 28)
Read Cycle



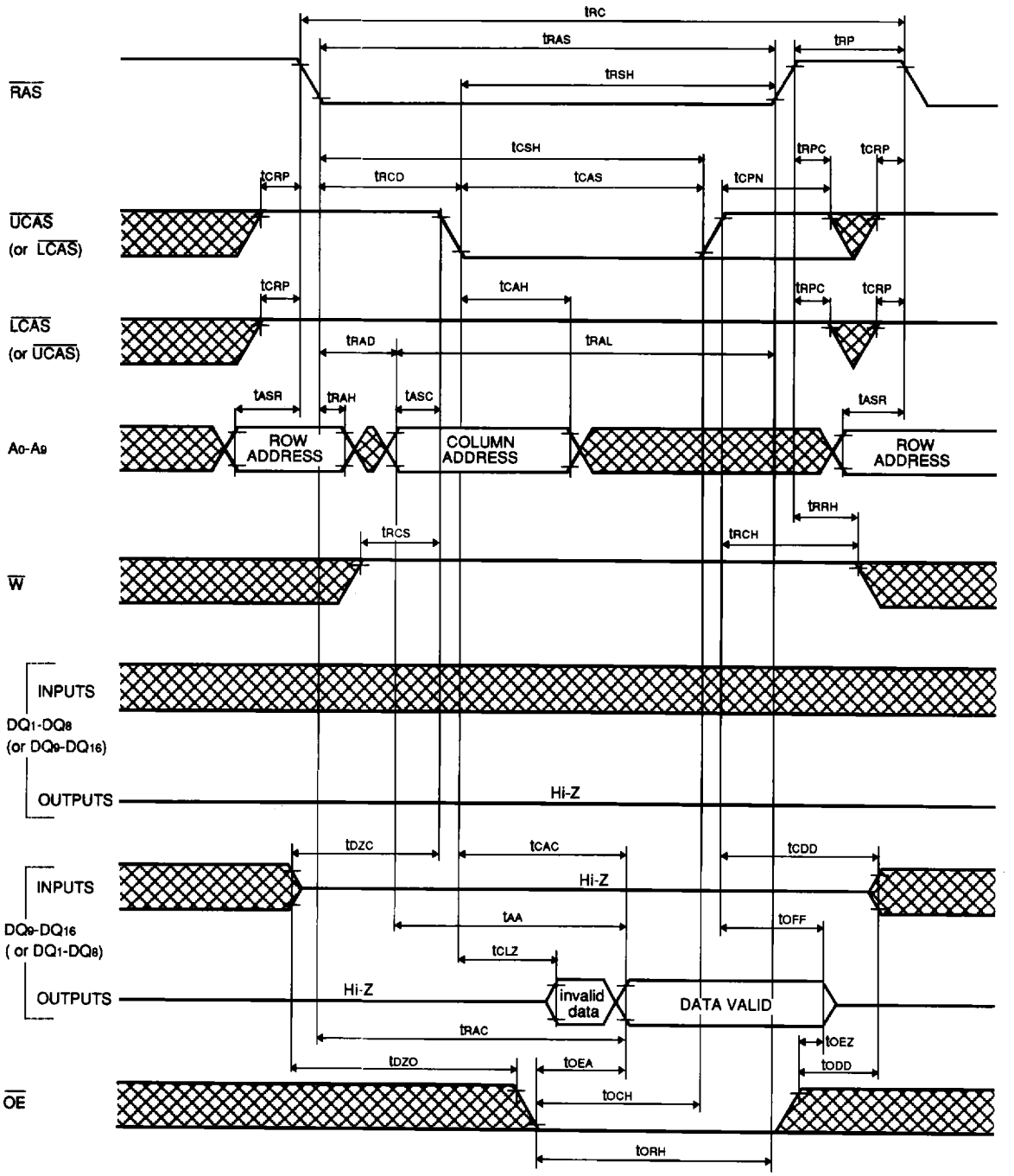
Note 28

Indicates the don't care input.
$V_{IH}(min.) \leq V_{IN} \leq V_{IH}(max)$ or $V_{IL}(min.) \leq V_{IN} \leq V_{IL}(max)$

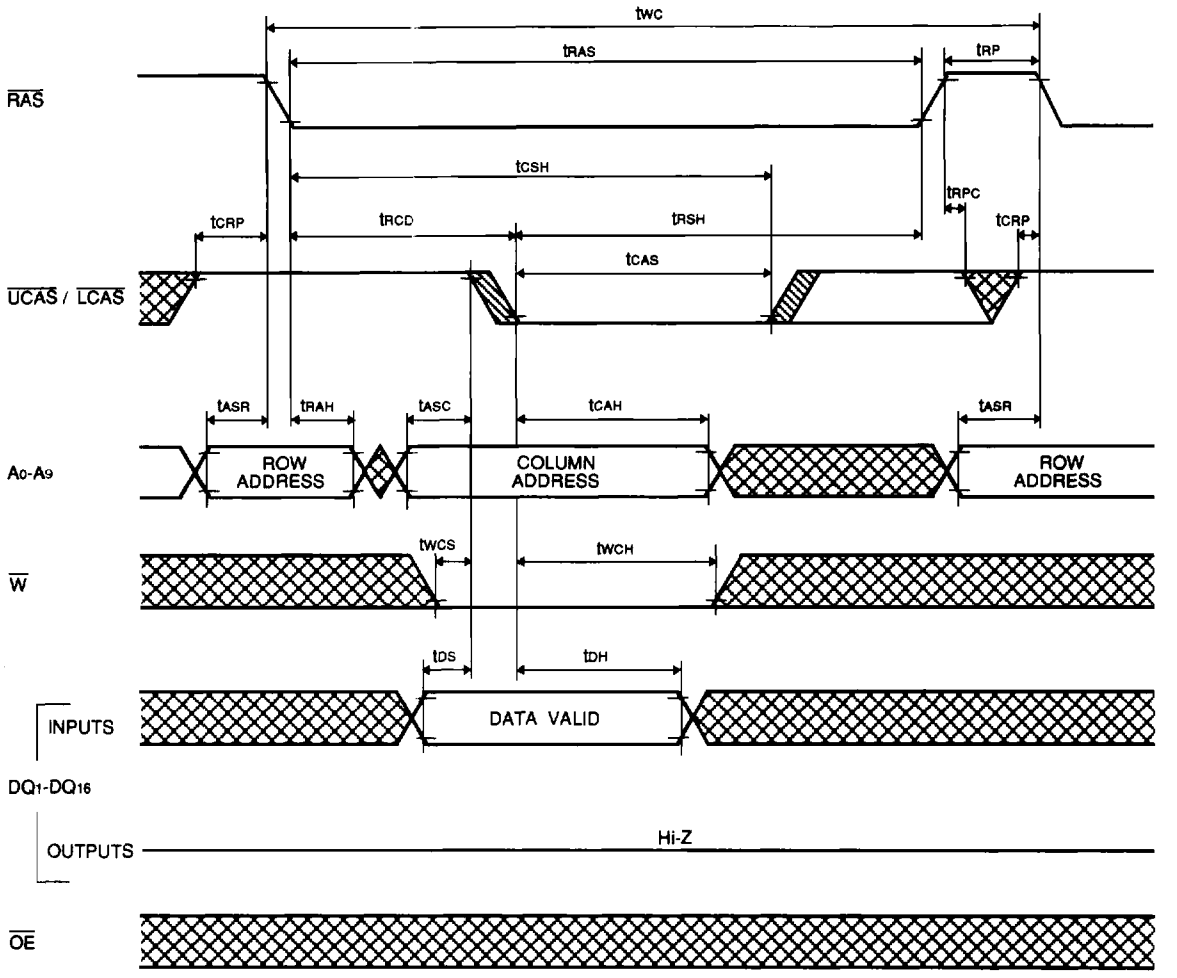
Indicates the invalid output.

Indicates the skew of the two inputs.

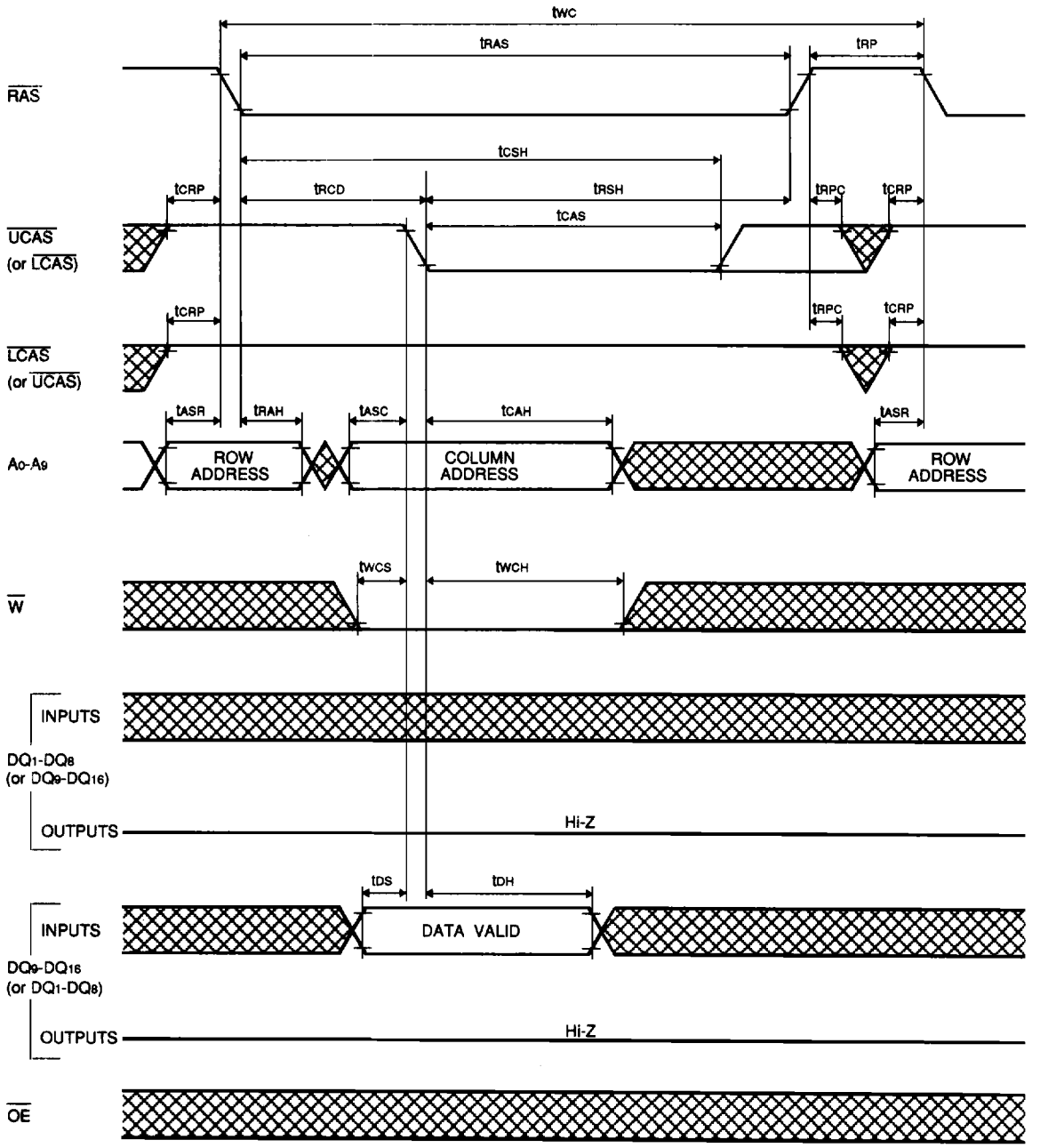
Upper / (Lower) Byte Read Cycle



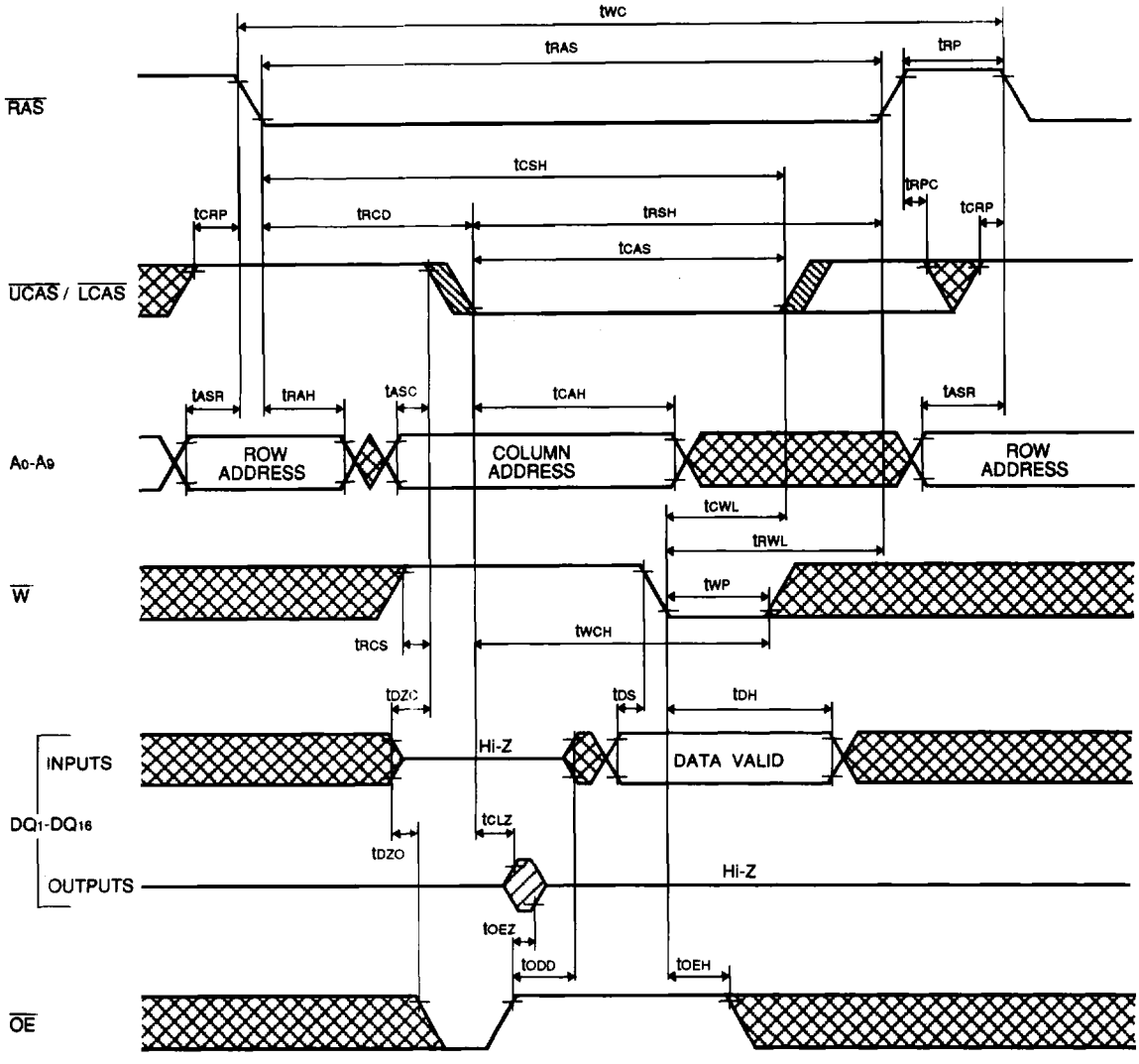
Write Cycle (Early write)



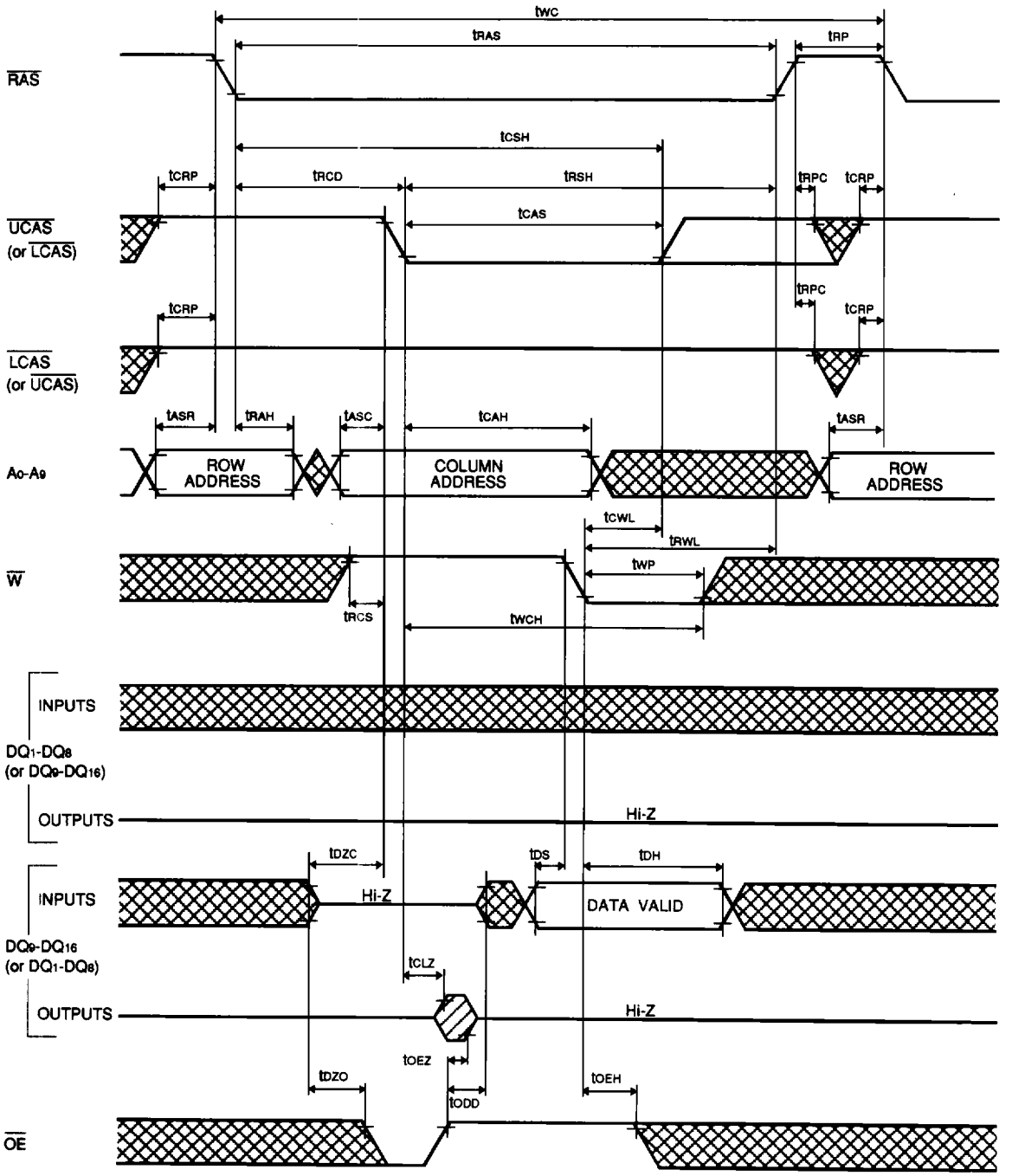
Upper/(Lower) Byte Write Cycle (Early write)



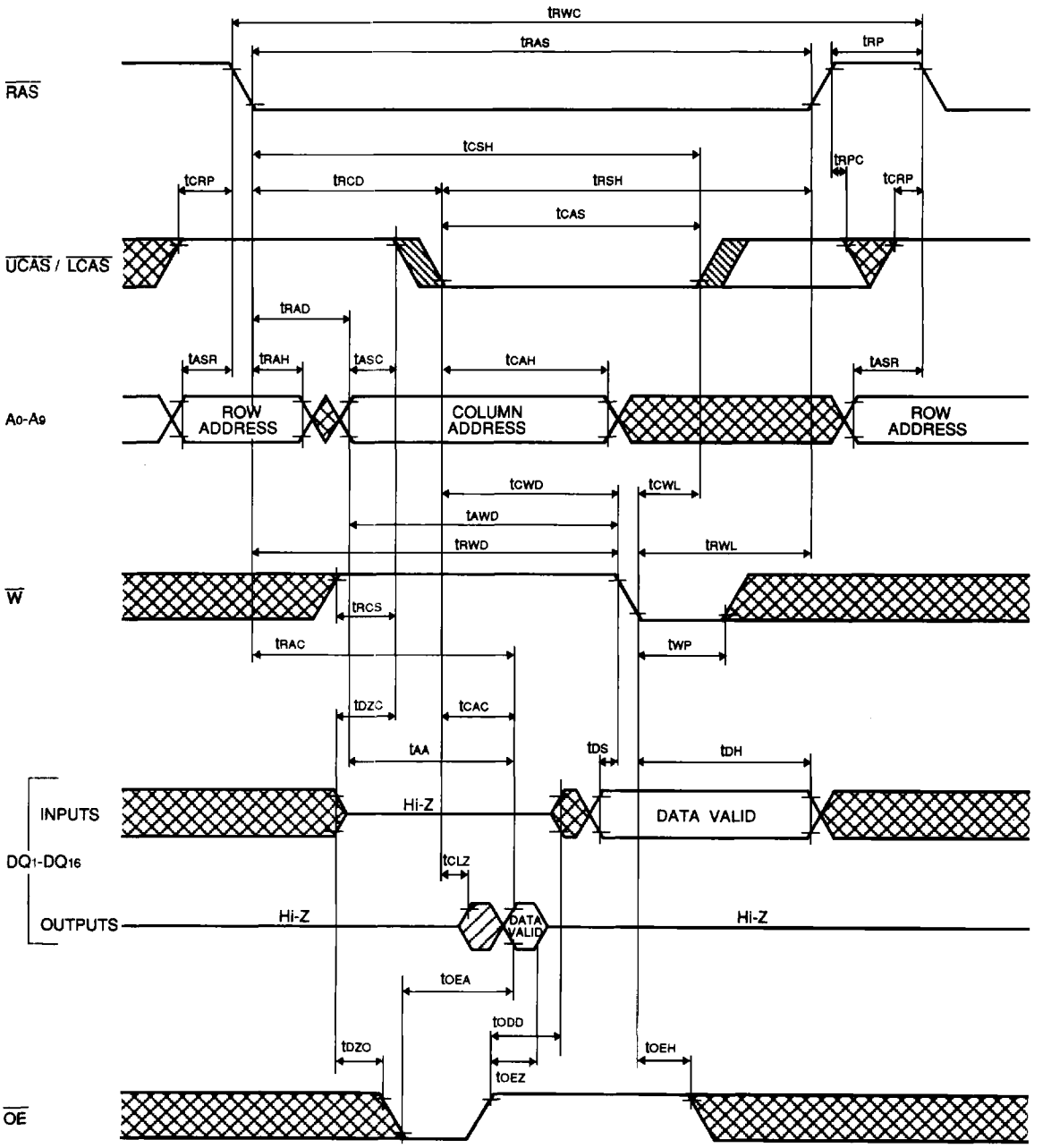
Write Cycle (Delayed write)



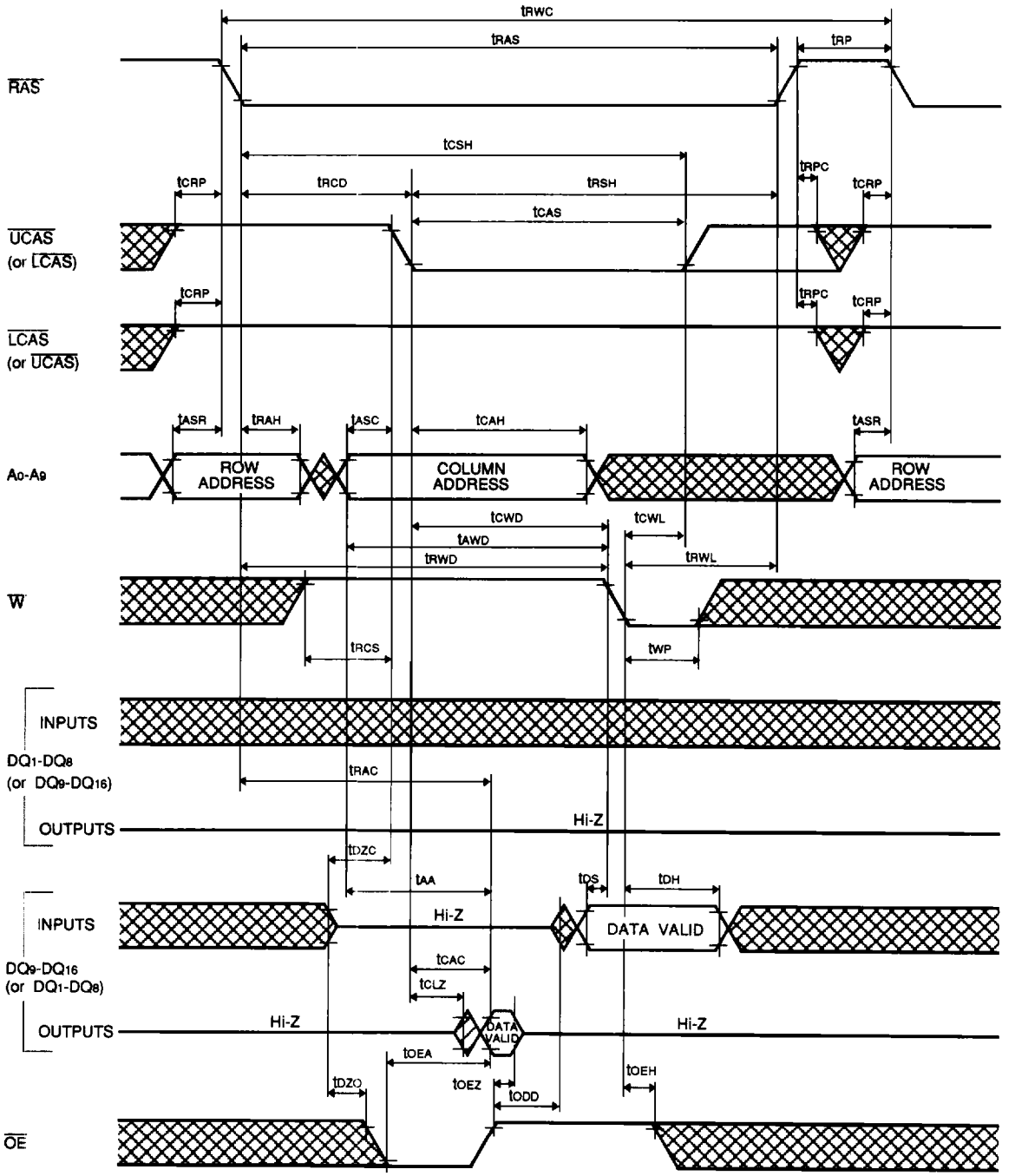
Upper/(Lower) Byte Write Cycle (Delayed write)



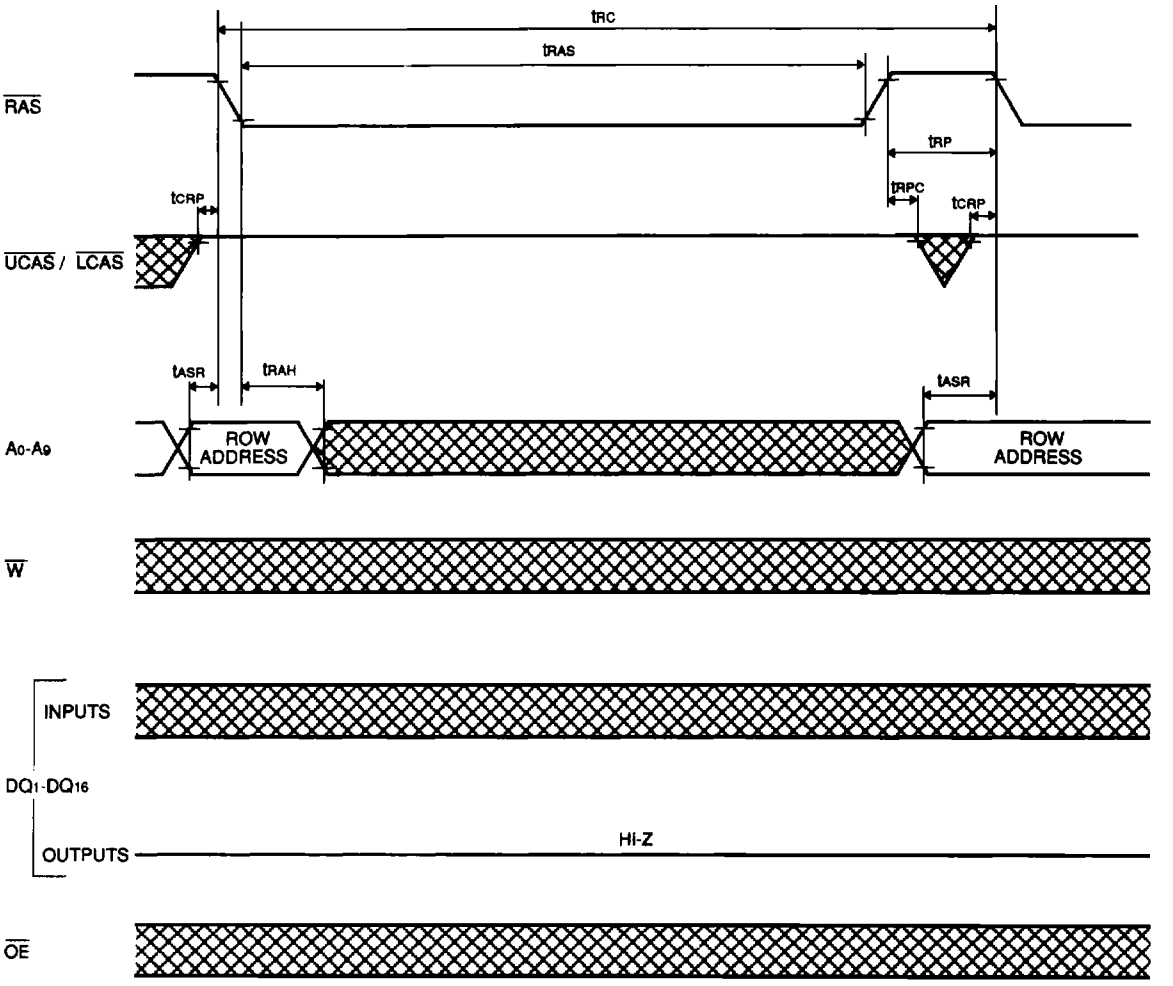
Read-Write, Read-Modify-Write Cycle



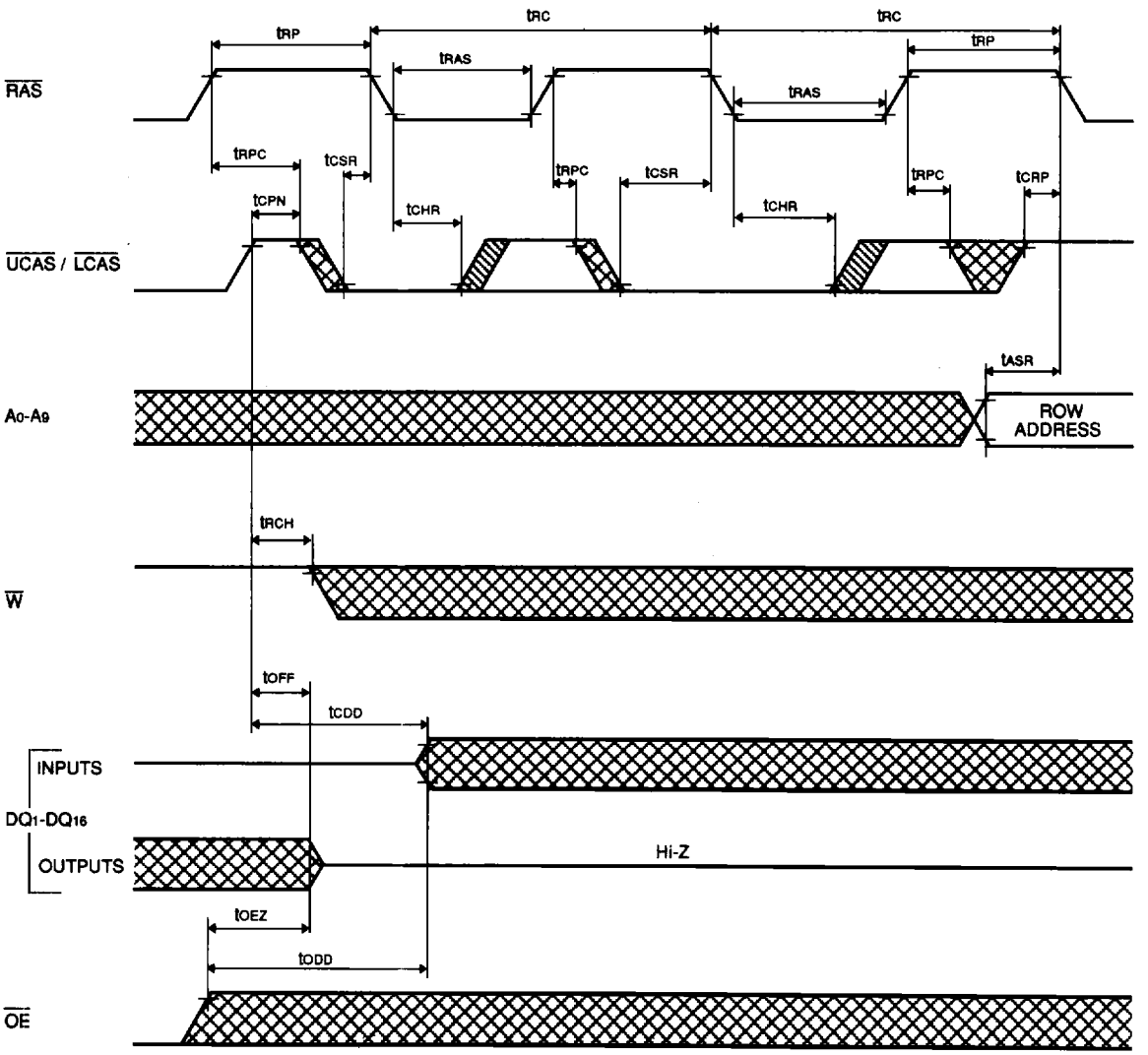
Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



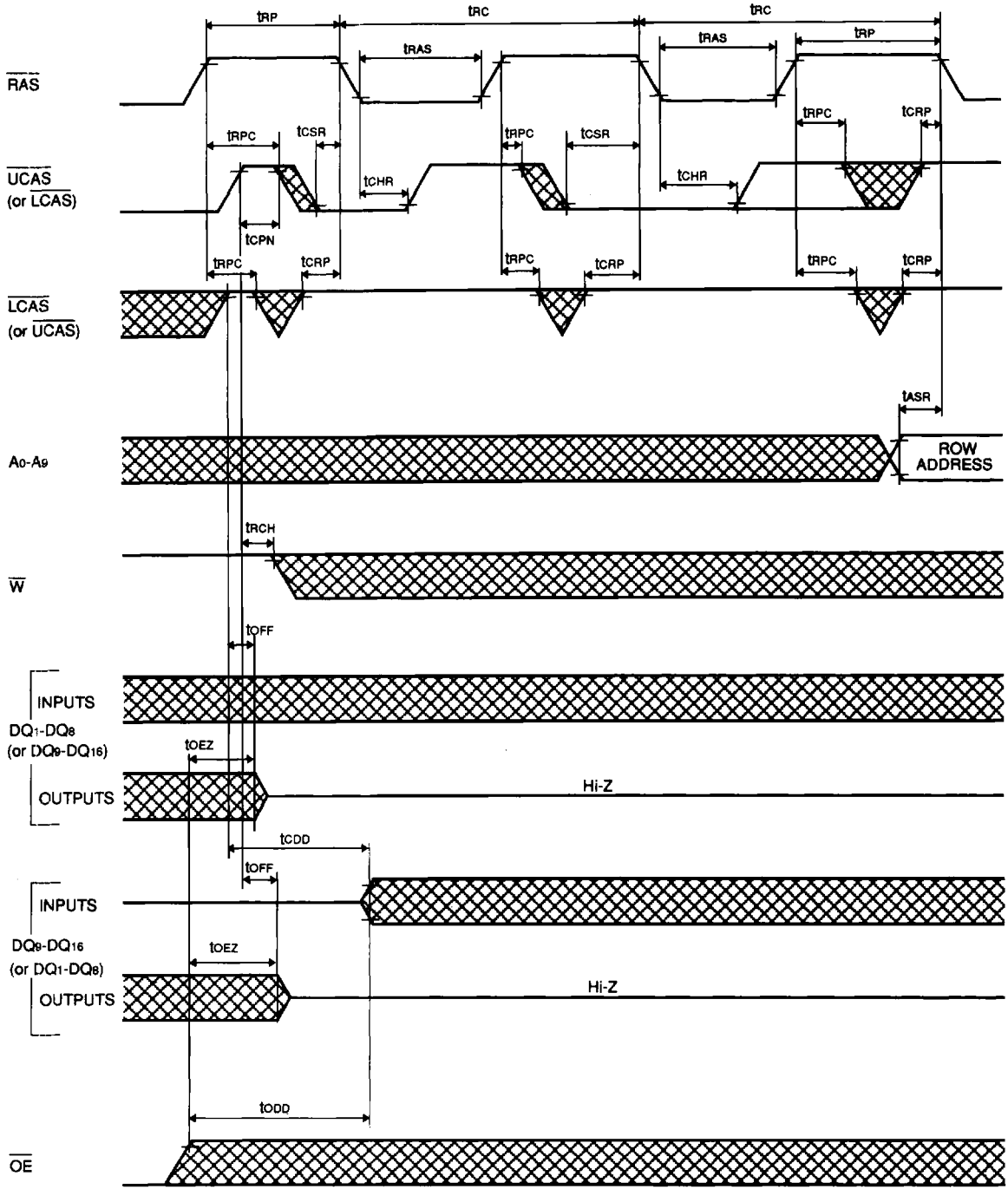
RAS-only Refresh Cycle



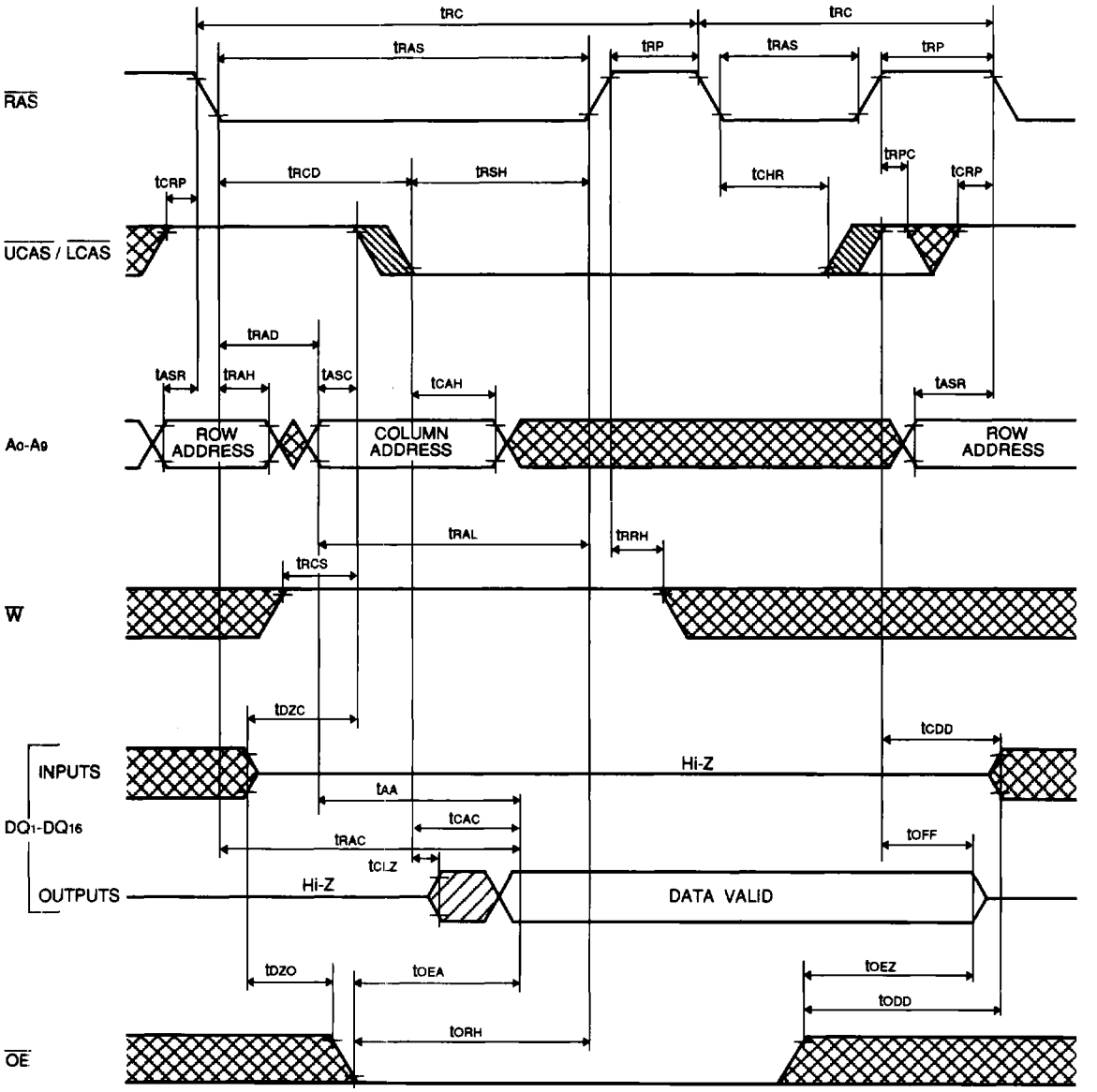
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Upper/(Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

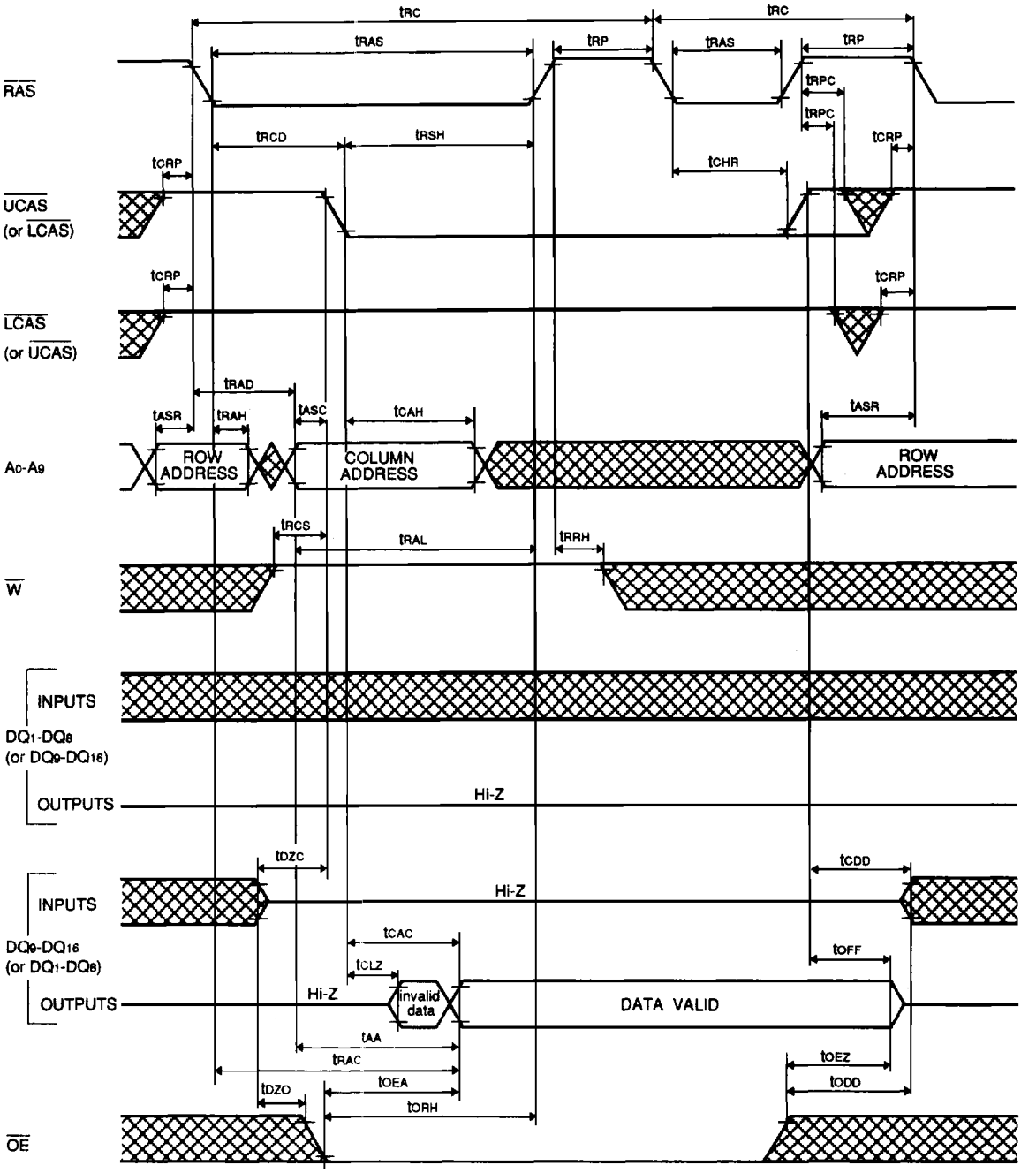


Hidden Refresh Cycle (Read) (Note 29)



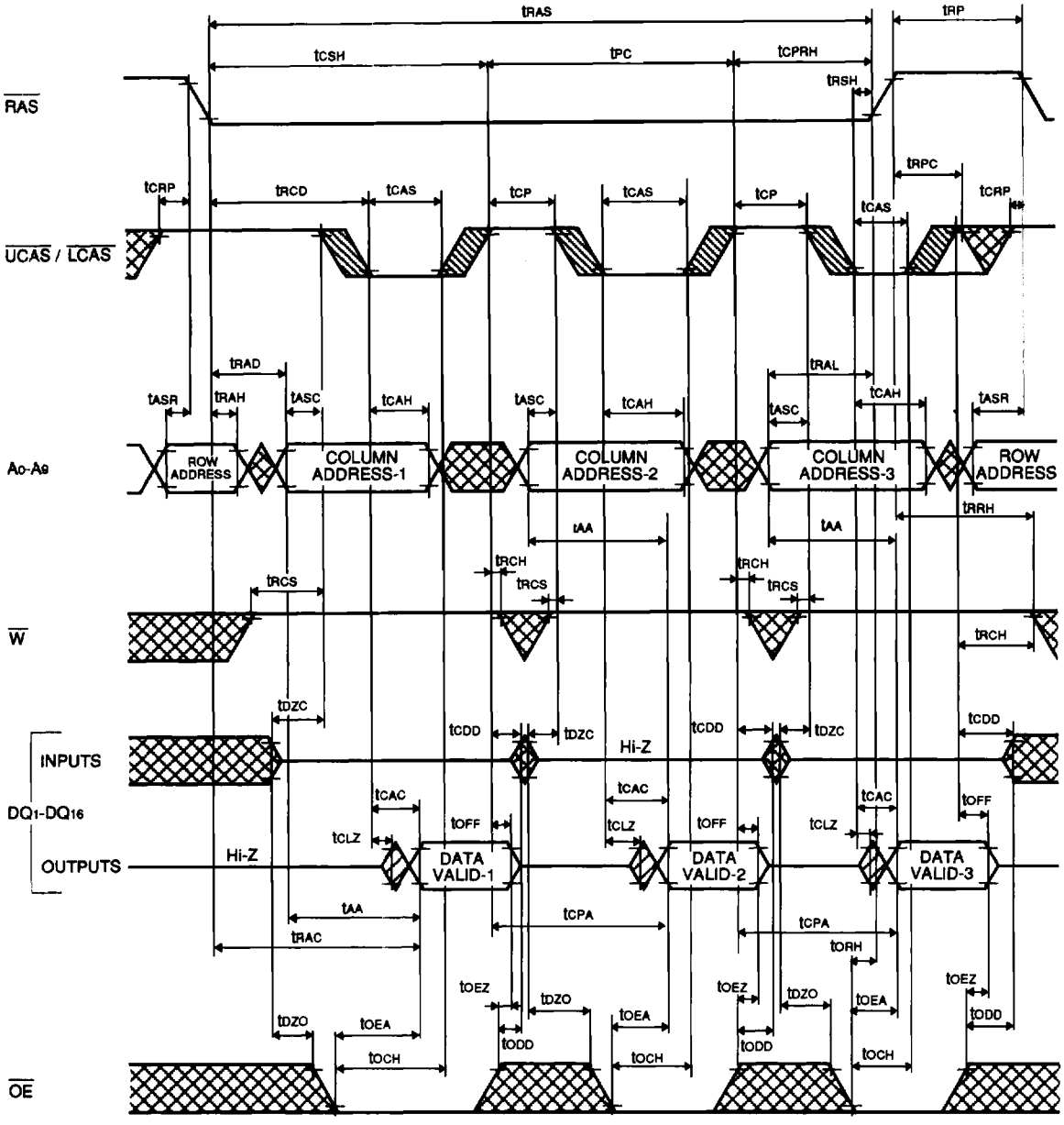
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 29)

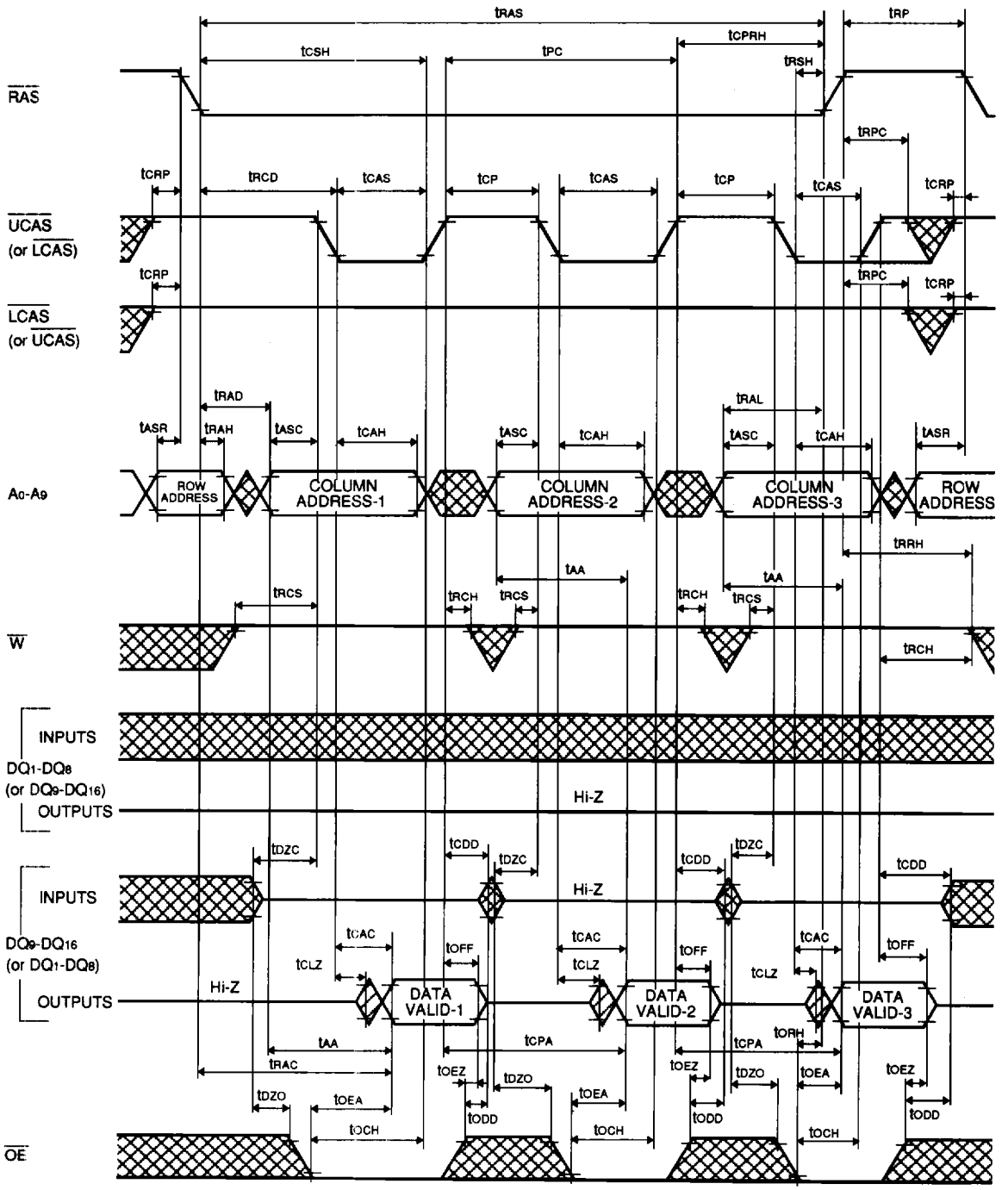


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

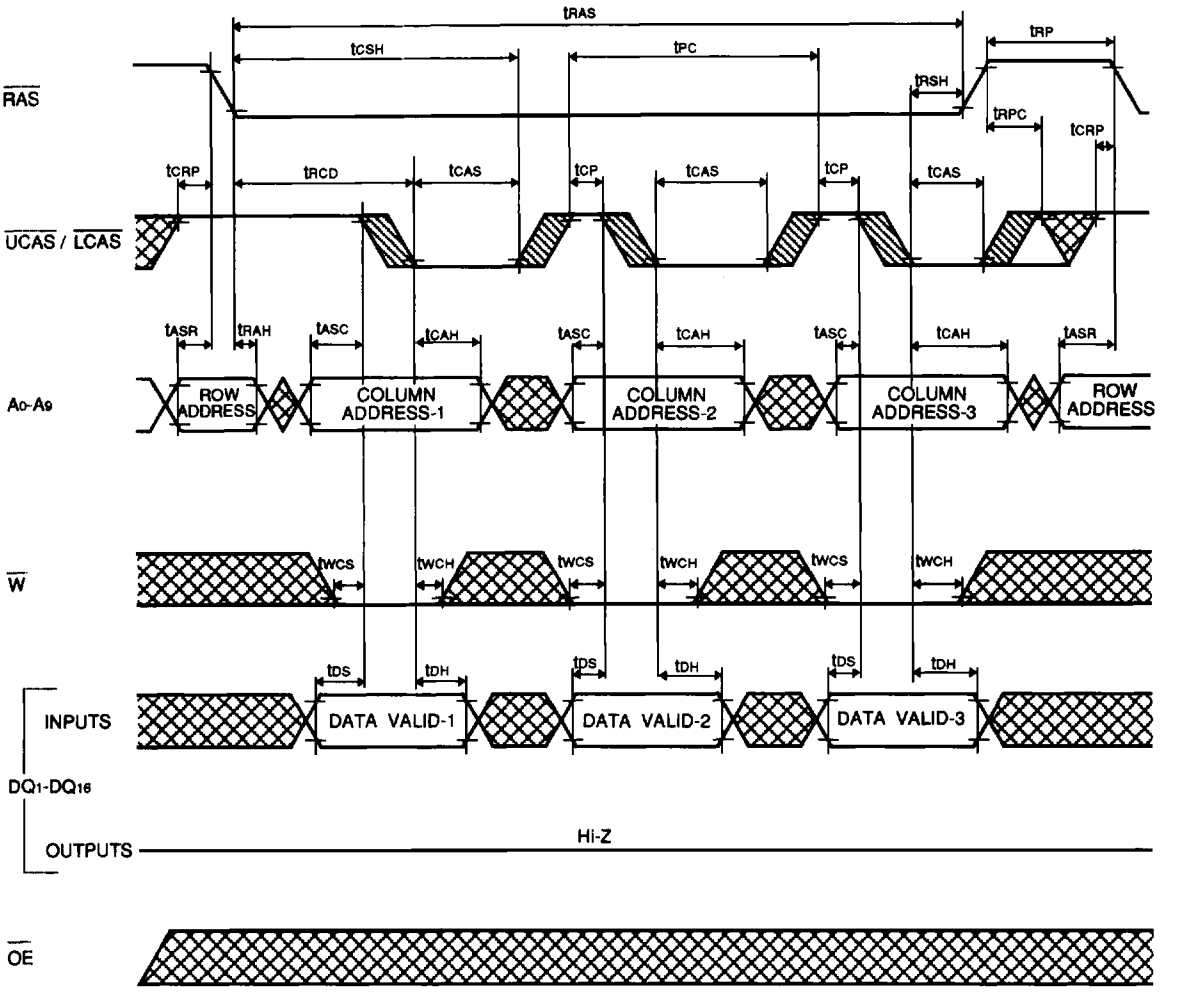
Fast Page Mode Read Cycle



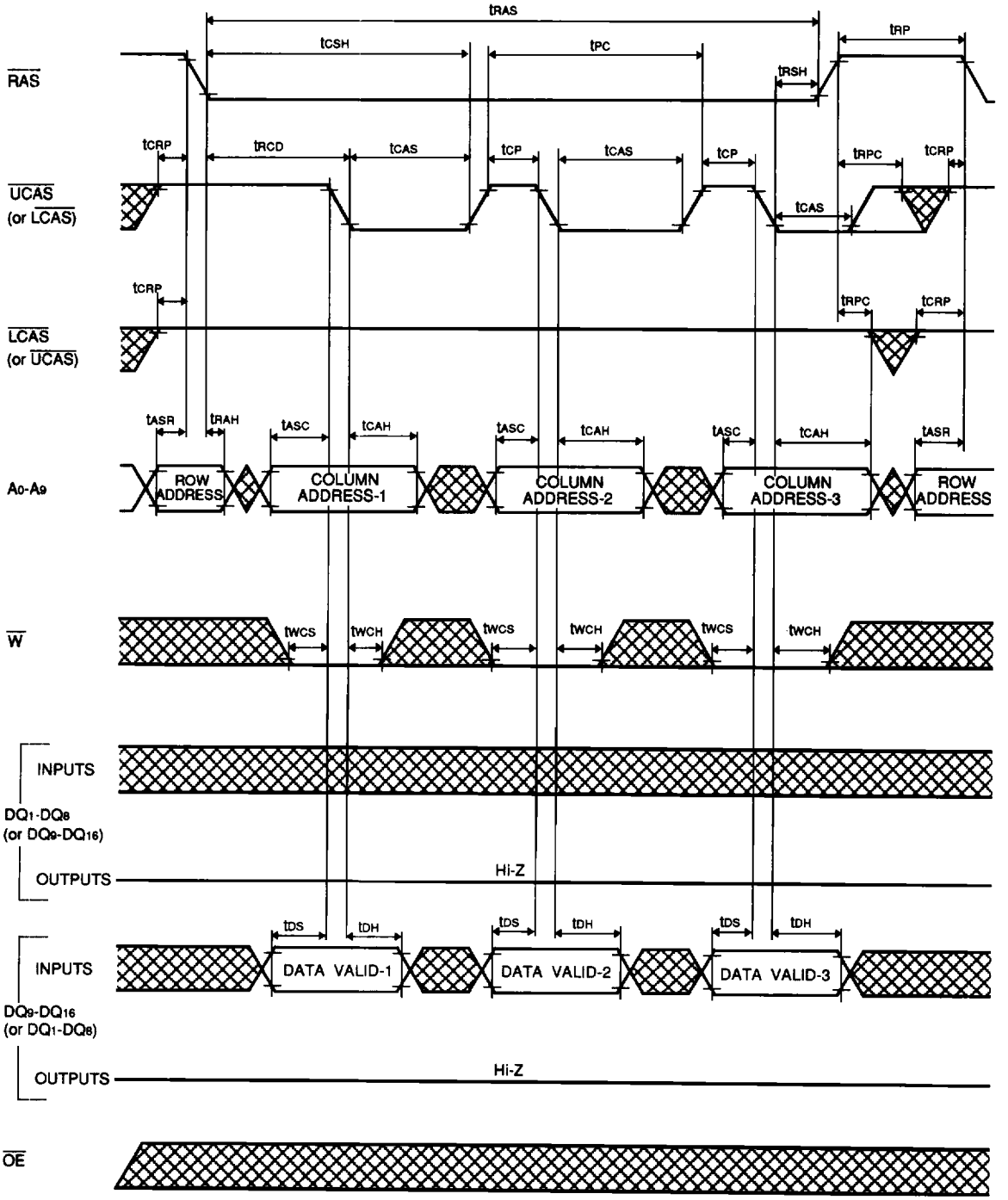
Upper/(Lower) Fast Page Mode Read Cycle



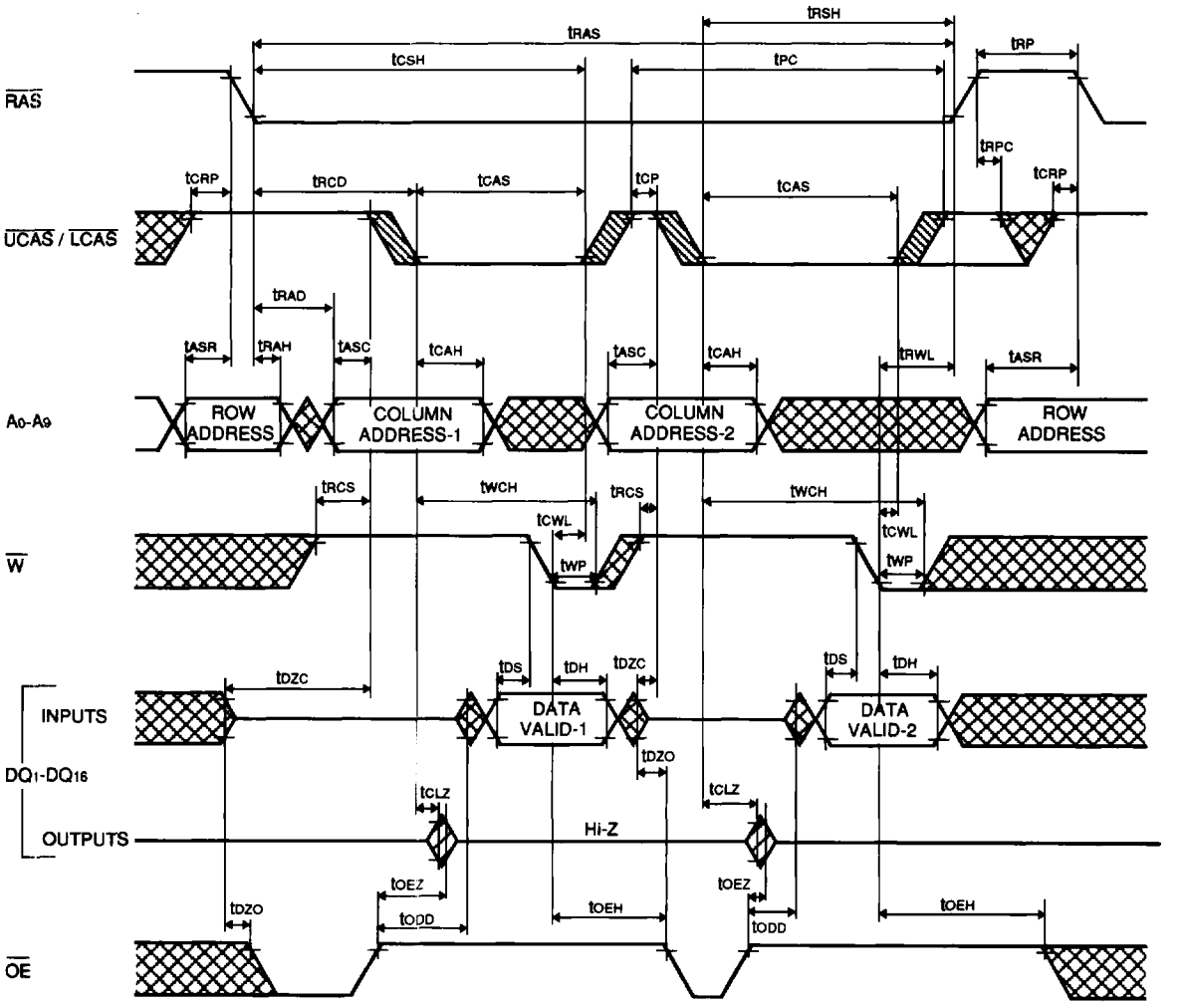
Fast Page Mode Write Cycle (Early Write)



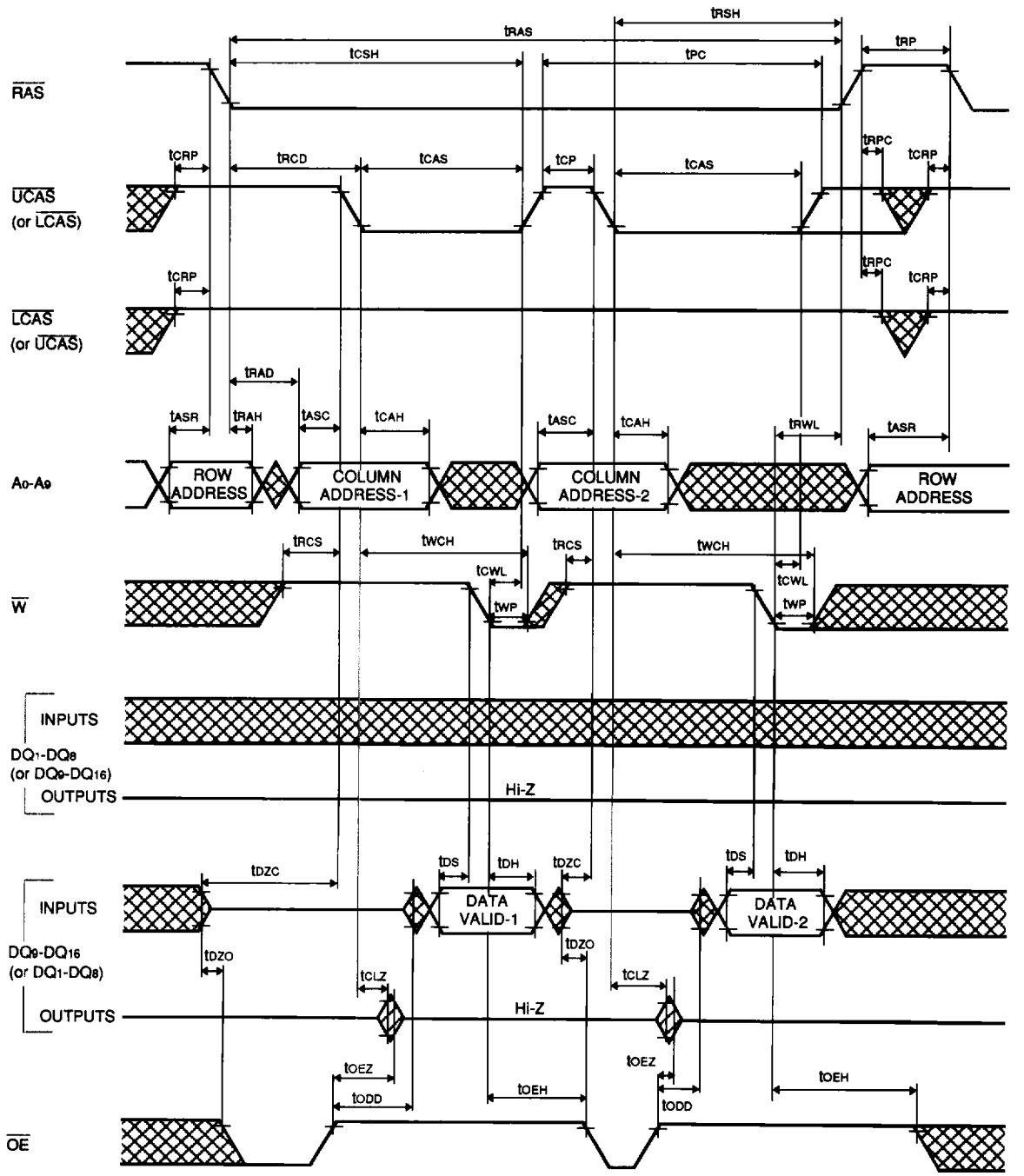
Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



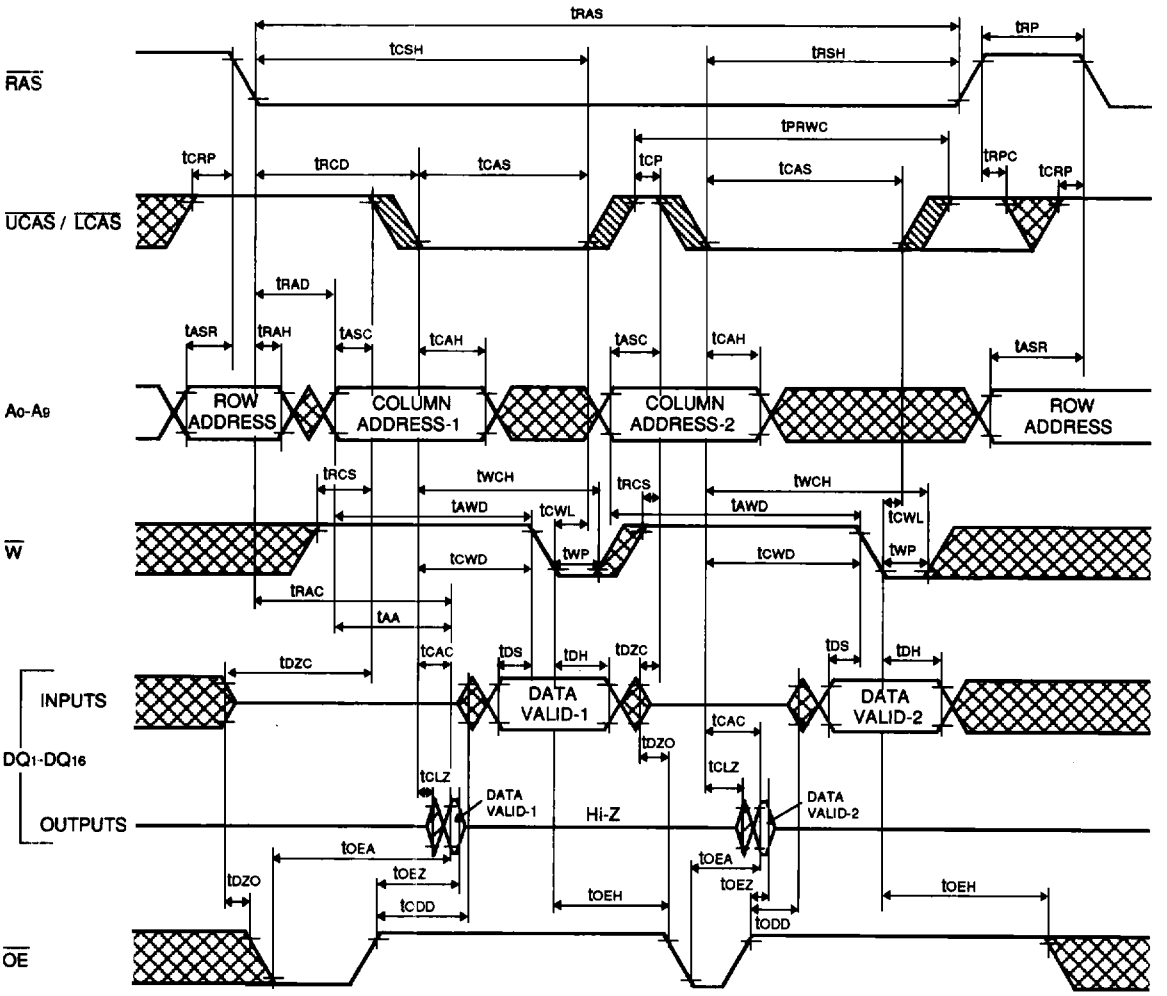
Fast Page Mode Write Cycle (Delayed Write)



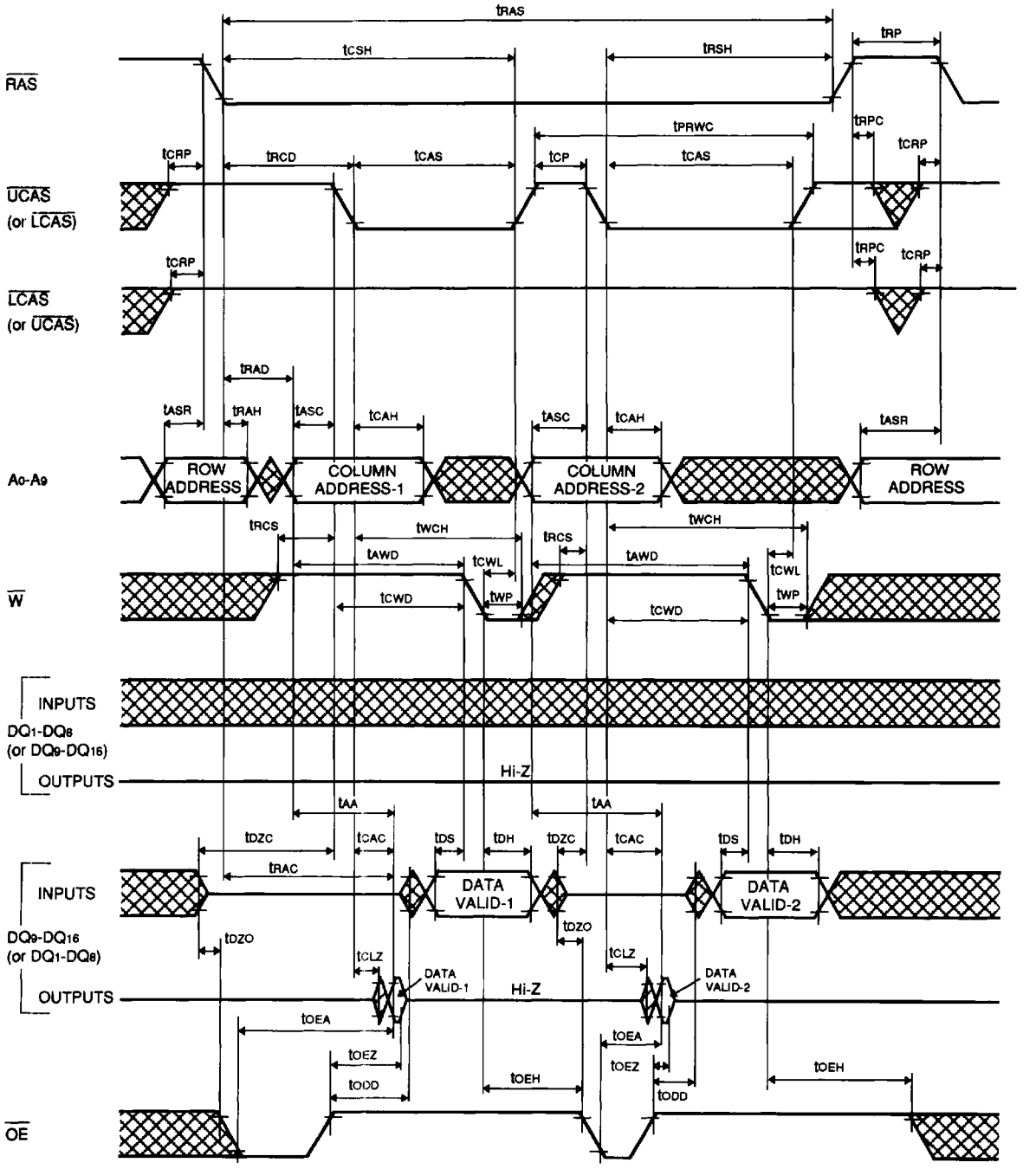
Fast Page Mode Upper / (Lower) Byte Write (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S / -8S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC9\ (AV)}$	Average supply current from Vcc Self - Refresh cycle	M5M4V18160B -6S, -7S, -8S	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			200	μA

TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V18160B-6S		M5M4V18160B-7S		M5M4V18160B-8S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

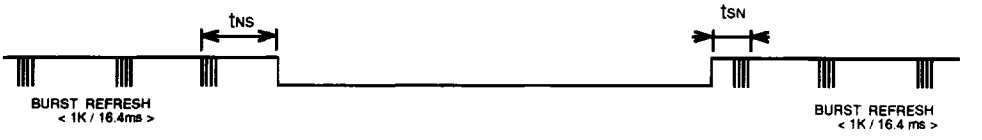
SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

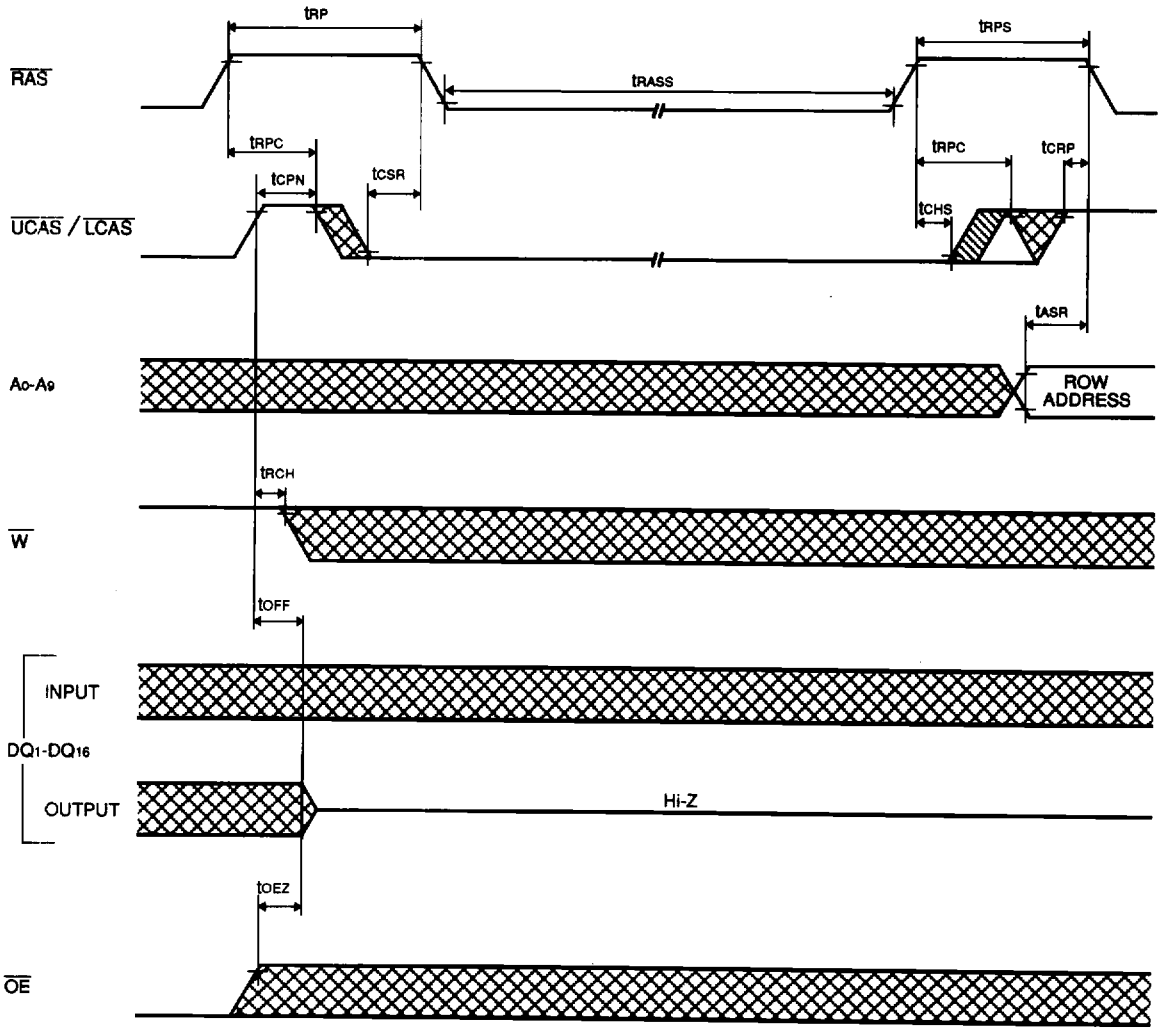
The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh , on the condition of tNS≦ 16.4 ms and tSN ≦ 16.4 ms.

(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh , on the condition of tNS + tSN ≦ 16.4 ms.



Self Refresh Cycle



Upper/(Lower) Self Refresh Cycle*