DUAL 4-BIT LATCH

The HEF4508B is a dual 4-bit latch, which consists of two identical independent 4-bit latches with separate strobe (ST), master reset (MR), output-enable input ($\overline{EO}$) and 3-state outputs (O).

With the ST input in the HIGH state, the data on the D inputs appear at the corresponding outputs provided $\overline{EO}$ is LOW. Changing the ST input to the LOW state locks the data into the latch. A HIGH on the reset line forces the outputs to a LOW level regardless of the state of the ST input. The 3-state outputs are controlled by the output-enable input. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state regardless of other input conditions. This allows the outputs to interface directly with bus orientated systems. When $\overline{EO}$ is LOW the contents of the latches are available at the outputs.

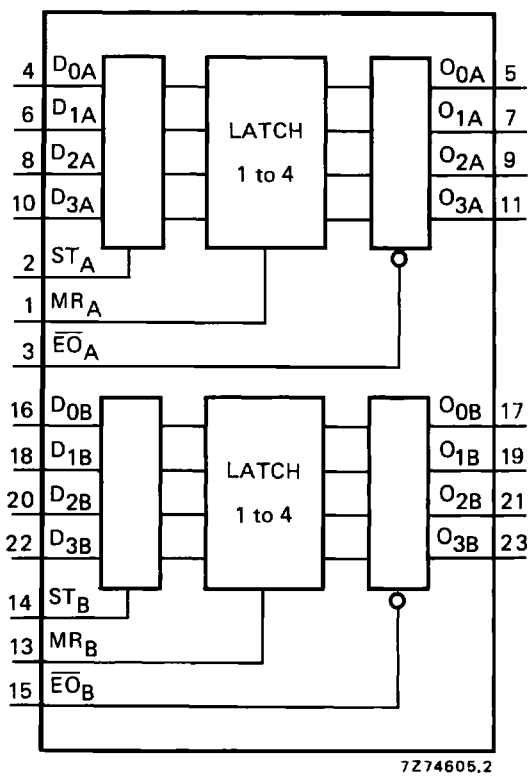

Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

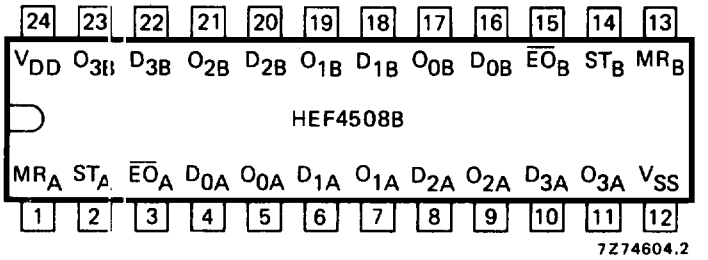

Fig. 2 Pinning diagram.

HEF4508BP(N): 24-lead DIL; plastic (SOT101-1)
HEF4508BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
HEF4508BT(D): 24-lead SO; plastic (SOT137-1)
( ): Package Designator North America

PINNING

D_{0A} to D_{3A}, D_{03} to D_{3B}	data inputs
ST_A, ST_B	strobe inputs
MR_A, MR_B	master reset inputs
$\overline{EO}_A$, $\overline{EO}_B$	output enable inputs
O_{0A} to O_{3A}, O_{0B} to O_{3B}	3-state outputs

FUNCTION TABLE

inputs				output
MR	ST	$\overline{EO}$	D_n	O_n
L	H	L	H	H
L	H	L	L	L
L	L	L	X	latched
H	X	L	X	L
X	X	H	X	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance OFF state

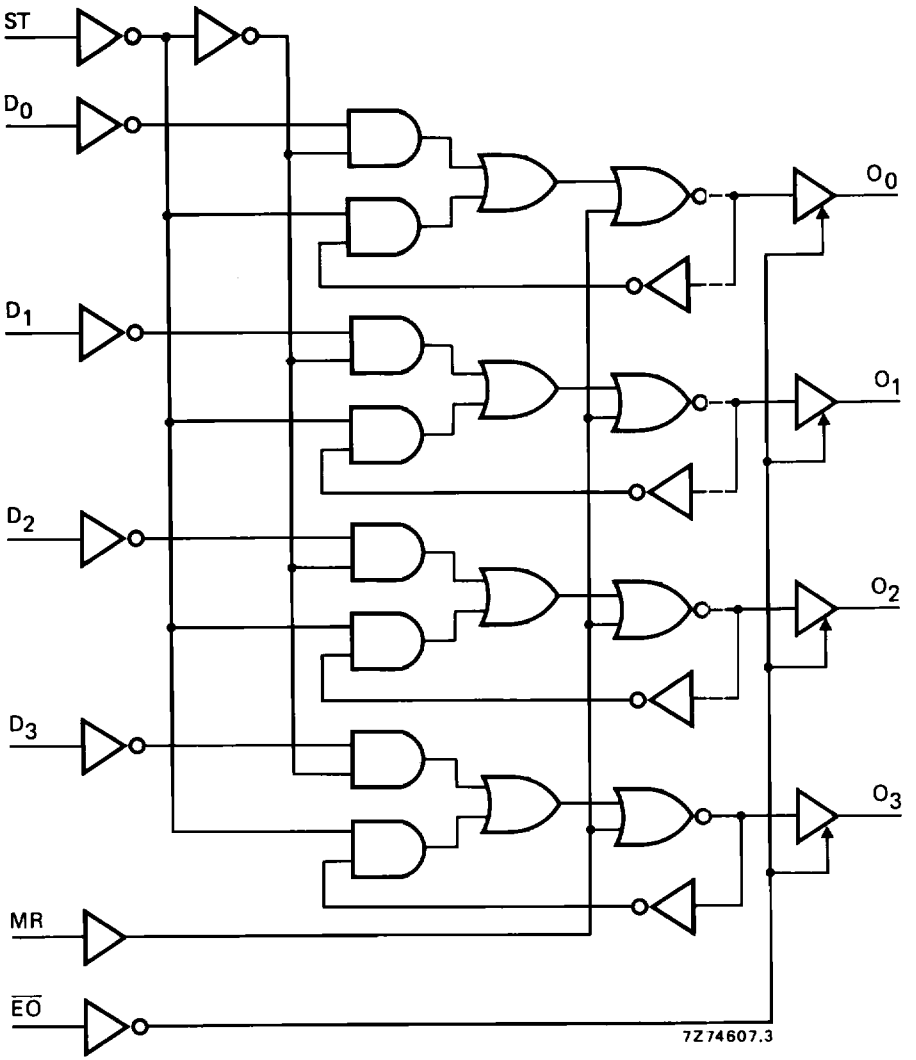

Fig. 3 Logic diagram (one 4-bit latch).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4.

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
ST → O_n	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
D_n → O_n	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
MR → O_n	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays							
Output enable times							
$\overline{EO}$ → O_n	5			45	90	ns	
HIGH	10	t_{PZH}		20	40	ns	
	15			18	36	ns	
	5			45	90	ns	
LOW	10	t_{PZL}		20	40	ns	
	15			18	36	ns	
Output disable times							
$\overline{EO}$ → O_n	5			35	70	ns	
HIGH	10	t_{PHZ}		20	40	ns	
	15			18	36	ns	
	5			45	90	ns	
LOW	10	t_{PLZ}		20	40	ns	
	15			18	36	ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum ST pulse width; HIGH	5	t_{WSTH}	50	25		ns	see also waveforms Fig. 4
	10		30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	40	20		ns	
	10		24	12		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	20	0		ns	
	10		20	0		ns	
	15		15	0		ns	
Set-up times $D_n \rightarrow$ ST	5	t_{su}	35	10		ns	
	10		25	5		ns	
	15		20	0		ns	
Hold times $D_n \rightarrow$ ST	5	t_{hold}	20	0		ns	
	10		20	0		ns	
	15		15	0		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$9\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$25\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

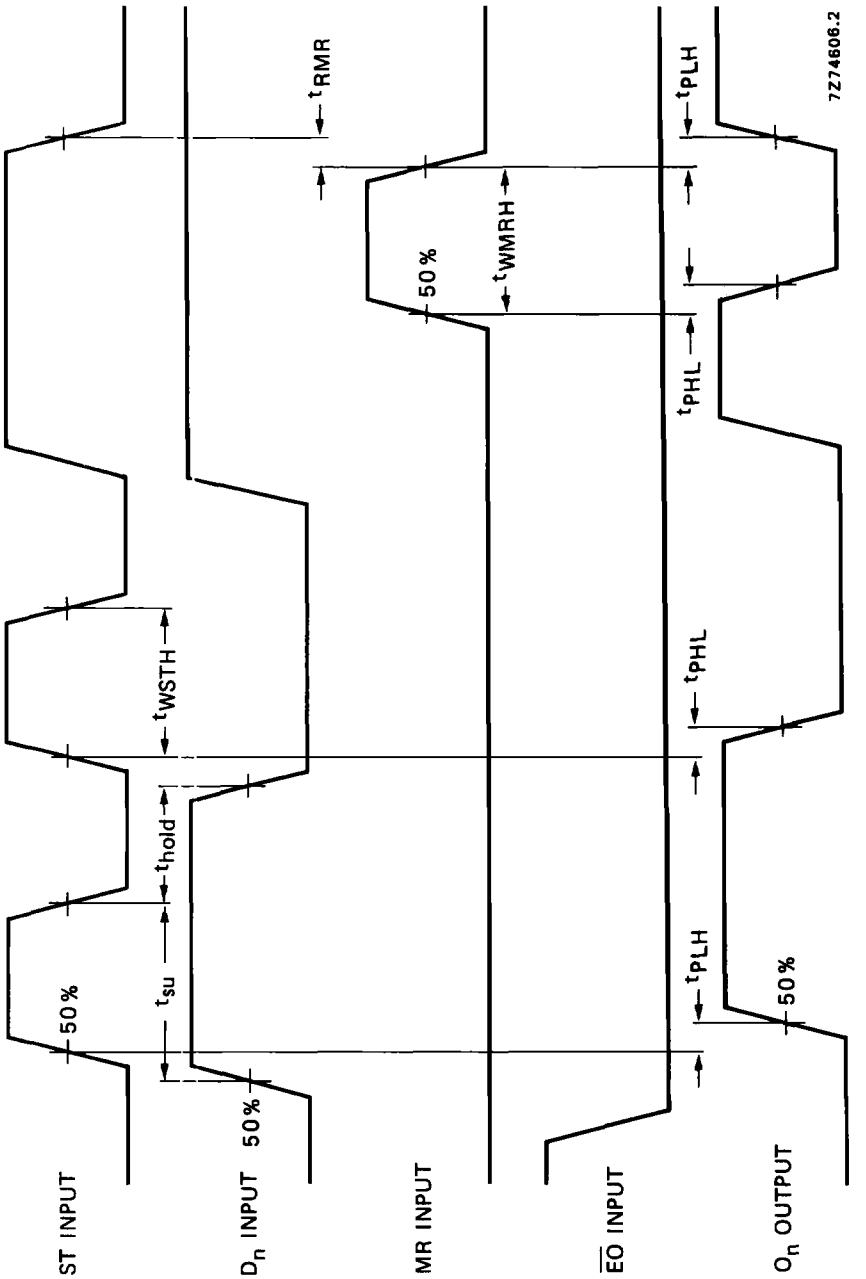

Fig. 4 Waveforms showing minimum ST and MR pulse widths, set-up and hold times for D_n to ST, recovery time for MR and propagation delays from ST to O_n, D_n to O_n and MR to O_n.

APPLICATION INFORMATION

Some examples of application for the HEF4508B are:

- Buffer storage
- Holding registers
- Data storage and multiplexing

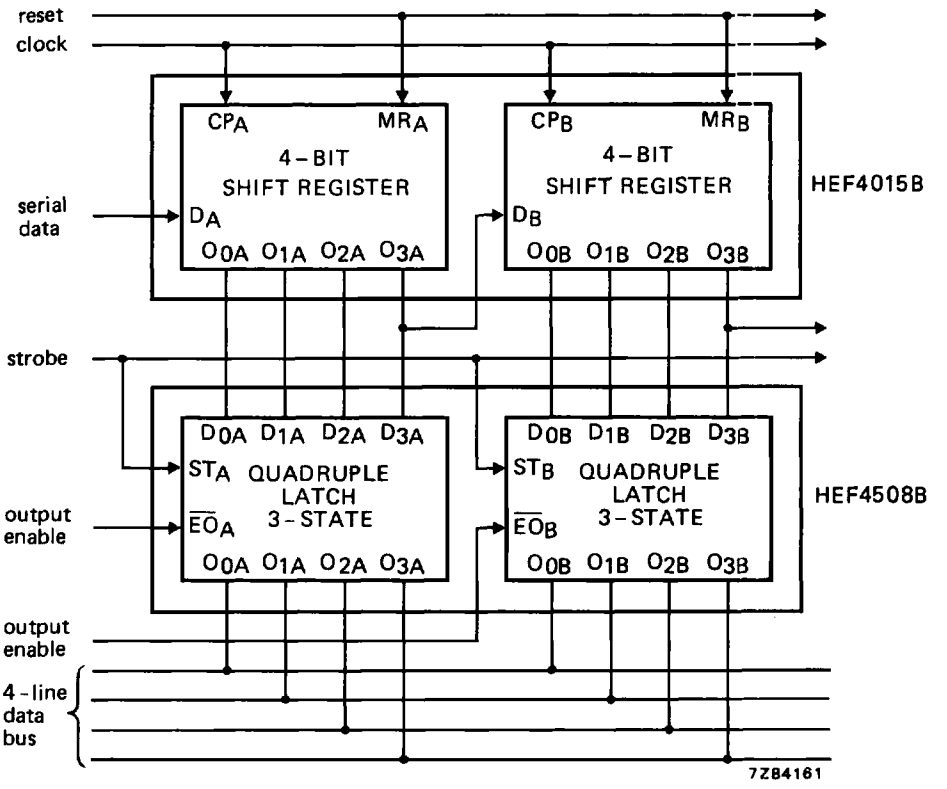

Fig. 5 Example of a bus register using HEF4508B and HEF4015B.

APPLICATION INFORMATION (continued)

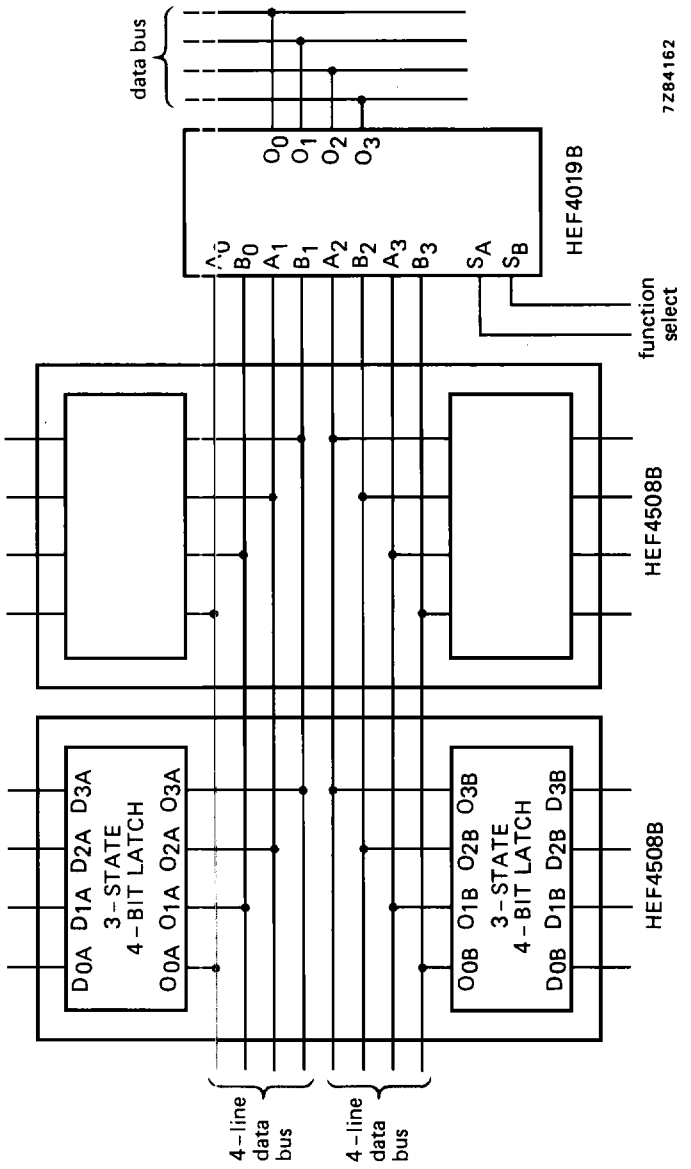

Fig. 6 Example of a dual multiplexed bus register with function select using two HEF4508B and one HEF4019B.

FUNCTION SELECT

S_A	S_B	function
L	L	inhibit (all L)
H	L	select A bus
L	H	select B bus
H	H	$A_1 + B_1$