NDA-322

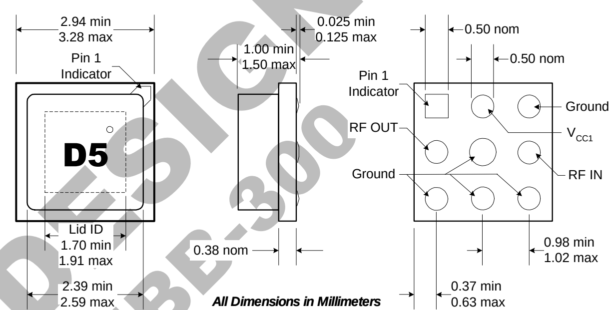
InGaP/GaAs HBT MMIC DISTRIBUTED AMPLIFIER DC TO 12GHz

Typical Applications

- Narrow and Broadband Commercial and Military Radio Designs
- Linear and Saturated Amplifiers
- Gain Stage or Driver Amplifiers for MWRadio/Optical Designs

Product Description

The NDA-322 Casacadable Broadband InGaP/GaAs MMIC amplifier is a low-cost, high-performance solution for high frequency RF, microwave, or optical amplification needs. This 50Ω gain block is based on a reliable HBT proprietary MMIC design, providing unsurpassed performance for small-signal applications. Designed with an external bias resistor, the NDA-322 provides flexibility and stability. In addition, the NDA-320-D chip was designed with an additional ground via, providing improved thermal resistance performance. The NDA-series of distributed amplifiers provide design flexibility by incorporating AGC functionality into their designs.

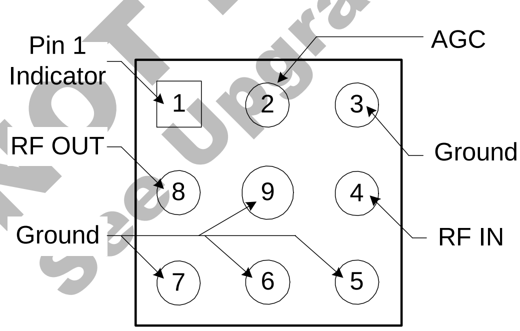


Notes:
1. Solder pads are coplanar to within ±0.025 mm.
2. Lid will be centered relative to frontside metallization with a tolerance of ±0.13 mm.
3. Mark to include two characters and dot to reference pin 1.

Package Style: MPGA, Bowtie, 3x3, Ceramic

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☑ InGaP/HBT
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaN HEMT
- ☐ GaAs MESFET
- ☐ Si CMOS
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- Reliable, Low-Cost HBT Design
- 9.0dB Gain/P1dB of 13.1dBm @ 2GHz
- Fixed Gain or AGC Operation
- 50Ω I/O Matched for High Freq. Use
- Secondary Ground-Via for Better Thermal Management

Ordering Information

NDA-322	InGaP/GaAs HBT MMIC Distributed Amplifier DC to 12GHz

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NDA-322

Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+20	dBm
Power Dissipation	300	mW
Device Current, I_{CC1}	42	mA
Device Current, I_{CC2}	48	mA
Junction Temperature, Tj	200	°C
Operating Temperature	-45 to +85	°C
Storage Temperature	-65 to +150	°C

Exceeding any one or a combination of these limits may cause permanent damage.

Caution! ESD sensitive device.

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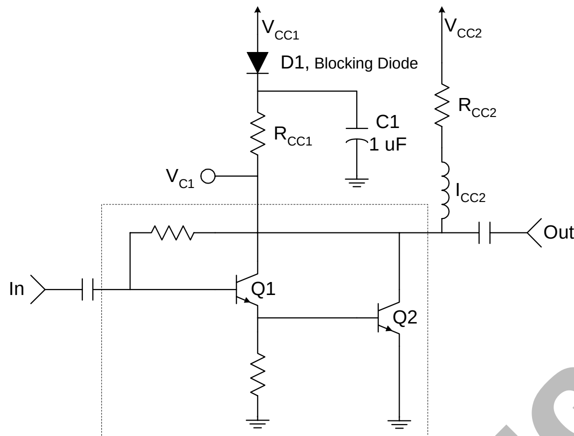
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC1}=+10V, V_{CC2}=+10V, V_{C1}=+4.75V, V_{C2}=+2.98V, I_{CC1}=24mA, I_{CC2}=40mA, Z_0=50Ω, T_A=+25°C
Small Signal Power Gain, S21	8.0	9.0		dB	f=0.1GHz to 6.0GHz
		10.0		dB	f=6.0GHz to 10.0GHz
	8.0	10.0		dB	f=10.0GHz to 12.0GHz
Gain Flatness		±0.6		dB	f=0.1GHz to 8.0GHz
Input and Output VSWR		1.9:1			f=0.1GHz to 10.0GHz
		1.9:1			f=10.0GHz to 12.0GHz
Bandwidth, BW		12.5		GHz	BW3 (3dB)
Output Power @ 1dB Compression		13.1		dBm	f=2.0GHz
		17.0		dBm	f=6.0GHz
		9.0		dBm	f=12.0GHz
Noise Figure, NF		6.4		dB	f=2.0GHz
Third Order Intercept, IP3		23.0		dBm	f=2.0GHz
Reverse Isolation, S12		-15		dB	f=0.1GHz to 12.0GHz
Device Voltage, V_Z		4.7		V	
AGC Control Voltage, V_{C1}	3.6	4.0	4.2	V	
Gain Temperature Coefficient, $\delta G_T/\delta T$		-0.0015		dB/°C	
MTTF versus Junction Temperature					
Case Temperature		85		°C	
Junction Temperature		113.9		°C	
MTTF		>1,000,000		hours	
Thermal Resistance					
θ_{JC}		124		°C/W	$\frac{J_T - T_{CASE}}{V_D \cdot I_{CC}} = \theta_{JC}(°C/Watt)$

Suggested Voltage Supply: $V_{CC1} \geq 4.7V$, $V_{CC2} \geq 5.0V$

Pin	Function	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
2	VCC1	AGC bias pin. Biasing is accomplished with an external series resistor to V_{CC1}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{CC1} - V_{DEVICE1})}{I_{CC1}}$$ Care should also be taken in the resistor selection to ensure that the current into the part never exceeds maximum datasheet operating (mA) over the planned operating temperature. This means that a resistor between the supply and this pin is always required, even if a supply near 5.0V is available, to provide DC feedback to prevent thermal runaway. Alternatively, a constant current supply circuit may be implemented. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
3	GND	Same as pin 1.	
4	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
5	GND	Same as pin 1.	
6	GND	Same as pin 1.	
7	GND	Same as pin 1.	
8	RF OUT AND VCC2	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC2}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{CC2} - V_{DEVICE2})}{I_{CC2}}$$ Care should also be taken in the resistor selection to ensure that the current into the part never exceeds maximum datasheet operating current (mA) over the planned operating temperature. This means that a resistor between the supply and this pin is always required, even if a supply near 5.0V is available, to provide DC feedback to prevent thermal runaway. Alternatively, a constant current supply circuit may be implemented. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
9	GND	Same as pin 1.	

Typical Bias Configuration

Application notes related to biasing circuit, device footprint, and thermal considerations are available on request.



Simplified Schematic of Distributed Amplifer

Bias Resistor Selection
R_{CC1}: For 4.7V<V_{CC1}<5.0V R_{CC1}=0Ω For 5.0V<V_{CC1}<10.0V R_{CC1}=V_{CC1}-4.7/0.024Ω
R_{CC2}: For 5.0V<V_{CC2}<10.0V R_{CC1}=V_{CC2}-2.9/0.040Ω

Typical Bias Parameters for V_{CC1}=V_{CC2}=10V:

V_{CC1} (V)	V_{CC2} (V)	I_{CC1} (mA)	V_{C1} (V)	R_{CC1} (Ω)	I_{CC2} (mA)	V_{C2} (V)	R_{CC2} (Ω)
10	10	24	4.75	220	40	2.9	150

Application Notes

Die Attach

The die attach process mechanically attaches the die to the circuit substrate. In addition, it electrically connects the ground to the trace on which the chip is mounted, and establishes the thermal path by which heat can leave the chip.

Assembly Procedure

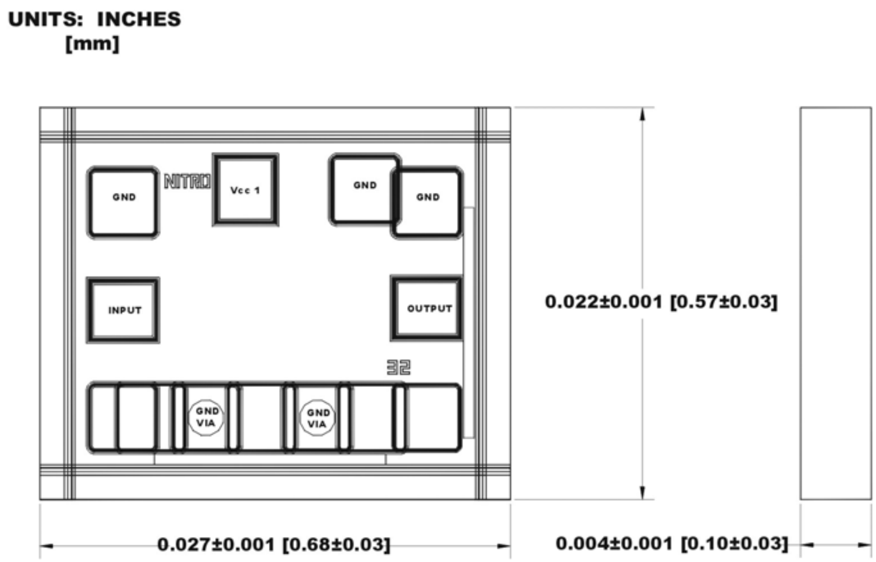
Epoxy or eutectic die attach are both acceptable attachment methods. Top and bottom metallization are gold. Conductive silver-filled epoxies are recommended. This procedure involves the use of epoxy to form a joint between the backside gold of the chip and the metallized area of the substrate. A 150°C cure for 1 hour is necessary. Recommended epoxy is Ablebond 84-1LMI from Ablestik.

Bonding Temperature (Wedge or Ball)

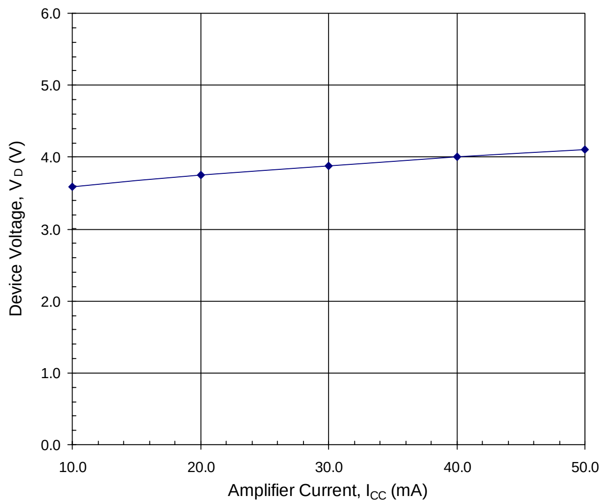
It is recommended that the heater block temperature be set to 160°C±10°C.

Chip Outline Drawing - NDA-320-D

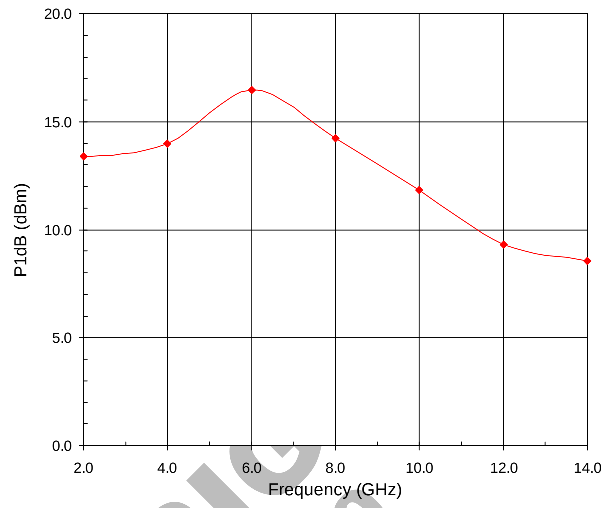
Chip Dimensions: 0.027” x 0.022” x 0.004”



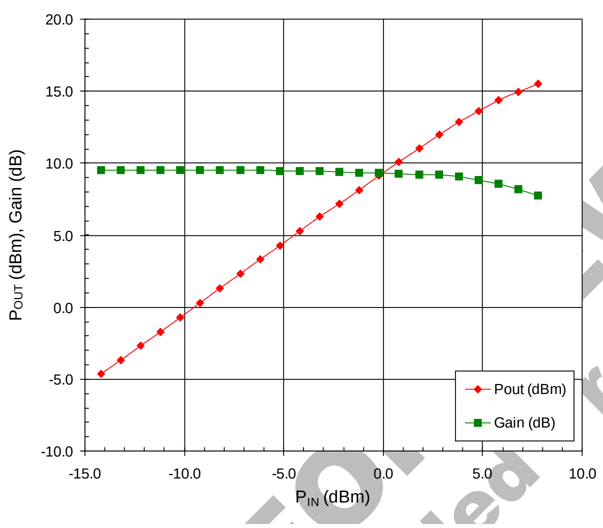
Device Voltage versus Amplifier Current



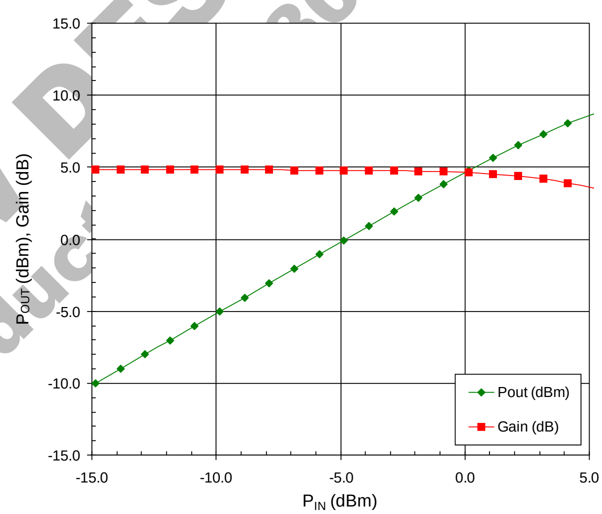
P1dB versus Frequency at 25°C



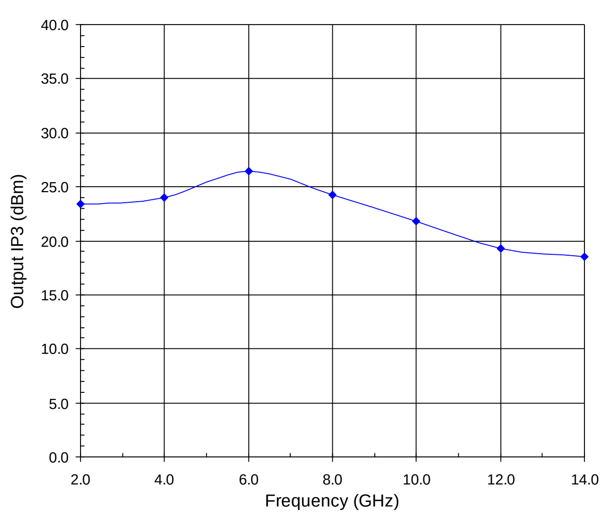
P_{OUT}/Gain versus P_{IN} at 6 GHz



P_{OUT}/Gain versus P_{IN} at 14 GHz



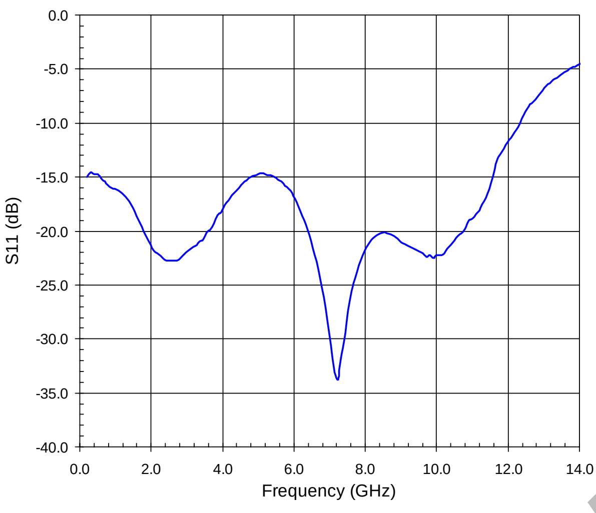
Third Order Intercept versus Frequency at 25°C



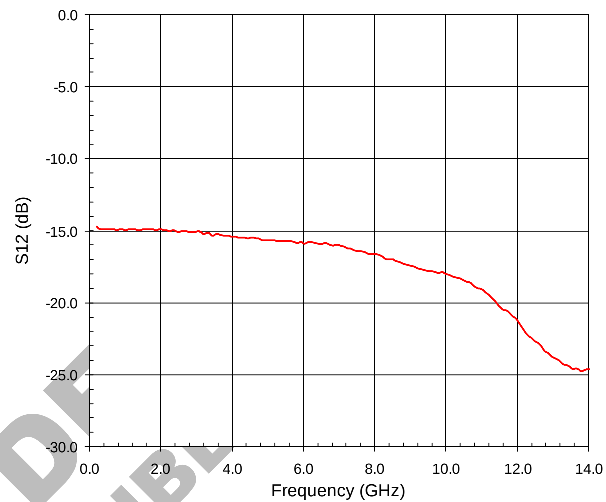
The s-parameter gain results shown below include device performance as well as evaluation board and connector loss variations. The insertion losses of the evaluation board and connectors are as follows:

1GHz to 4GHz=-0.06dB
5GHz to 9GHz=-0.22dB
10GHz to 14GHz=-0.50dB
15GHz to 20GHz=-1.08dB

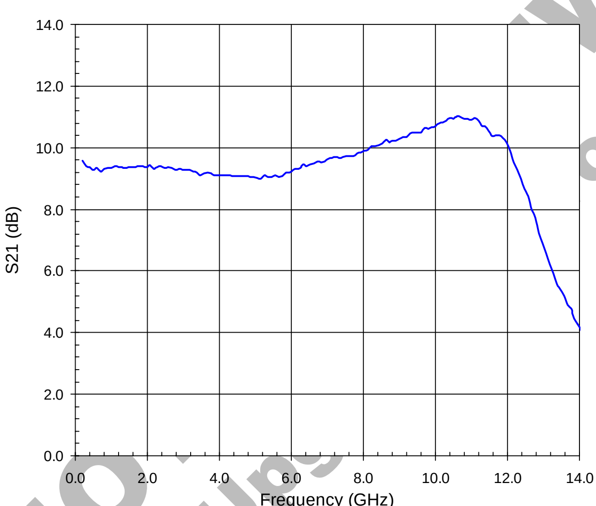
S11 versus Frequency



S12 versus Frequency



S21 versus Frequency



S22 versus Frequency