SN54AS29825, SN54AS29826, SN74AS29825, SN74AS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, MAY 1986

- **Designed to be Interchangeable with AMD's AM29825 and AM29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Production Circuitry**
- **Power-Up High Impedance State**
- **Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Dependable Texas Instruments Quality and Reliability**

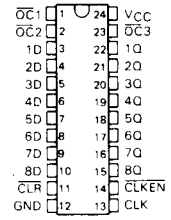
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

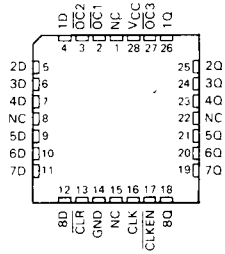
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'AS29825 has noninverting D inputs and the 'AS29826 has inverting D inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

The buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

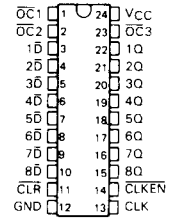
SN54AS29825 . . . JT PACKAGE
SN74AS29825 . . . DW OR NT PACKAGE
(TOP VIEW)



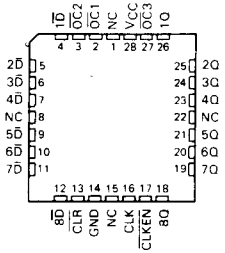
SN54AS29825 . . . FK PACKAGE
SN74AS29825 . . . FN PACKAGE
(TOP VIEW)



SN54AS29826 . . . JT PACKAGE
SN74AS29826 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS29826 . . . FK PACKAGE
SN74AS29826 . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

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The SN54AS29825 and SN54AS29826 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29825 and SN74AS29826 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'AS29825

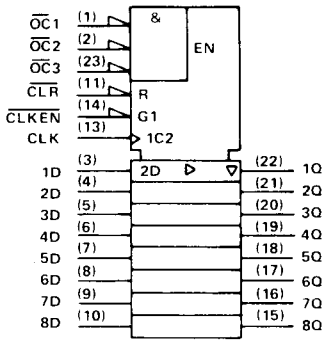
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS29826

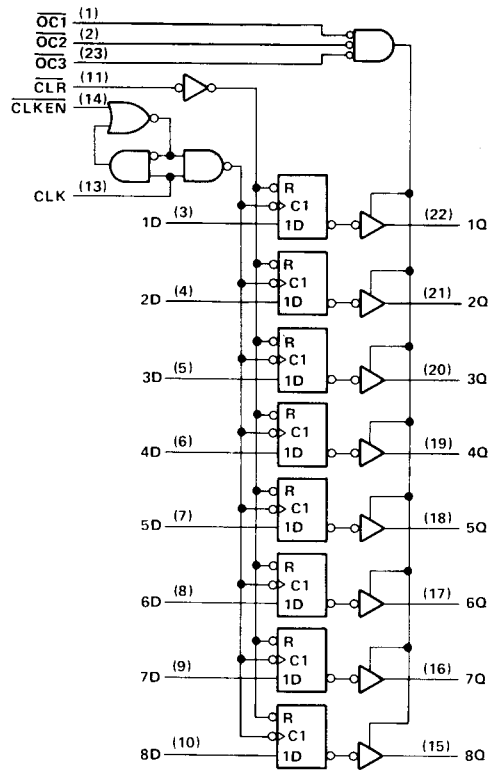
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'AS29825 logic symbol†



'AS29825 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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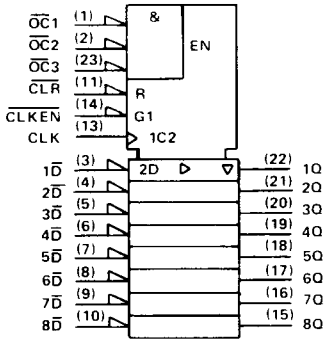
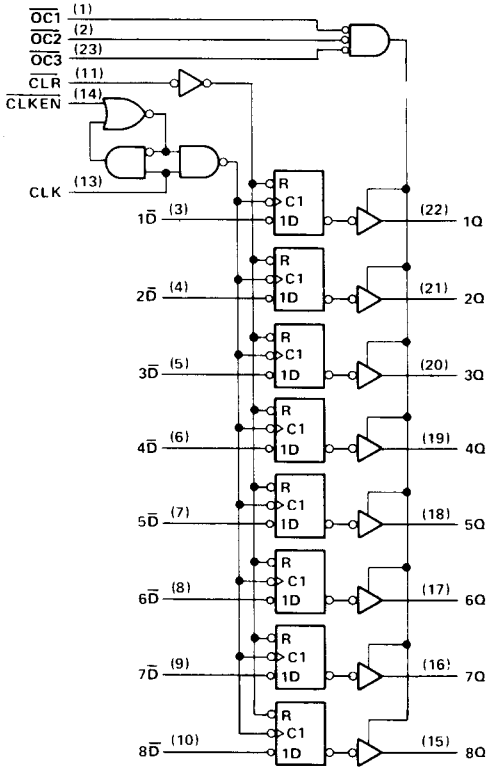
'AS29826 logic symbol†



'AS29826 logic diagram (positive logic)



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Pin numbers shown are for DW, JT, and NT packages.