DATA SHEET

74AC16374/74ACT16374

16-bit edge-triggered D-type flip-flop (3-State)

Product specification

1997 Aug 01

Philips Semiconductors

PHILIPS

16-bit edge triggered D-type flip-flop (3-State)

74AC16374
74ACT16374

FEATURES

- 74ACT16374 has TTL-compatible inputs
- 74AC16374 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Distributed power and ground pins for minimum noise and ground bounce

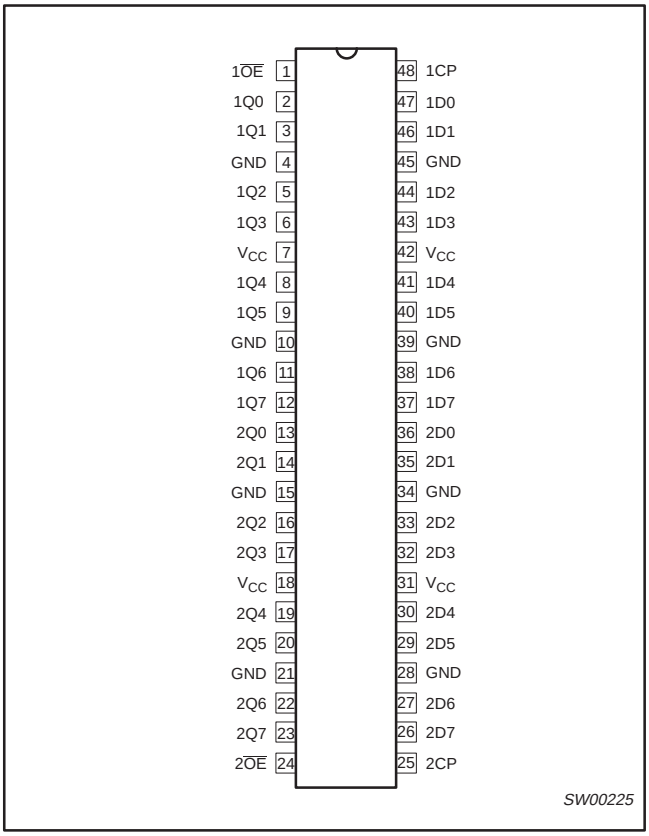
DESCRIPTION

The 74AC16374/74ACT16374 is a 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. The '16374' consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided for each octal.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC V_{CC} = 3.3V	AC V_{CC} = 5.0V	ACT V_{CC} = 5.0V	
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 50pF	4.2	2.9	4.6	ns
f_{max}	Maximum clock frequency	C_L = 50pF	160	200	180	MHz
C_I	Input capacitance		4.5			pF
C_{PD}	Power dissipation capacitance	V_I = GND to V_{CC}[1]				pF
		Outputs enabled[2]	27		30	pF
		Outputs enabled[3]	220		250	pF
		Outputs disabled[2]	15		17	pF
		Outputs disabled[3]	60		70	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. Switch the clock and one data input such that one flip-flop toggles.
3. Switch the clocks and all data inputs such that all 16 flip-flops toggle.

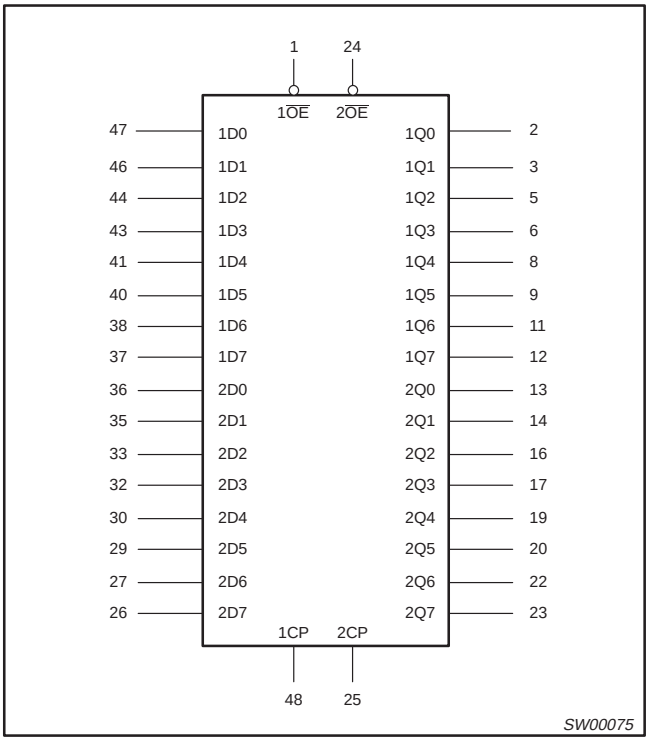
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74AC16374 DL 74ACT16374 DL	7AC16374 DL 7AT16374 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74AC16374 DGG 74ACT16374 DGG	7AC16374 DGG 7AT16374 DGG	SOT362-1

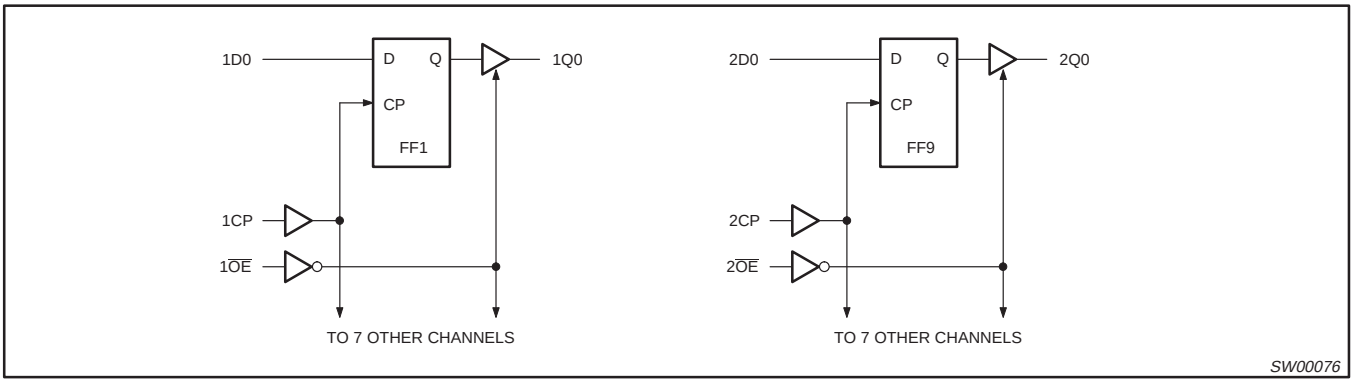
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q1 to 1Q7	3-State flip-flop outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q1 to 2Q7	3-State flip-flop outputs
24	$2\overline{OE}$	Output enable input (active LOW)
25	2CP	Clock input
36, 35, 33, 32, 30, 29, 27, 26	2D1 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D1 to 1D7	Data inputs
48	1CP	Clock input

LOGIC SYMBOL



LOGIC DIAGRAM

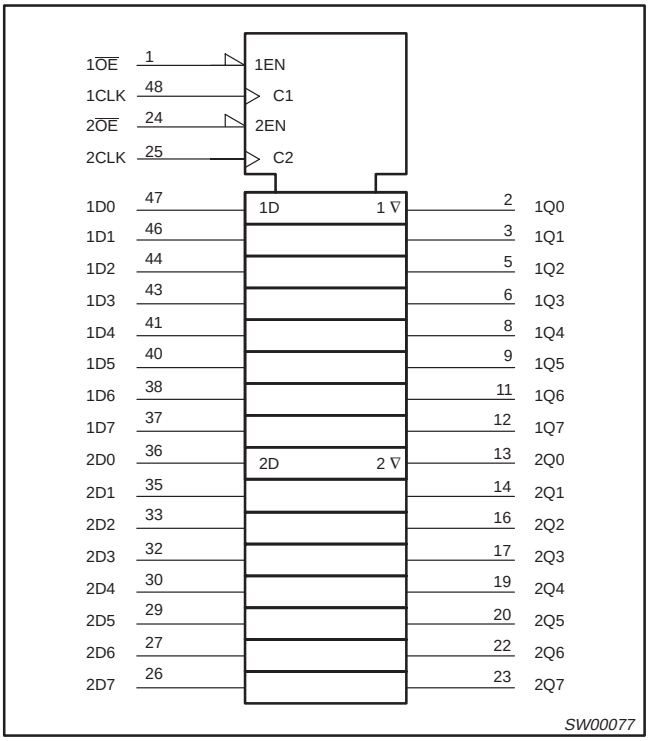


FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0 to Q7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage for 'AC	2.0	6.0	V
V_{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V_{IN}	DC input voltage range	0	V_{CC}	V
V_O	DC output voltage range	0	V_{CC}	V
T_{amb}	Operating free-air temperature range	–40	+85	°C
$\Delta V/\Delta t$	Minimum input edge rate — AC devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125		

ABSOLUTE MAXIMUM RATINGS[1]

in accordance with the Absolute Maximum Rating System (IEC134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	V_{IN} = –0.5V	–20	mA
		V_{IN} = V_{CC} + 0.5V	+20	
V_{IN}	DC input voltage		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	V_O = –0.5V	–20	mA
		V_O = V_{CC} + 0.5V	+20	
V_O	DC output voltage		–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current per output		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		± 200	mA
T_{stg}	Storage temperature range		–65 to 150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (74AC16374)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –12mA[1]	3.0	2.46			V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76			
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76			
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12mA[1]	3.0			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			±1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} = V_{IL}, V_{IH} V_{OUT} = V_{CC}, GND	5.5			±2.5	μA
I_{OLD}	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			80	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

DC ELECTRICAL CHARACTERISTICS (74ACT16374)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76	3.86		V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76	4.86		
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			± 1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} = V_{IL}, V_{IH} V_{OUT} = V_{CC}, GND	5.5			± 2.5	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{IN} = V_{CC} – 2.1V Other inputs at V_{CC} or GND; I_{OUT} = 0	5.5			1.0	mA
I_{OLD}	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			80	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0ms, one output loaded at a time

In accordance with the Absolute Maximum Rating System (IEC 134)

AC CHARACTERISTICS (74AC16374)

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1]	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay CP to Q_n	3.3 5.0	2.0 1.5	4.2 2.9	9 7	1.5 1.0	10 8	ns	1, 4
t_{PHL}	Propagation delay CP to Q_n	3.3 5.0	2.0 1.5	4.2 2.9	9 7	1.5 1.0	10 8	ns	1, 4
t_{PZH}	3-State output enable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	4.4 3.0	9 7	1.5 1.0	10 8	ns	2, 4
t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	4.3 3.0	9 7	1.5 1.0	10 8	ns	2, 4
t_{PHZ}	3-State output disable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	3.3 2.2	8 6	1.5 1.0	9 7	ns	2, 4
t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	4.1 2.9	8 6	1.5 1.0	9 7	ns	2, 4
t_w	CP pulse width HIGH or LOW	3.3 5.0	4.5 4.0	1.6 1.4		5 4.5		ns	3
t_{su}	Set-up time D_n to CP	3.3 5.0	1.5 1.5	0.2 0.2		2 2		ns	3
t_h	Hold time D_n to CP	3.3 5.0	1.0 1.0	0 0.2		1.5 1.5		ns	3
f_{max}	Maximum clock pulse frequency	3.3 5.0	100 150	160 200		90 140		MHz	

NOTE:
1. Voltage range 3.3V is V_{CC} = 3.3V ± 0.3V
   Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

AC CHARACTERISTICS (74ACT16374)

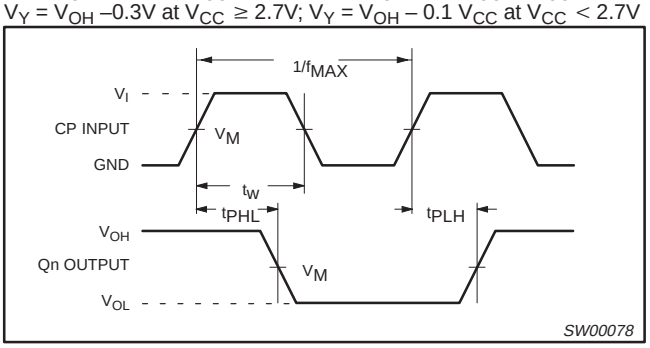
GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1]	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay CP to Q_n	5.0	2.0	4.6	9	2.0	10	ns	1, 4
t_{PHL}	Propagation delay CP to Q_n	5.0	2.0	4.6	9	1.5	10	ns	1, 4
t_{PZH}	3-State output enable time $\overline{OE}$ to Q_n	5.0	2.0	4.3	9	1.5	10	ns	2, 4
t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	5.0	1.5	4.3	9	1.5	10	ns	2, 4
t_{PHZ}	3-State output disable time $\overline{OE}$ to Q_n	5.0	1.5	3.9	8	1.0	9	ns	2, 4
t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	5.0	1.5	4.5	8	1.0	9	ns	2, 4
t_w	CP pulse width HIGH or LOW	5.0	4.0	1.6		4.5		ns	3
t_{su}	Set-up time D_n to CP	5.0	1.5	–0.2		2		ns	3
t_h	Hold time D_n to CP	5.0	1.5	0.4		2		ns	3
f_{max}	Maximum clock pulse frequency	5.0	120	180		110		MHz	

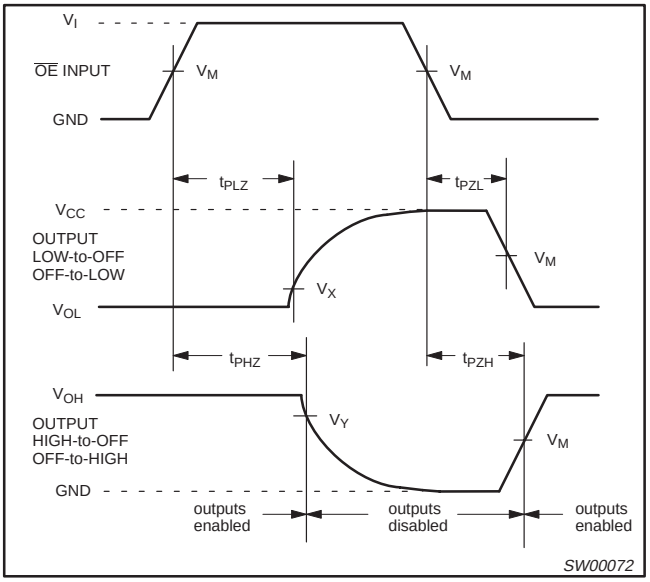
NOTE:
1. These values are at V_{CC} = 5.0V ± 0.5V

AC WAVEFORMS

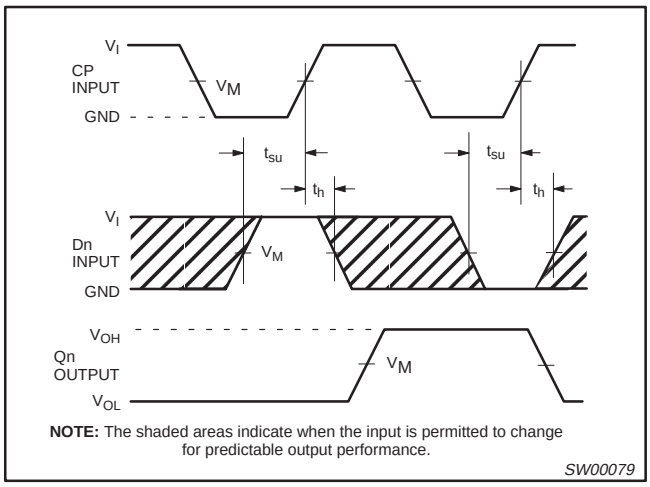
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V



Waveform 1. Clock (CP) to output (Qn) propagation delays, the clock pulse width and the maximum clock pulse frequency

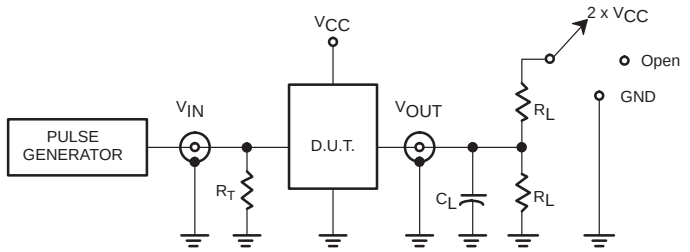


Waveform 2. 3-State enable and disable times



Waveform 3. Data set-up and hold times for the Dn input to the CP input

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

FAMILY	V_{IN} Input Requirements	V_m Input	V_m Output
AC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
ACT	GND to 3.0V	1.5V	50% V_{CC}

DEFINITIONS

R_L = Load resistor; see AC Characteristics for value.

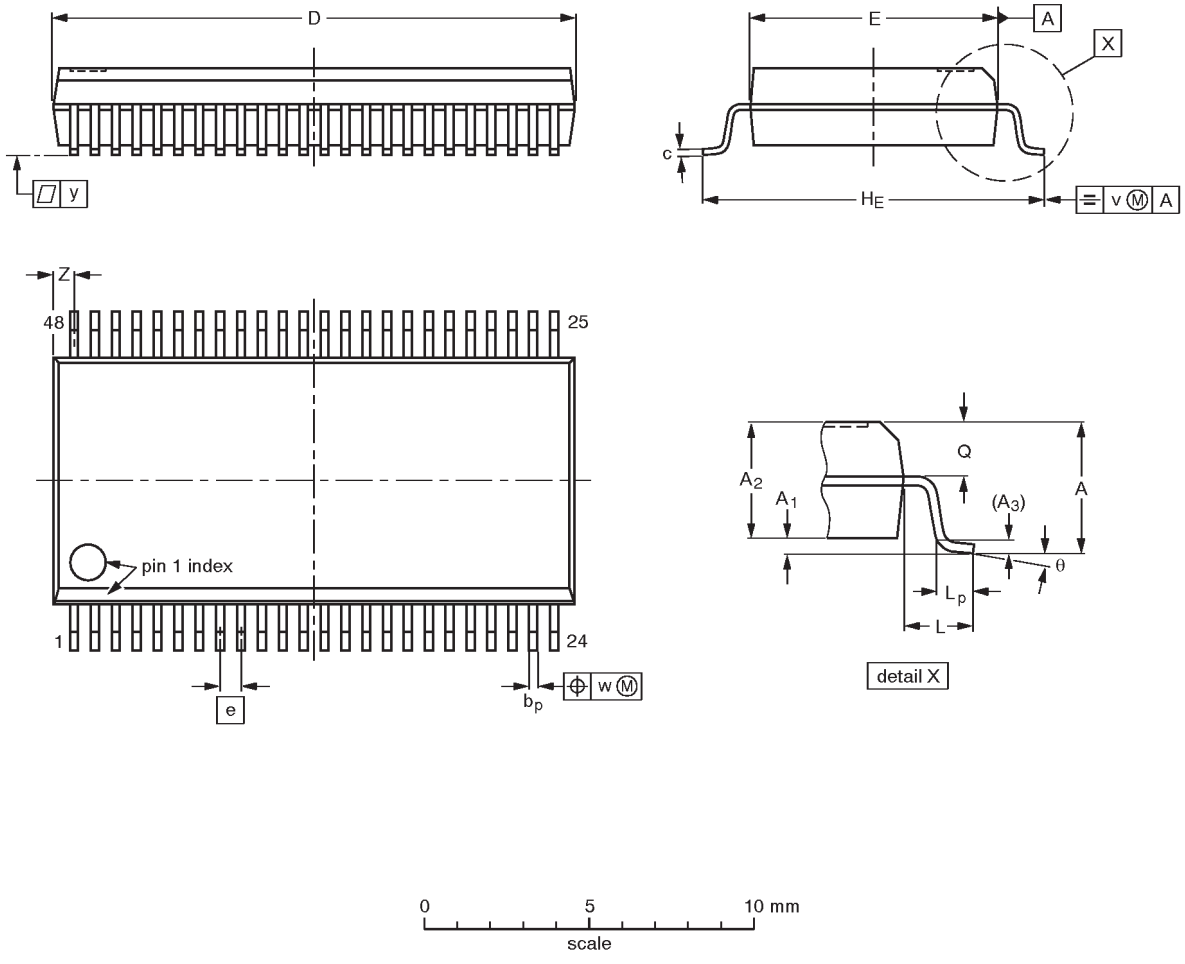
C_L = Load capacitance, see AC characteristics

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00302

Waveform 4. Load circuitry for switching times

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

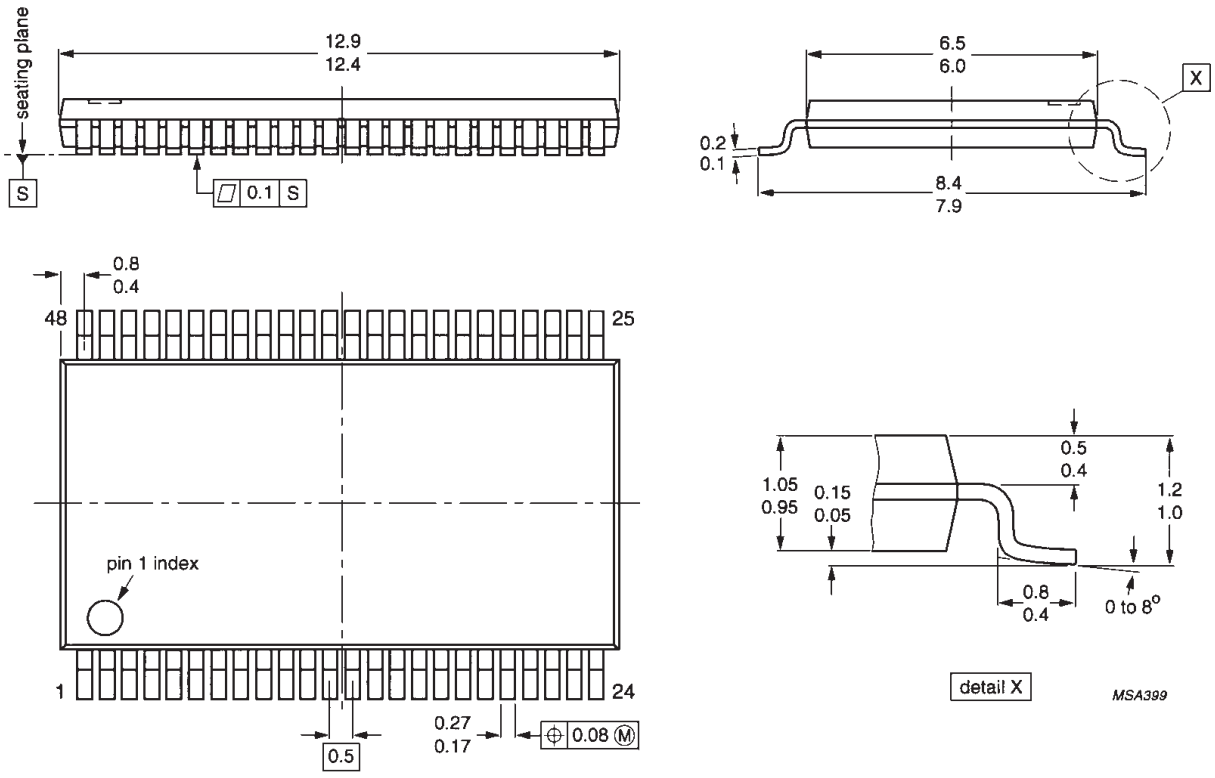
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm **SOT362-1**



Dimensions in mm.

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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