GALVANTECH, INC.

GVT73024UL8
ULTRA LOW POWER 128K X 8 SRAM

ASYNCHRONOUS ULTRA LOW POWER FULL CMOS SRAM

128K x 8 SRAM

LOW POWER SUPPLY VOLTAGE
LOW STANDBY CURRENT

FEATURE

- Low standby current: 5ua (max.)
- Low operating current: 1.5mA/MHz (typ.)
- Wide power supply voltage range:
  3.0V to 3.6V for GVT73024UL8XX family
  2.7V to 3.3V for GVT73024UL8XXB family
  2.3V to 2.7V for GVT73024UL8XXC family
  1.8V to 2.2V for GVT73024UL8XXD family
- Low data retention voltage: 1.5V (Min)
- Full CMOS 6-transistor memory cell
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- Easy memory expansion with CE1#, CE2 and OE# options
- Automactic power-down when deselected

OPTIONS — MARKING

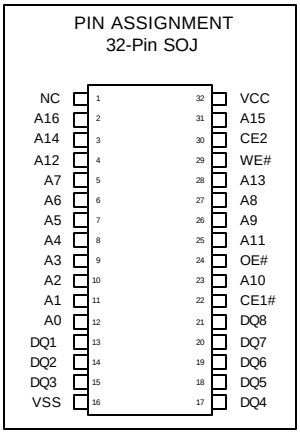
- Power supply voltage
  - 3.3V ± 0.3V — -None
  - 3.0V ± 0.3V — -B
  - 2.5V ± 0.2V — -C
  - 2.0V ± 0.2V — -D
- Timing
  - 55ns access — -55
  - 70ns access — -70
  - 85ns access — -85
  - 100ns access — -100
  - 300ns access — -300
- Packages
  - 32-pin SOJ (300 mil) — SJ
  - 32-pin TSOP (type I) — TS
  - 32-pin sTSOP (type I) — ST
- Temperature
  - Commercial — None — (0°C to 70°C)
  - Industrial — I — (-40°C to 85°C)

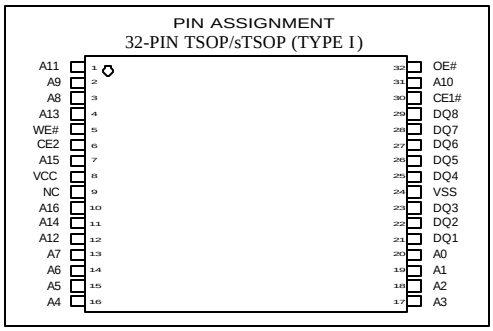
GENERAL DESCRIPTION

The GVT73024UL8 is organized as a 131,072 x 8 SRAM using a six-transistor full CMOS memory cell along with low-power CMOS process, using double-layer polysilicon, double-layer metal technology.

Static design eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers two chip enables (CE1# and CE2) along with output enable (OE#) for this organization.

The chip is enabled when CE1# is LOW and CE2 is HIGH. With chip being enabled, writing to this device is accomplished when write enable (WE#) is LOW and reading is accomplished when (OE#) go LOW with (WE#) remaining HIGH. The device offers a low power standby mode when chip is not selected. This allows system designers to meet low standby power requirements.





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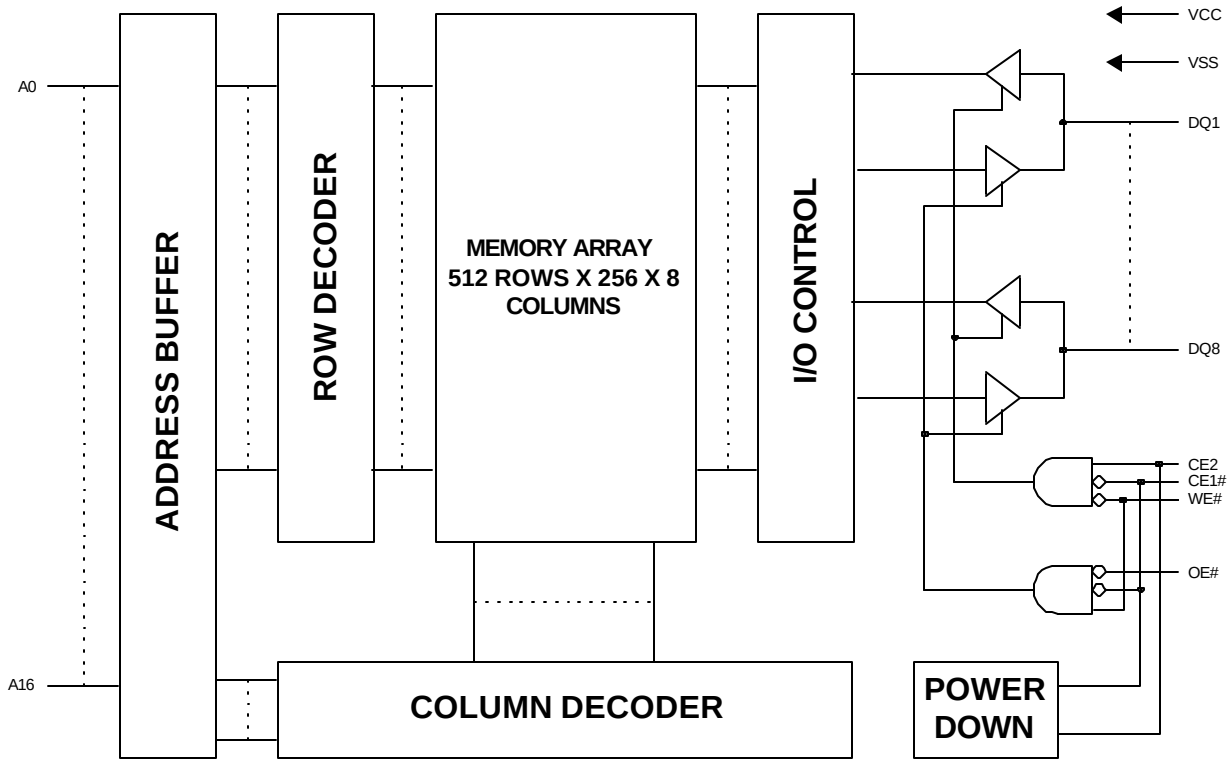
Rev. 8/99

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE1#	CE2	WE#	OE#	DQ	POWER
READ	L	H	H	L	Q	ACTIVE
WRITE	L	H	L	X	D	ACTIVE
OUTPUT DISABLE	L	H	H	H	HIGH-Z	ACTIVE
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY

PIN DESCRIPTIONS

SOJ Pin Numbers	TSOP & sTSOP Pin Numbers	SYMBOL	TYPE	DESCRIPTION
12, 11, 10, 9, 8, 7, 6, 5, 27, 28, 23, 25, 4, 28, 3, 31, 2	20, 19, 18, 17, 16, 15, 14, 13, 3, 2, 31, 1, 12, 4, 11, 7, 10	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
29	5	WE#	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. WE# is LOW for a WRITE cycle and HIGH for a READ cycle.
22, 30	30, 6	CE1#, CE2	Input	Chip Enables: These inputs are used to enable the device. When CE1# is LOW and CE2 is HIGH, the chip is selected. When either CE1# is HIGH or CE2 is LOW, the chip is disabled and automatically goes into standby power mode.
24	32	OE#	Input	Output Enable: This active LOW input enables the output drivers.
13, 14, 15, 17, 18, 19, 20, 21	21, 22, 23, 25, 26, 27, 28, 29	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and data outputs.
32	8	VCC	Supply	Power Supply: 1.8V to 3.6V, depending upon the product family.
16	24	VSS	Supply	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.3V to +4.0V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-65°C to +150°C
Power Dissipation 0.7W
Soldering Temperature (10s) .....260°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

DESCRIPTION	SYMBOL	PRODUCT	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VCC	GVT73024UL8XX	3.0	3.3	3.6	V	1
		GVT73024UL8XXB	2.7	3.0	3.3		
		GVT73024UL8XXC	2.3	2.5	2.7		
		GVT73024UL8XXD	1.8	2.0	2.2		
Input High (Logic 1) voltage	V_{IH}	GVT73024UL8XX	2.2	-	VCC+0.2	V	1, 2
		GVT73024UL8XXB	2.2				
		GVT73024UL8XXC	2.0				
		GVT73024UL8XXD	1.6				
Input Low (Logic 0) Voltage	V_{IL}		-0.2		0.4	V	1, 2

DC AND OPERATING ELECTRICAL CHARACTERISTICS

(All Temperature Ranges; VCC = 1.8 V to 3.6V. unless otherwise noted, V_{LC}=0.2V, V_{HC}=VCC-0.2V)

DESCRIPTION	SYM	CONDITIONS		MIN.	TYP.	MAX.	UNITS	NOTES
Input Leakage Current	IL_I	0V ≤ V_{IN} ≤ VCC		-1		1	uA	
Output Leakage Current	IL_O	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC		-1		1	uA	
Operating Power Supply Current	Icc1	Cycle Time=1us; CE1# = V_{IL} & CE2 = V_{IH};Other Inputs = V_{IH}/V_{IL}; I_{OUT} = 0mA		-	1.5	3	mA	3, 14
	Icc2	Cycle Time=Min; CE1# = V_{IL} & CE2 = V_{IH};Other Inputs = V_{IH}/V_{IL}; I_{OUT} = 0mA	VCC=3.6V@55ns	-	-	55	mA	3
			VCC=3.3V@70ns	-	-	50		
			VCC=2.7V@85ns	-	-	30		
			VCC=2.2V@300ns	-	-	15		
TTL Standby Current	I_{SB}	CE1# ≥ V_{IH} or CE2 ≤ V_{IL}; Other Inputs=V_{IH} or V_{IL}; f= 0		-	-	0.3	mA	
CMOS Standby Current	I_{SB1}	CE1# ≥ V_{HC} or CE2≤ V_{LC}; Other Inputs=V_{HC} or V_{LC}; f= 0		-	-	5	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA @ VCC=2.7V I_{OL} = 0.5mA @ VCC=2.3V I_{OL} = 0.33mA @ VCC=1.8V		-	-	0.4	V	1
Output High Voltage	V_{OH}	I_{OH} = -1.0mA @ VCC=3.0V		2.4	-	-	V	1
		I_{OH} = -0.5mA @ VCC=2.5V		2.0	-	-		
		I_{OH} = -0.44mA @ VCC=2.0V		1.6	-	-		

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 3V	C_I	6	pF	4
Input/Output Capacitance (DQ)		$C_{I/O}$	8	pF	4

PRODUCT LIST

Part Name	Voltage Range & Speed Grade
GVT73024UL8XX	3.3V ± 0.3V; 55ns, 70ns, 85ns and 100ns
GVT73024UL8XXB	3.0V ± 0.3V; 55ns, 70ns, 85ns and 100ns
GVT73024UL8XXC	2.5V ± 0.2V; 70ns, 85ns and 100ns
GVT73024UL8XXD	2.0V ± 0.2V; 300ns

AC ELECTRICAL CHARACTERISTICS (Note 5)

(All Temperature Ranges; VCC = 3.0V to 3.6V for GVT73024ULXX family; VCC = 2.7V to 3.3V for GVT73024ULXXB family; VCC = 2.3V to 2.7V for GVT73024ULXXC family; VCC = 1.8V to 2.2V for GVT73024ULXX family))

DESCRIPTION		-55		-70		-85		-100		-300			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	55		70		85		100		300		ns	
Address access time	^tAA		55		70		85		100		300	ns	13
Chip Enable access time	^tACE		55		70		85		100		300	ns	13
Output hold from address change	^tOH	10		10		15		15		30		ns	
Chip Enable to output in Low-Z	^tLZCE	10		10		10		10		50		ns	4, 7
Chip disable to output in High-Z	^tHZCE		20		25		25		25		60	ns	4, 6, 7
Output Enable access time	^tAOE		20		30		40		50		150	ns	13
Output Enable to output in Low-Z	^tLZOE	5		5		5		5		30		ns	4, 7
Output Enable to output in High-Z	^tHZOE		20		25		25		25		60	ns	4, 6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		55		70		85		100		300	ns	4
WRITE Cycle													
WRITE cycle time	^tWC	55		70		85		100		300		ns	
Chip Enable to end of write	^tCW	40		45		50		60		300		ns	
Address valid to end of write, with OE# HIGH	^tAW	40		45		50		60		300		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP2$	40		45		50		60		200		ns	
WRITE pulse width, with OE# HIGH	$^tWP1$	40		45		50		60		200		ns	
Data setup time	^tDS	25		30		35		40		120		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		20		ns	4, 7
Write Enable to output in High-Z	^tHZWE		20		25		25		25		60	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	0.4V to 2.4V for VCC=3.3V &3.0V; 0.4V to 2.2V for VCC=2.5V; 0.4V to 1.8V for VCC=2.0V
Input rise and fall times	5ns
Input and output reference levels	1.5V for VCC=3.3V and 3.0V; 1.1V for VCC=2.5V; 0.9V for VCC=2.0V
Output load	C_L = 100pF and 1 TTL Gate

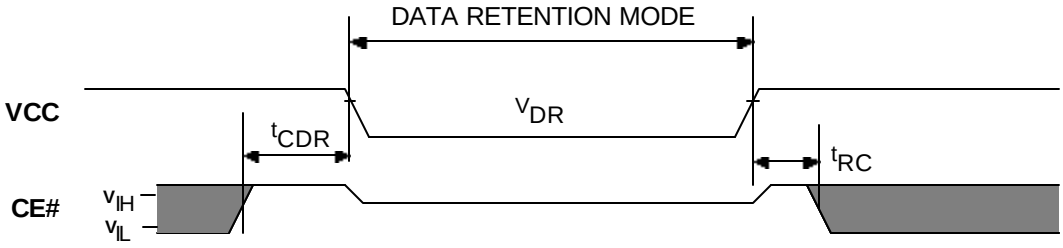
NOTES

1. All voltages referenced to VSS (GND).
2. Undershoot: $V_{IL} \leq$ -1.0V for t ≤ 20ns
   Overshoot: $V_{IH} \geq$ VCC+1.0V for t ≤ 20ns
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in the table of AC Test Conditions unless otherwise noted.
6. High-Z is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE and ^tHZWE is less than ^tLZWE.
8. WE# is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip Enable and Write Enable can initiate and terminate a WRITE cycle.
13. Capacitance derating applies to capacitance different from the load capacitance shown in AC Test Condition table.
14. Typical values are measured at 3.3V and 25ºC.

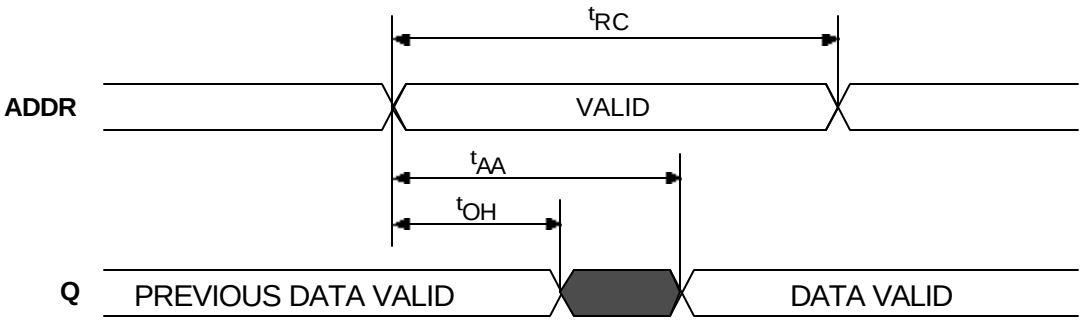
DATA RETENTION ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	1.5	-	3.6	V	1
Data Retention Current	CE1# ≥VCC -0.2 or CE2≤ VSS +0.2; all other inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; f= 0;Vcc = 3.0V	I_{CCDR}	-	-	5	uA	
Chip Deselect to Data Retention Time		t_{CDR}	0	-	-	ns	4
Operation Recovery Time		t_R	t_{RC}	-	-	ns	4, 11

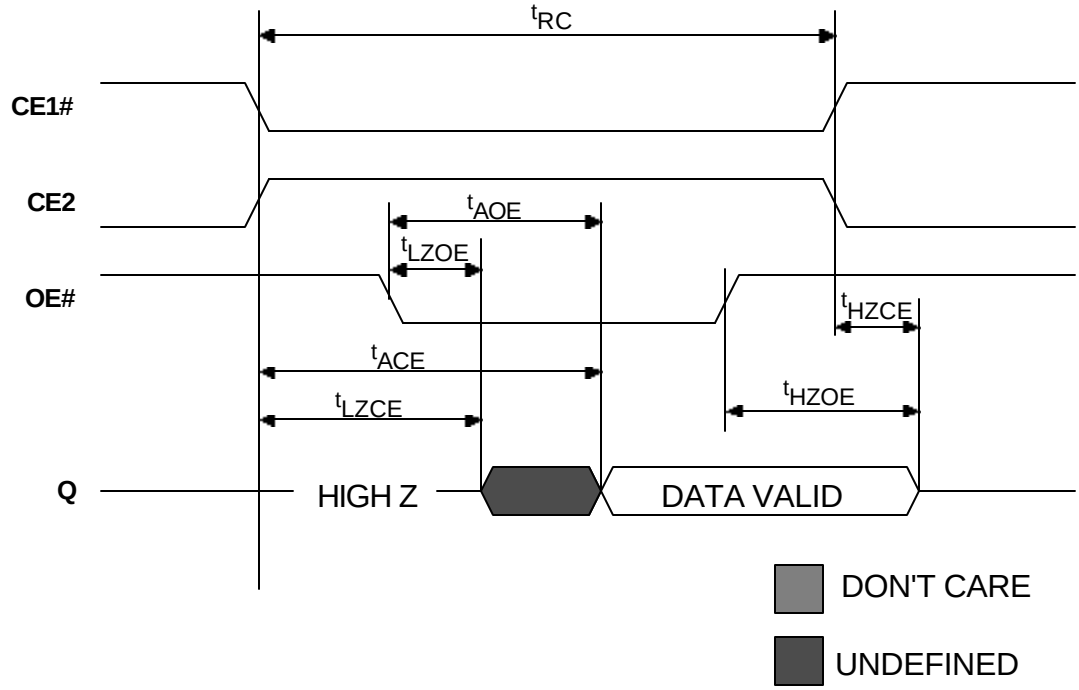
LOW VCC DATA RETENTION WAVEFORM



READ CYCLE NO. 1 (8, 9)

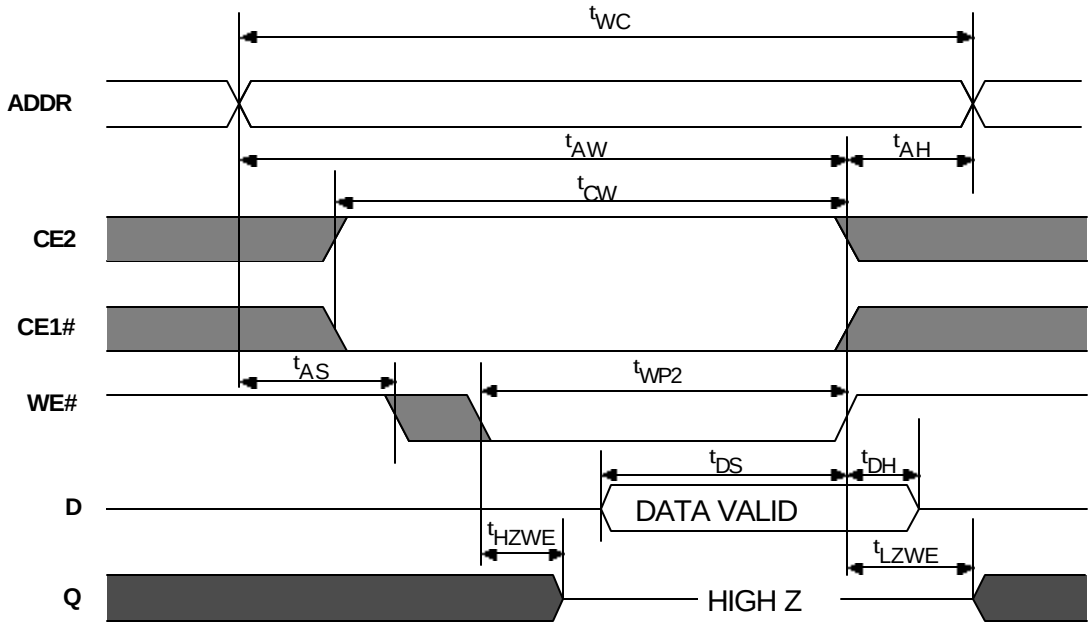


READ CYCLE NO. 2 (7, 8, 10, 12)



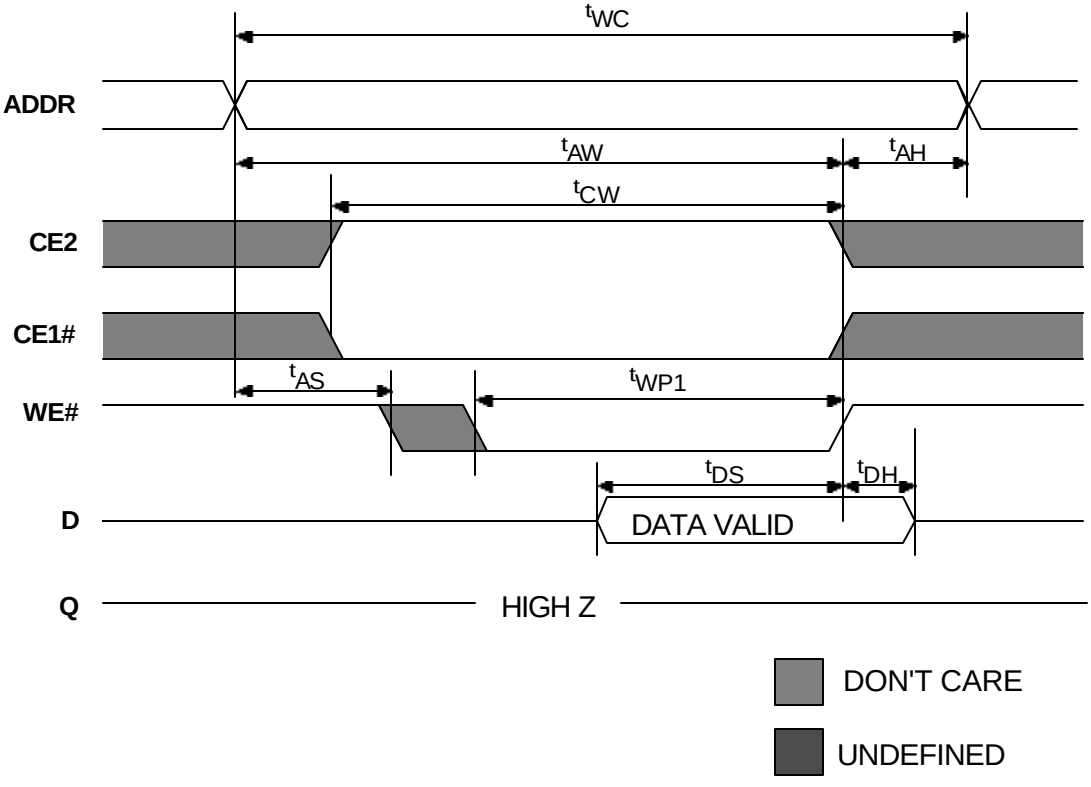
WRITE CYCLE NO. 1[7, 12]

(Write Enable Controlled with Output Enable OE# active LOW))

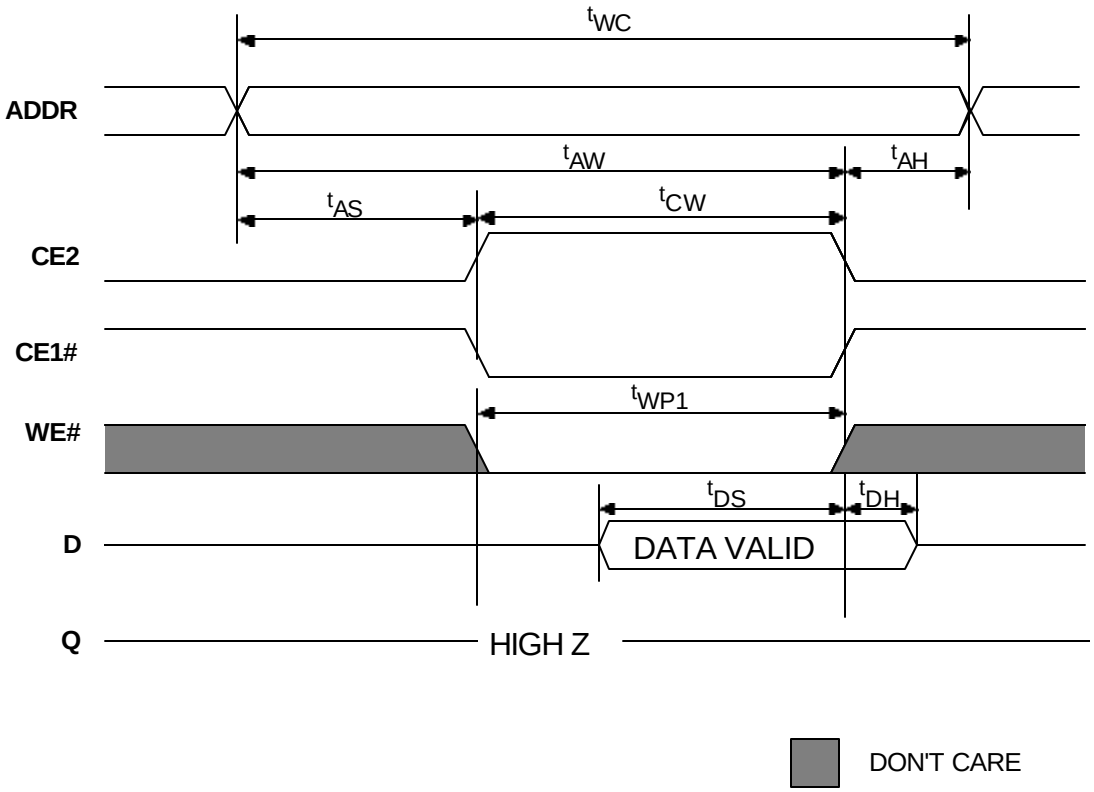


WRITE CYCLE NO. 2[12]

(Write Enable Controlled with Output Enable OE# inactive HIGH)

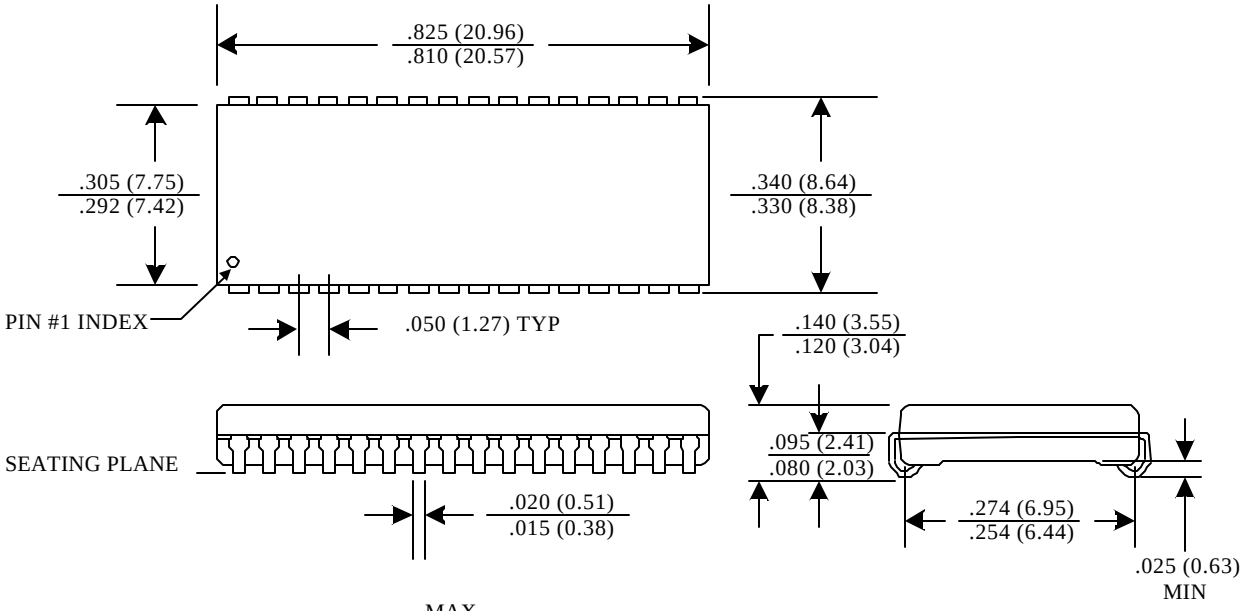


WRITE CYCLE NO. 3(12)
(Chip Enable Controlled)



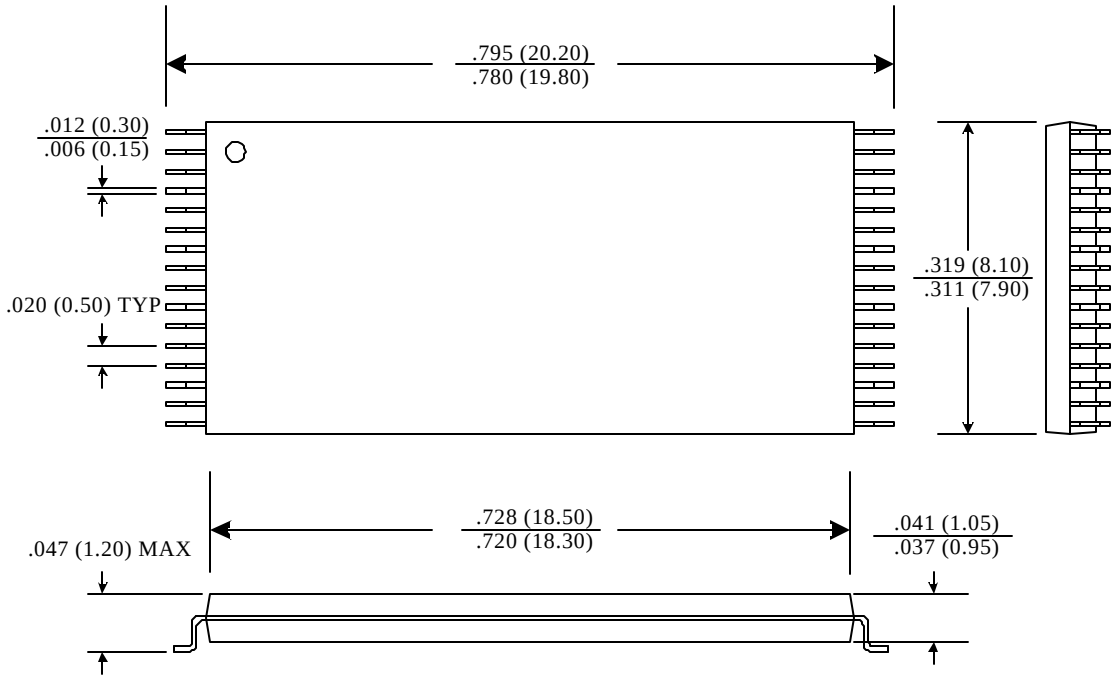
Package Dimensions

32-pin 300 Mil Plastic SOJ (SJ)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, min where noted.

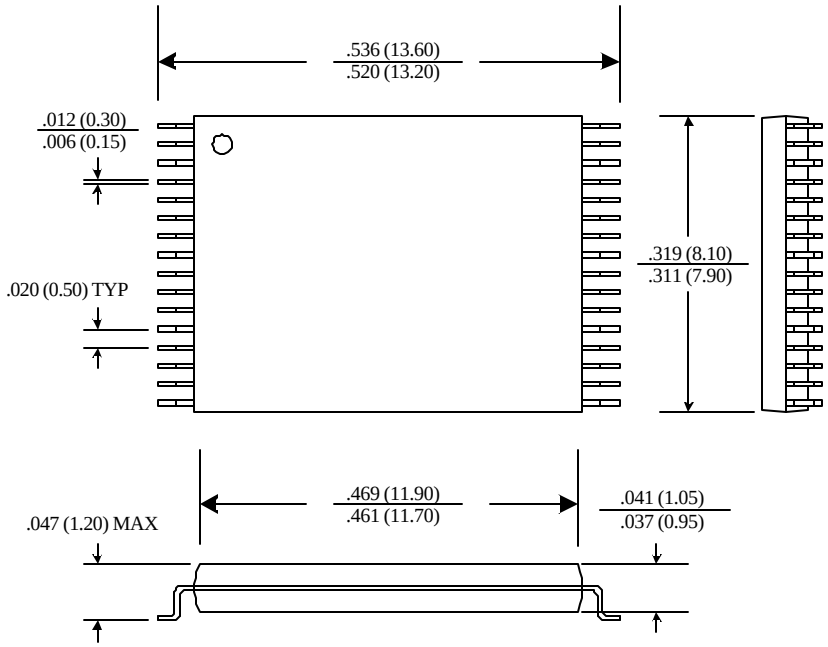
32-pin Plastic TSOP (TS)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, max where noted.

Package Dimensions (continued)

32-pin Plastic STSOP (ST)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, max where noted.

Ordering Information

GVT 73024UL8 XX X - XXX X

Galvantech Prefix

Part Number

Temperature (Blank = Commercial
I = Industrial)

Speed (55 = 55ns, 70= 70ns,
85 = 85ns, 100 = 100ns,
300 = 300ns)

Voltage (Blank = 3.0V to 3.6V,
B = 2.7V to 3.3V,
C = 2.3V to 2.7V,
D = 1.8V to 2.2V)

Package (SJ = 300 mil SOJ,
TS= TSOP TYPE I,
ST= sTSOP TYPE I)