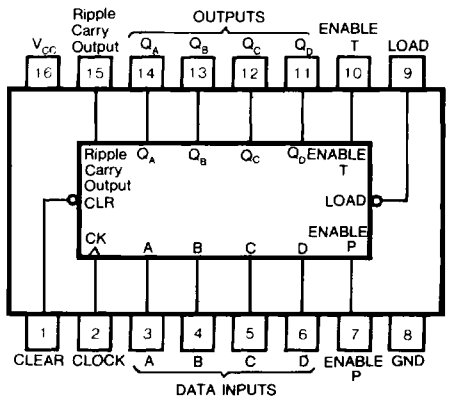
GD54/74LS161A

SYNCHRONOUS 4 BIT COUNTERS; BINARY, DIRECT CLERAR

Feature

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change conicident with each other when so instructed by the count-enable inputs and internal gating.

This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input wave form.

This counter is fully programmable; that is the outputs may be preset to either level. As presetting is synchronous setting up a low level at the load input disables the counter and causes the outputs to agree with the setup dsta after the next clock pulse regardless of the levels of the enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two counter-enable inputs and a riple carry output. Both countenable inputs (ENABLE P and ENABLE T) must be high to count, and ENABLE T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high level portion of the Q_A output. The high-level overflow riple carry pulse can be enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

Function Table (Note 1)

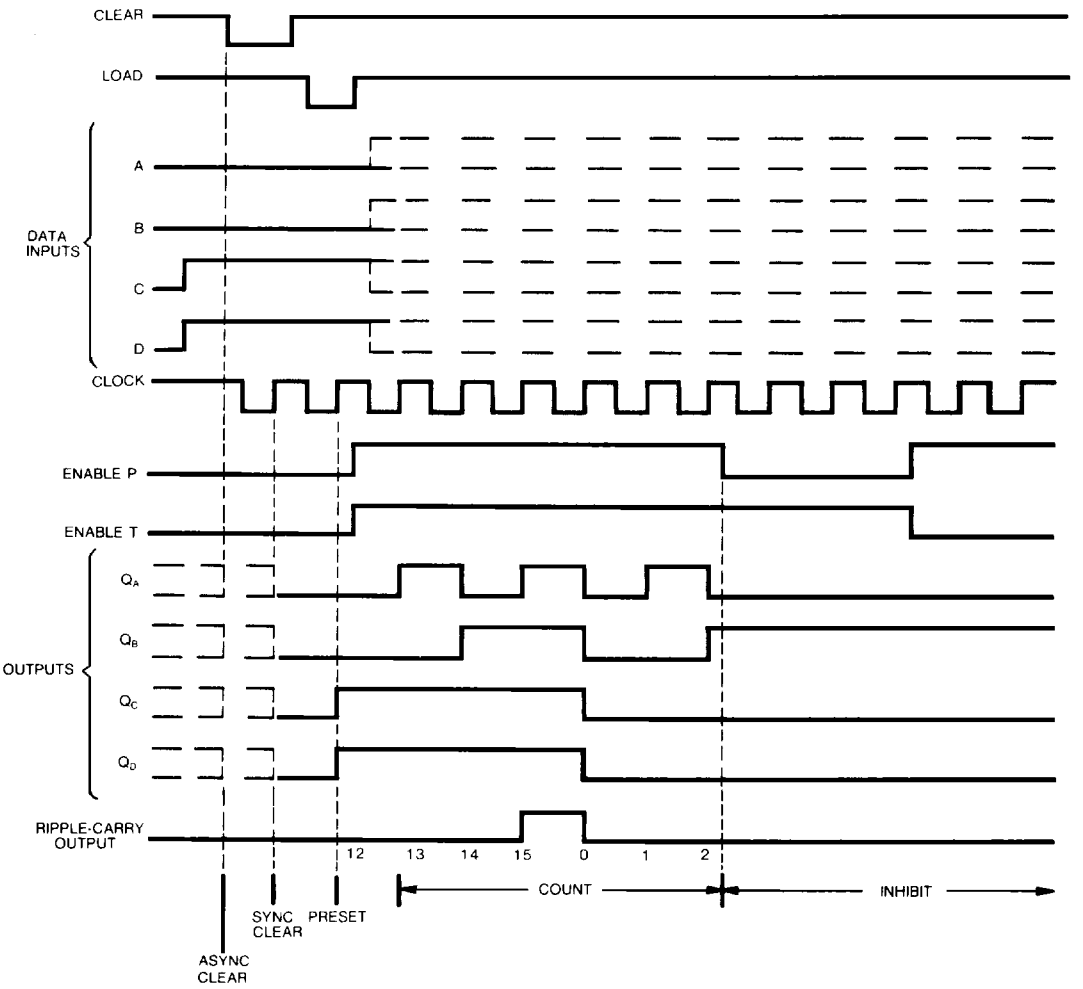
$\overline{CLR}$	$\overline{LOAD}$	E_T	E_P	CK	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1: ↑ : Indicates a transition from low to high (positive edge triggering).
* : RCO is normally low but is high when all Q outputs and E_T are high simultaneously, i.e.,
$RCO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot E_T$
X : irrelevant

Typical Clear, Preset, Count, and Inhibit Sequences

Illustrated below is the following sequence:

1. Clear outputs to zero (asynchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		25	MHz
$tw_{(clock)}$	Width of clock pulse			25			ns
$tw_{(clear)}$	Width of clear pulse			20			ns
t_{SU}	Setup time	Data inputs A,B,C,D.		20			ns
		Enable P or T		20			
		Load		20			
t_h	Hold time at any input			3			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Data or enable P				0.1	mA
			Load, clock or enable T				0.2	
			Clear				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Data or enable P				20	μA
			Load, clock or enable T				40	
			Clear				20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	Data or enable P				−0.4	mA
			Load, clock or enable T Clear				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=Max (Note 3)				18	31	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=Max (Note 4)				18	32	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.
Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

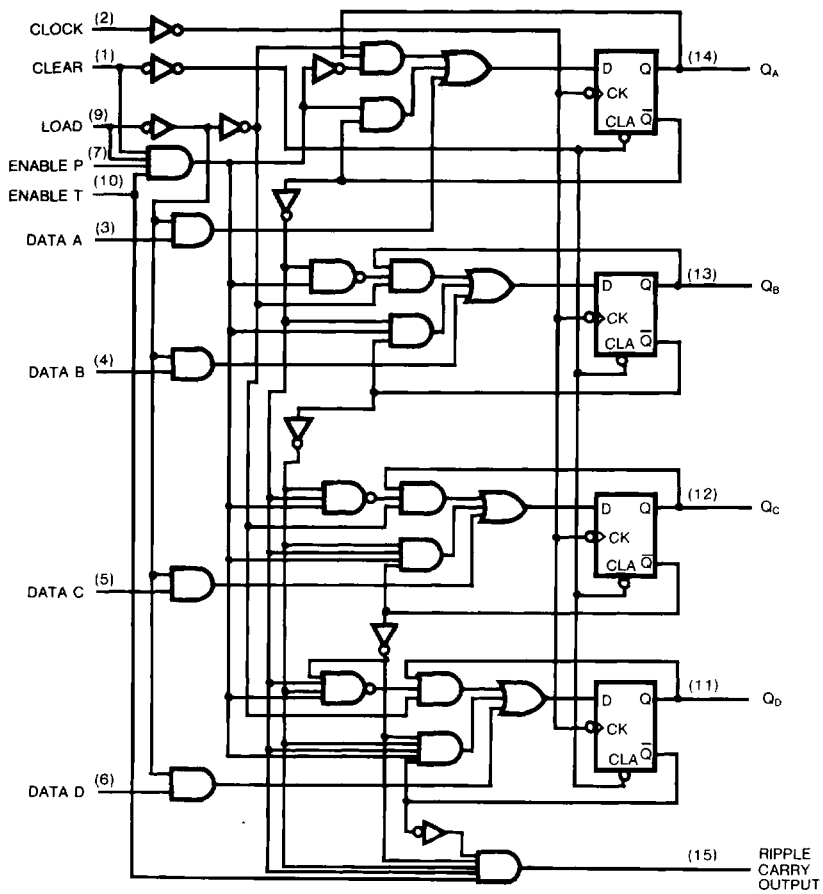
Switching Characteristics, $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L = 15pF$ $R_L = 2k\Omega$ See Note 1	25	32		MHz
t_{PLH}	Clock	Ripple carry			20	35	ns
t_{PHL}					18	35	
t_{PLH}	Clock (load input high)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Clock (load input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Enable T	Ripple carry			9	14	ns
t_{PHL}					9	14	
t_{PHL}	Clear	Any Q			20	28	ns

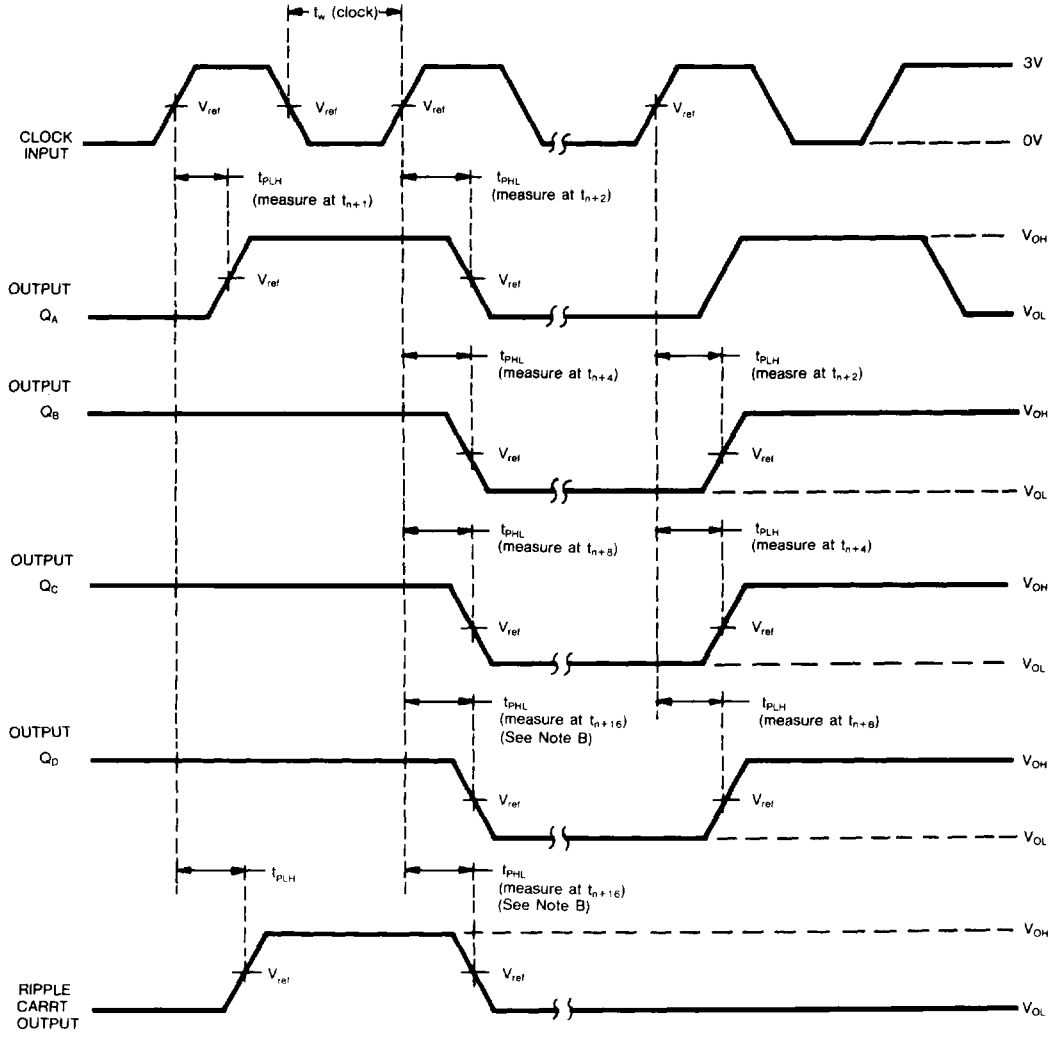
* f_{max} = maximum clock frequency
* t_{PLH} = propagation delay time, low-to-high-level output.
* t_{PHL} = propagation delay time, high-to-low-level output.

Note 1: propagation delay for clearing is measured from the clear input for the LS161A

Function Block Diagram

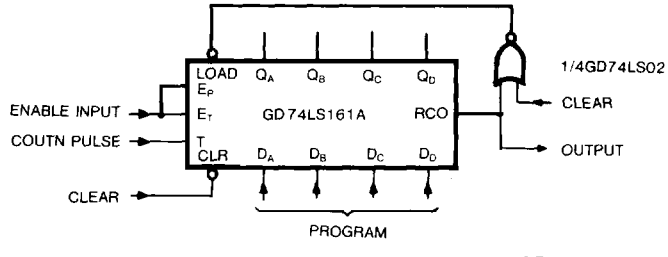


Parameter Measurement Information



Application Example

PROGRAMMABLE DIVIDER



D_A	D_B	D_C	D_D	Divide rate
L	L	L	L	1/16
H	L	L	L	1/15
L	H	L	L	1/14
H	H	L	L	1/13
L	L	H	L	1/12
H	L	H	L	1/11
L	H	H	L	1/10
H	H	H	L	1/9
L	L	L	H	1/8
H	L	L	H	1/7
L	H	L	H	1/6
H	H	L	H	1/5
L	L	H	H	1/4
H	L	H	H	1/3
L	H	H	H	1/2

Note: Reset is performed by applying count pulse with reset input high $\overline{RD}$ pin can't be used since Q_A-Q_D should be set low.