

# SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8 V$  at  $V_{CC}$ ,  $T_A = 25^\circ C$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2 V$  at  $V_{CC}$ ,  $T_A = 25^\circ C$**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

## description

The 'LV161A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V  $V_{CC}$  operation.

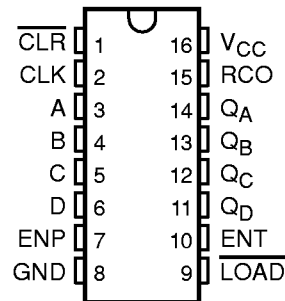
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

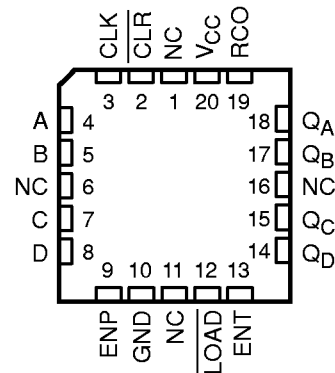
The clear function for the 'LV161A devices is asynchronous. A low level at the clear ( $\overline{CLR}$ ) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load (LOAD), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with  $Q_A$  high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

SN54LV161A . . . J OR W PACKAGE  
SN74LV161A . . . D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LV161A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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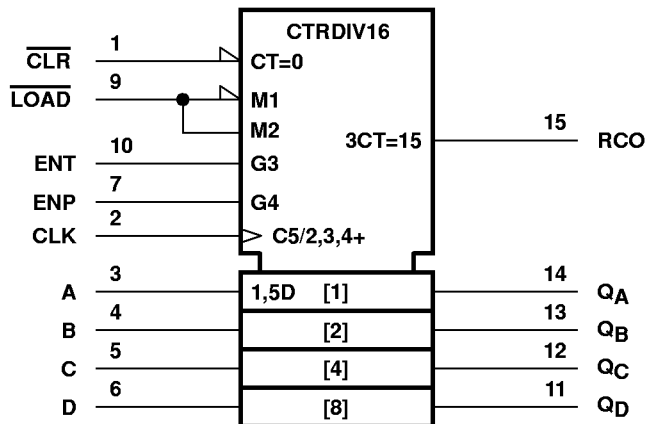
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## description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{LOAD}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54LV161A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LV161A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

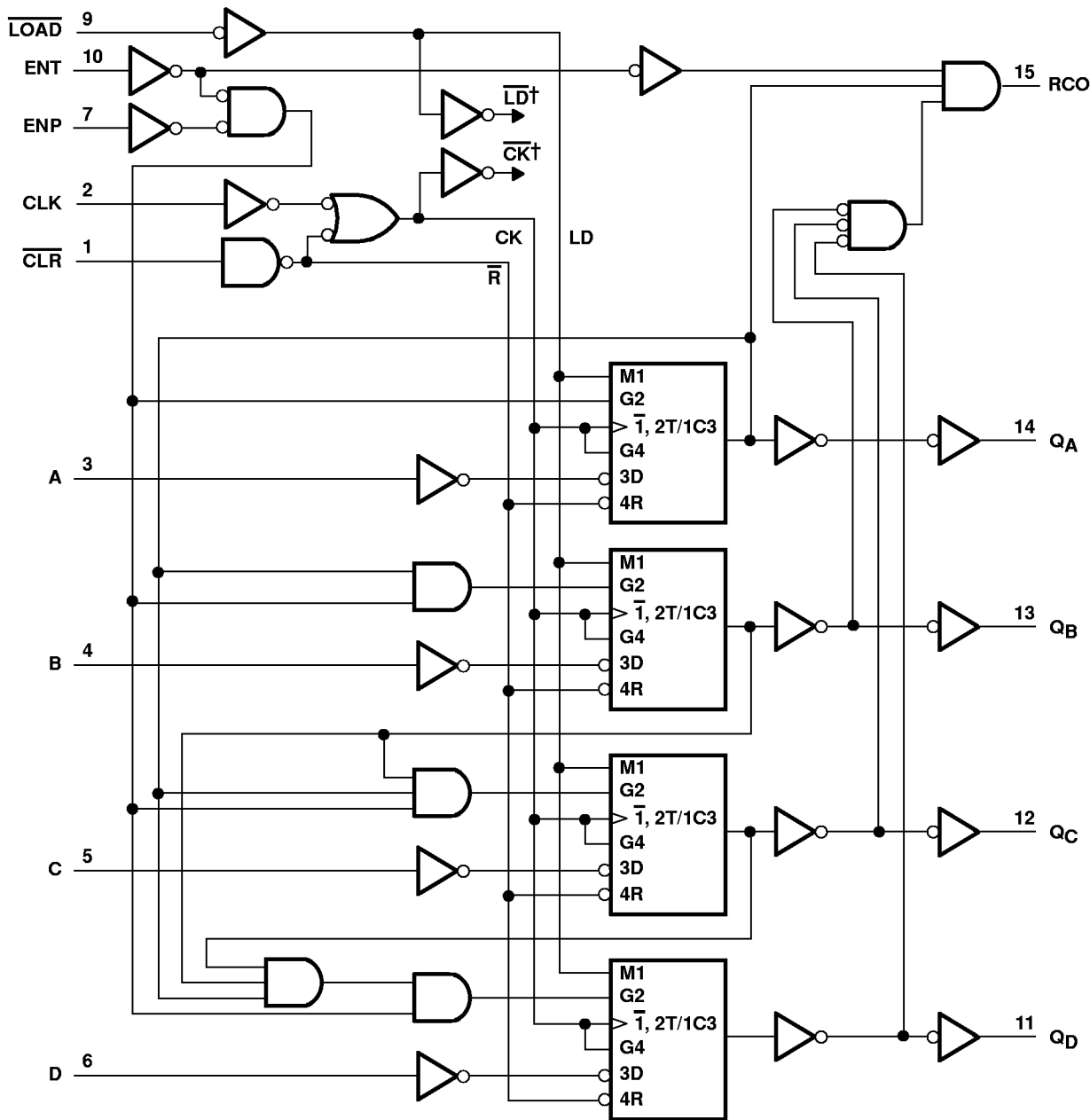
## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

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logic diagram (positive logic)



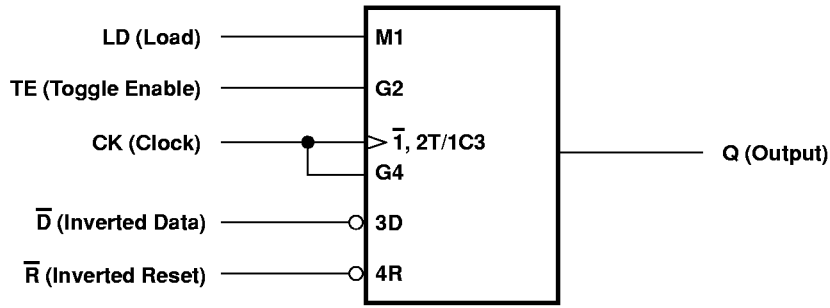
† For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.  
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

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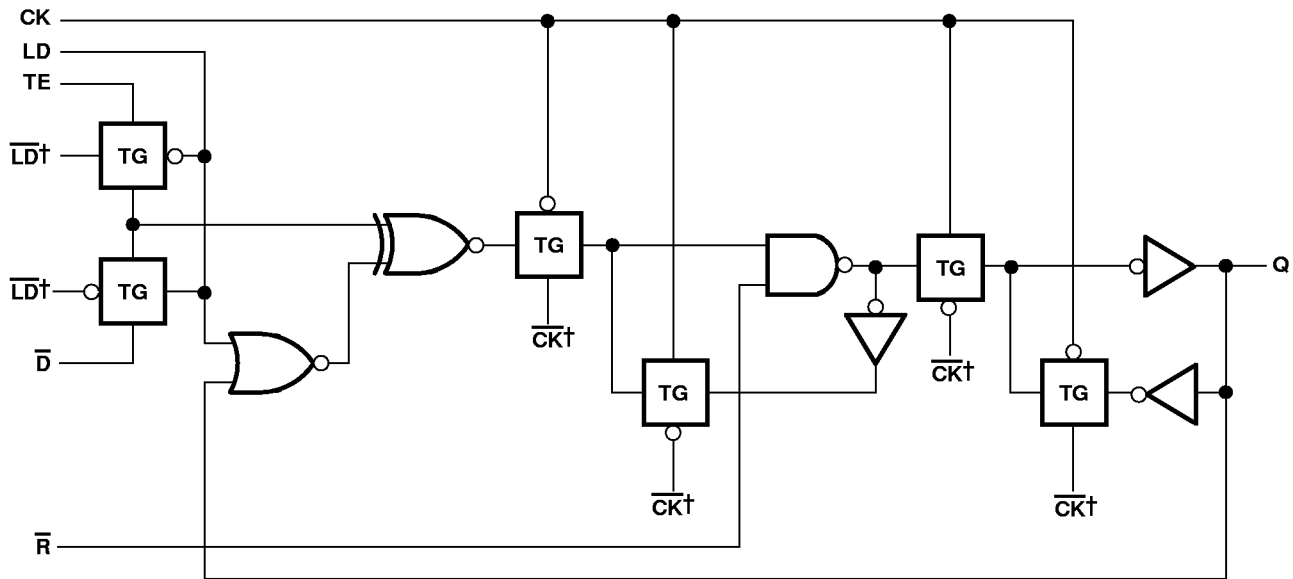
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## logic symbol, each D/T flip-flop



## logic diagram, each D/T flip-flop (positive logic)



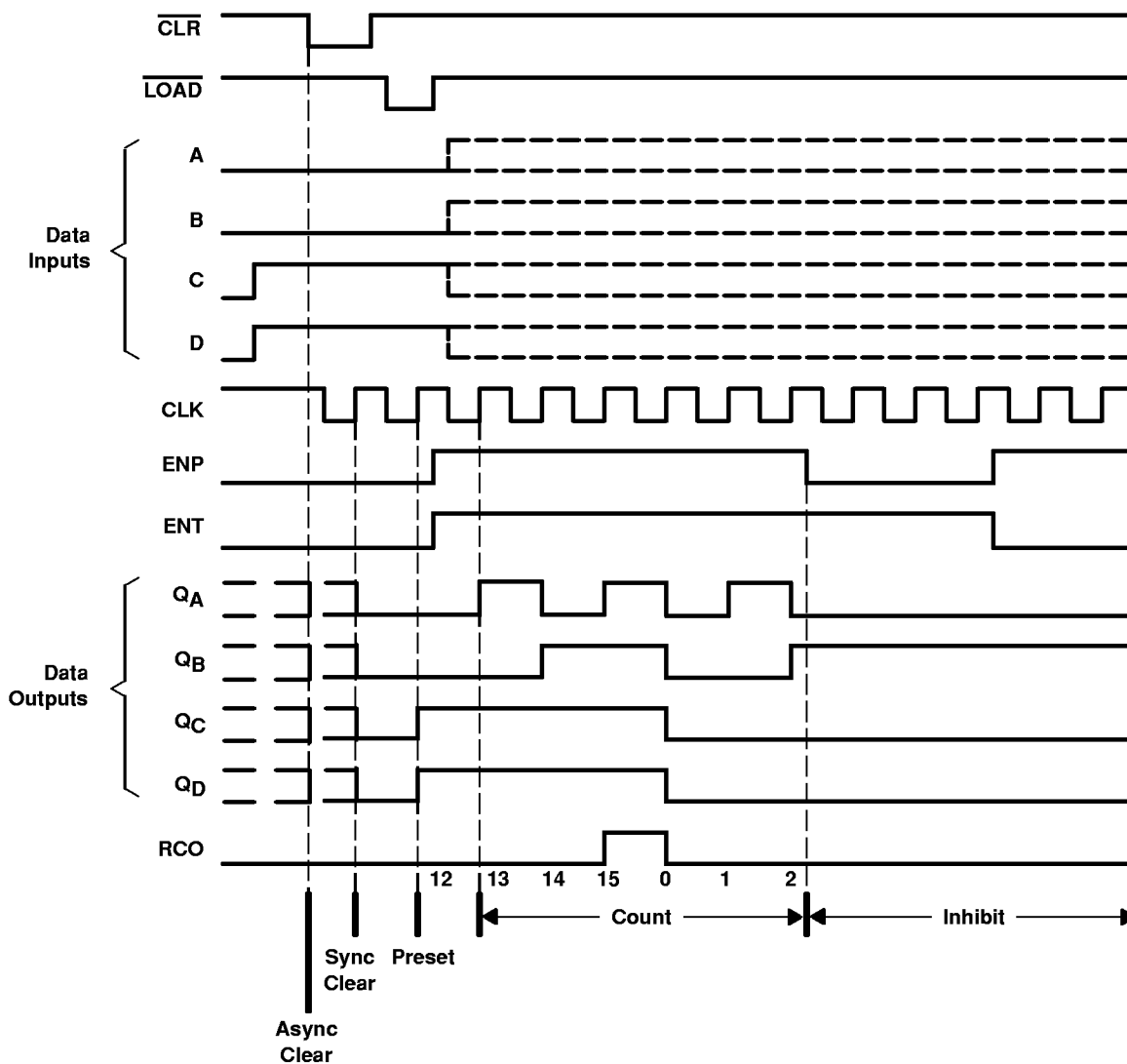
† The origins of  $\overline{LD}$  and  $\overline{CK}$  are shown in the logic diagram of the overall device.

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typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 7 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

		SN54LV161A		SN74LV161A		UNIT	
		MIN	MAX	MIN	MAX		
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V	
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	0.5		V	
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
$V_I$	Input voltage	0	5.5	0	5.5	V	
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	–50		$\mu$ A	
		$V_{CC} = 2.3$ V to 2.7 V	–2	–2			
		$V_{CC} = 3$ V to 3.6 V	–6	–6		mA	
		$V_{CC} = 4.5$ V to 5.5 V	–12	–12			
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	50		$\mu$ A	
		$V_{CC} = 2.3$ V to 2.7 V	2	2			
		$V_{CC} = 3$ V to 3.6 V	6	6		mA	
		$V_{CC} = 4.5$ V to 5.5 V	12	12			
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	200	0	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	0	100	0	100	
		$V_{CC} = 4.5$ V to 5.5 V	0	20	0	20	
$T_A$	Operating free-air temperature	–55	125	–40	85	°C	

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV161A			SN74LV161A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.44			0.44			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±1			±1			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V							pF
		5 V							

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = 25°C		SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low							ns
		CLR low							
t <sub>su</sub>	Setup time before CLK↑	CLR							ns
		Data (A, B, C, and D)							
		ENP, ENT							
		LOAD low							
t <sub>h</sub>	Hold time, all synchronous inputs after CLK↑							ns	

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = 25°C		SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low							ns
		CLR low							
t <sub>su</sub>	Setup time before CLK↑	CLR							ns
		Data (A, B, C, and D)							
		ENP, ENT							
		LOAD low							
t <sub>h</sub>	Hold time, all synchronous inputs after CLK↑							ns	

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low						ns
		$\overline{CLR}$ low						
$t_{su}$	Setup time before CLK $\uparrow$	$\overline{CLR}$						ns
		Data (A, B, C, and D)						
		ENP, ENT						
		$\overline{LOAD}$ low						
$t_h$	Hold time, all synchronous inputs after CLK $\uparrow$							ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5 V \pm 0.2 V$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15 \text{ pF}^*$								MHz
			$C_L = 50 \text{ pF}$								
$t_{PLH}^*$	CLK	Q	$C_L = 15 \text{ pF}$								ns
$t_{PHL}^*$											
$t_{PLH}^*$	CLK	RCO (count mode)									
$t_{PHL}^*$											
$t_{PLH}^*$	CLK	RCO (preset mode)									
$t_{PHL}^*$											
$t_{PLH}^*$	ENT	RCO									
$t_{PHL}^*$											
$t_{PHL}^*$	$\overline{CLR}$	Q									
		RCO									
$t_{PLH}$	CLK	Q	$C_L = 50 \text{ pF}$								ns
$t_{PHL}$											
$t_{PLH}$	CLK	RCO (count mode)									
$t_{PHL}$											
$t_{PLH}$	CLK	RCO (preset mode)									
$t_{PHL}$											
$t_{PLH}$	ENT	RCO									
$t_{PHL}$											
$t_{PHL}$	$\overline{CLR}$	Q									
		RCO									

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
$t_{PLH}^*$	CLK	Q	$C_L = 15\text{ pF}$							ns	
$t_{PHL}^*$											
$t_{PLH}^*$	CLK	RCO (count mode)									
$t_{PHL}^*$											
$t_{PLH}^*$	CLK	RCO (preset mode)									
$t_{PHL}^*$											
$t_{PLH}^*$	ENT	RCO									
$t_{PHL}^*$											
$t_{PHL}^*$	$\overline{\text{CLR}}$	Q									
		RCO									
$t_{PLH}$	CLK	Q	$C_L = 50\text{ pF}$						ns		
$t_{PHL}$											
$t_{PLH}$	CLK	RCO (count mode)									
$t_{PHL}$											
$t_{PLH}$	CLK	RCO (preset mode)									
$t_{PHL}$											
$t_{PLH}$	ENT	RCO									
$t_{PHL}$											
$t_{PHL}$	$\overline{\text{CLR}}$	Q									
		RCO									

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
$t_{\text{PLH}}^*$	CLK	Q	$C_L = 15\text{ pF}$							ns	
$t_{\text{PHL}}^*$											
$t_{\text{PLH}}^*$	CLK	RCO (count mode)									
$t_{\text{PHL}}^*$											
$t_{\text{PLH}}^*$	CLK	RCO (preset mode)									
$t_{\text{PHL}}^*$											
$t_{\text{PLH}}^*$	ENT	RCO									
$t_{\text{PHL}}^*$											
$t_{\text{PHL}}^*$	$\overline{\text{CLR}}$	Q									
		RCO									
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$						ns		
$t_{\text{PHL}}$											
$t_{\text{PLH}}$	CLK	RCO (count mode)									
$t_{\text{PHL}}$											
$t_{\text{PLH}}$	CLK	RCO (preset mode)									
$t_{\text{PHL}}$											
$t_{\text{PLH}}$	ENT	RCO									
$t_{\text{PHL}}$											
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q									
		RCO									

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	SN74LV161A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$				V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$				V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

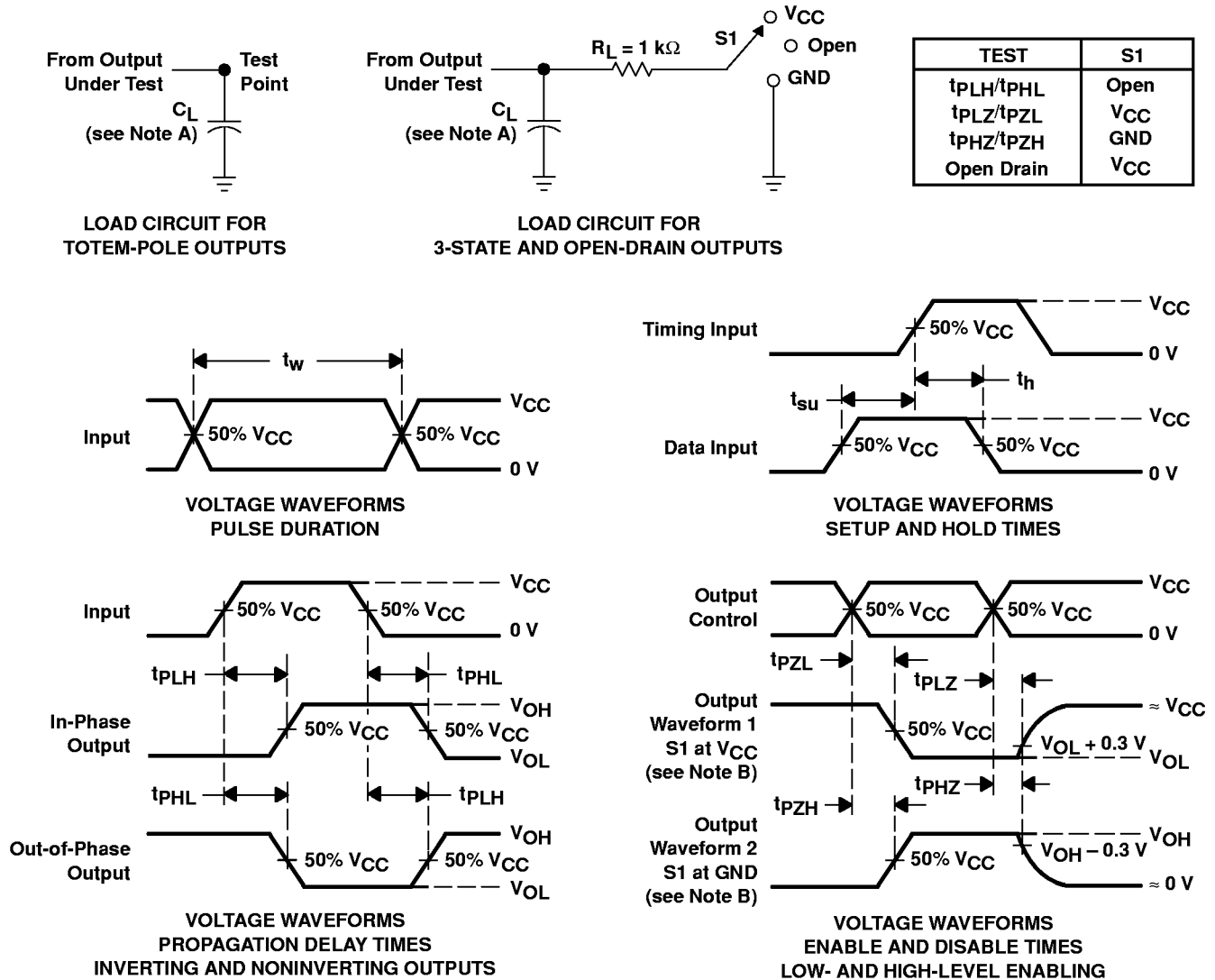
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V		pF
		5 V		

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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