Fast CMOS 16-Bit Registered Transceivers

Product Features:

Common Features:

- PI74FCT16646T and PI74FCT162646T have high current drive and four speed grades.
  Standard speeds at 9.0 ns max.
  "A" speeds at 6.3 ns max.
  "C" speeds at 5.4 ns max.
  "D" speeds at 4.4 ns max.
  "E" speeds at 3.8 ns max.
- Vcc = 5 V ±10%
- Hysteresis on all inputs
- Packaged in 56-pin plastic TSSOP and SSOP

PI74FCT16646T Features:

- High output drive: I_{OH} = –32 mA; I_{OL} = 64 mA
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0 V at Vcc = 5 V, T_A = 25°C

PI74FCT162646T Features:

- Balanced output drivers: ±24 mA
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6 V at Vcc = 5 V, T_A = 25°C

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

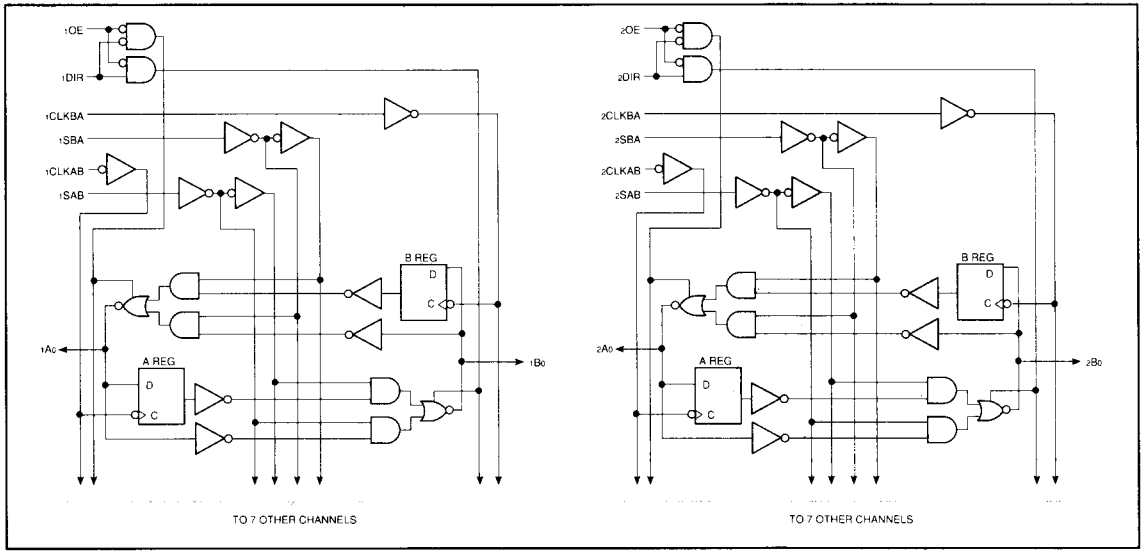
The PI74FCT16646T and PI74FCT162646T are 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable control (x$\overline{OE}$) and direction pins (xDIR) to control the transceiver functions. The Select (xSAB and xSBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74FCT16646T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162646T has ±24 mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

All products are available in 48-pin 240 mil wide plastic TSSOP and 300 mil wide plastic SSOP packages.

Logic Block Diagram

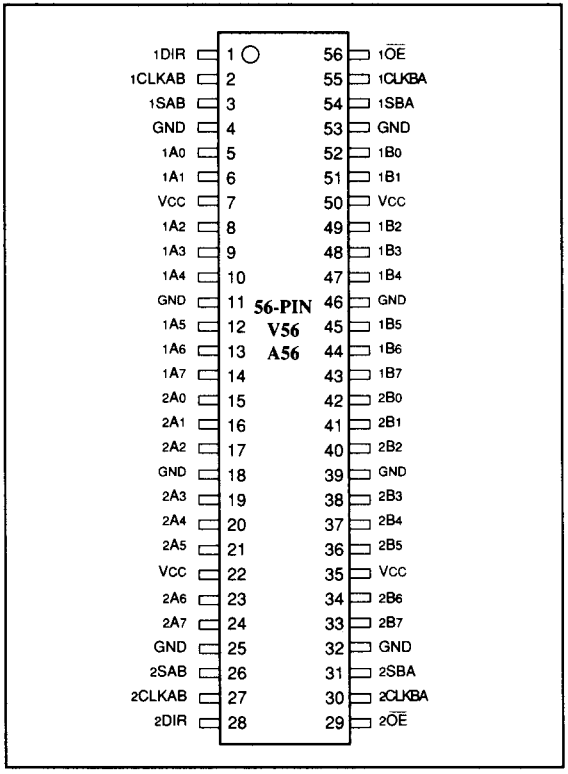


Truth Table

	Inputs						DATA I/O[2]	
Function/Operation	**xOE**	**xDIR**	**xCLKAB**	**xCLKBA**	**xSAB**	**xSBA**	**xAx**	**xBx**
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

1. The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition

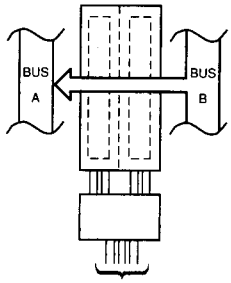
Product Pin Configuration



Product Pin Description

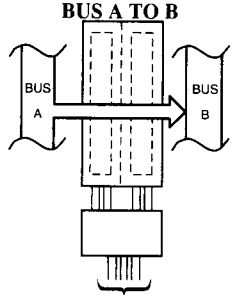
Pin Name	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
xDIR, xOE	Output Enable Inputs
GND	Ground
VCC	Power

REAL-TIME TRANSFER BUS B TO A



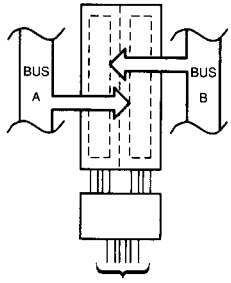
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO B



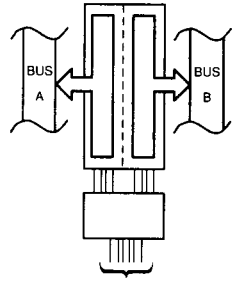
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

STORAGE FROM A AND/OR B



xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

TRANSFER STORES DATA TO A AND/OR B



xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			±5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			±5	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7 V			±10	µA
I_{OZL}	Output Current	V_{CC} = Max.	V_{OUT} = 0.5 V			±10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5 V		–50		–180	mA
V_H	Input Hysteresis				100		mV

PI74FCT16646T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.0 mA	2.5	3.5		V
			I_{OH} = –15.0 mA	2.4	3.5		
			I_{OH} = –32.0 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.2	0.55	V
I_{OFF}	Power Down Disable	V_{CC} = 0 V, V_{IN} or V_{OUT} ≤ 4.5 V		—	—	±100	µA

PI74FCT162646T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24.0 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5 V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5 V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5 V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5 V[3]		–60	–115	–150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	5.5	8	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		2	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4 V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open xDIR = x$\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xDIR = x$\overline{OE}$ = GND	V_{IN} = V_{CC} V_{IN} = GND		0.8	2.7[5]	mA
		One Bit Toggling f_i = 5 MHz 50% Duty Cycle	V_{IN} = 3.4 V V_{IN} = GND		1.3	4.2[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xDIR = x$\overline{OE}$ = GND	V_{IN} = V_{CC} V_{IN} = GND		3.8	7.5[5]	
		16 Bits Toggling f_i = 2.5 MHz 50% Duty Cycle	V_{IN} = 3.4 V V_{IN} = GND		8.3	21.0[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4 V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16646 Switching Characteristics over Operating Range

Preliminary

Parameters	Description	Conditions[1]	'16646T Com. Min	'16646T Com. Max	'16646AT Com. Min	'16646AT Com. Max	'16646CT Com. Min	'16646CT Com. Max	'16646DT Com. Min	'16646DT Com. Max	'16646ET Com. Min	'16646ET Com. Max	Unit
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tPZH tPZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tPHZ tPLZ	Output Disable Time xDIR or xOE to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tSU	Set-up Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	1.5	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	5.0	—	5.0	—	3.0	—	3.0[4]	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162646 Switching Characteristics over Operating Range

Preliminary

Parameters	Description	Conditions[1]	'162646T Com. Min	'162646T Com. Max	'162646AT Com. Min	'162646AT Com. Max	'162646CT Com. Min	'162646CT Com. Max	'162646DT Com. Min	'162646DT Com. Max	'162646ET Com. Min	'162646ET Com. Max	Unit
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tPZH tPZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tPHZ tPLZ	Output Disable Time xDIR or xOE to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tSU	Set-up Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	1.5	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	5.0	—	5.0	—	3.0	—	3.0[4]	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This limit is gauranteed but not tested.