National Semiconductor

PRELIMINARY

August 1998

VME01
16-Bit TTL Compatible Data Transceiver with Incident Wave Switching

General Description

The VME01 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs designed with incident wave switching, live insertion support and enhanced noise margin for TTL backplane applications.

A V_{CC} bias pin provides for the precharging of the A side outputs during live insertion. When set at 5.0V, this pin will establish a voltage of 1.5V on the A port before V_{CC} is connected. This precharge will minimize the capacitive discharge, and associated discontinuity, onto the active backplane during board insertion.

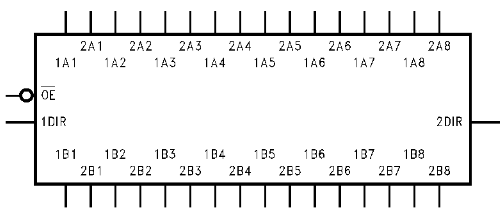
The B port includes a bus hold circuit to latch the output to the value last forced on that pin.

The B port of this device includes 25Ω series output resistors, which minimize undershoot and ringing.

Features

- Supports the VME64 ETL specification
- Functionally and pin compatible with TI SN74ABTE16245
- Improved TTL-compatible input threshold range
- High drive TTL-compatible outputs (I_{OH} = −60 mA, I_{OL} = 90 mA)
- Supports 25Ω incident wave switching on the A port
- V_{CC} Bias pin minimizes signal distortion during live insertion
- BiCMOS design significantly reduces power dissipation.
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise
- 25Ω series-dampening resistor on B-port
- Available in 48-pin SSOP and ceramic flatpak
- Guaranteed output skew
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection

Logic Symbol



DS100228-1

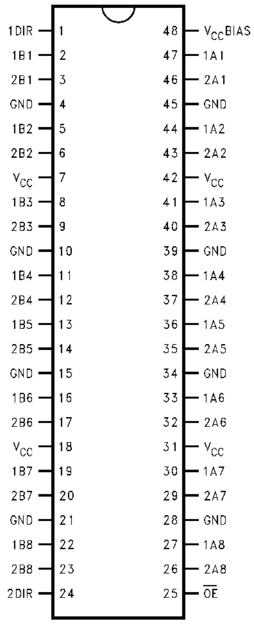
Pin Description

Pin Names	Description
1DIR-2DIR	Transmit/Receive Inputs
$\overline{OE}$	Output Enable Input (Active LOW)
$1A_n$, $2A_n$	Backplane Bus Inputs or TRI-STATE Outputs, with Live Insertion
$1B_n$, $2B_n$	Local Bus Input Pins or TRI-STATE Outputs, with Bus Hold
V_{CC} Bias	Live Insertion Power Supply

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Connection Diagram

Pin Assignment for SSOP and Flatpak



DS100228-2

Functional Description

The device uses byte-wide Direction (DIR) control and a singular Output Enable ($\overline{OE}$) control. The DIR inputs determine the direction of data flow through the device. The $\overline{OE}$ input disables both the A and the B ports, effectively isolating both buses.

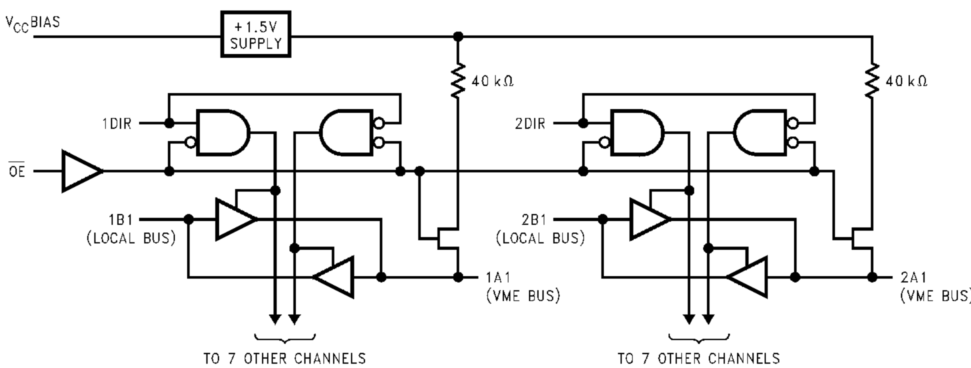
The part contains active circuitry which keeps all outputs disabled when V_{CC} is less than 2.2V to aid in live insertion applications.

Truth Table

(Each 8-bit Section)

Inputs		Operation
$\overline{OE}$	DIR	
L	L	A Data to B Bus
L	H	B Data to A Bus
H	X	Isolation

Logic Diagram (Positive Logic)

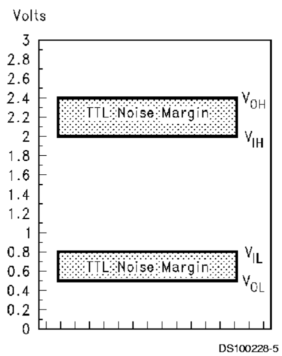


DS100228-3

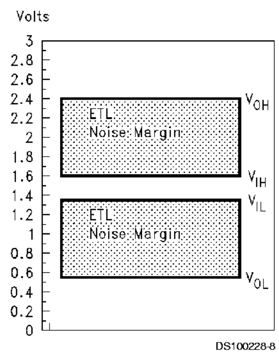
ETL's Improved Noise Immunity

TTL input thresholds are typically determined by temperature-dependent junction voltages which result in worst case input thresholds between 0.8V and 2.0V. By contrast, ETL provides greater noise immunity because its input thresholds are determined by current mode input circuits similar to those used for ECL or BTL. ETL's worst case input thresholds, between 1.4V and 1.6V, are compensated for temperature, voltage and process variations.

Improved Input Threshold Characteristics of ETL



TTL Worst Case V_{OUT}–V_{IN}

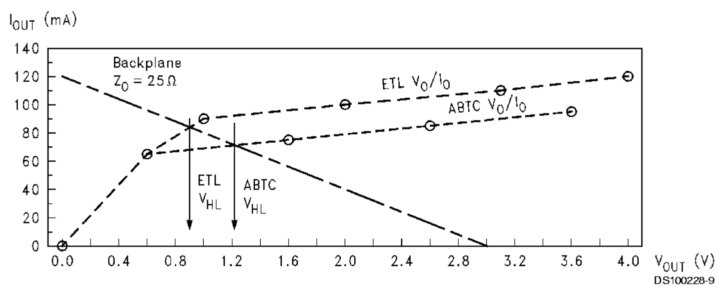


ETL Worst Case V_{OUT}–V_{IN}

Incident Wave Switching

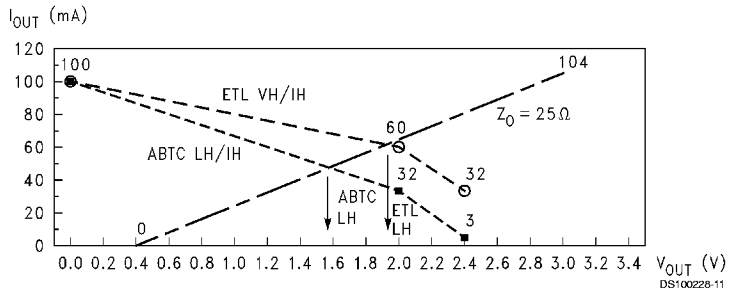
When TTL logic is used to drive fully loaded backplanes, the combination of low backplane bus characteristic impedance, wide TTL input threshold range and limited TTL drive generally require multiple waveform reflections before a valid signal can be received across the backplane. The VME International Trade Association (VITA) defined ETL to provide incident wave switching which increases the data transfer rate of a VME backplane and extends the life of VME applications. TTL compatibility with existing VME backplanes and modules was maintained. To demonstrate the incident wave switching capability, consider a VME application. A VME bus must be terminated to +2.94V with 190Ω at each end of its 21 card backplane. The surge impedance presented by a fully loaded VME backplane is approximately 25Ω. If the output voltage/current of an ABTC driver is plotted with this load, the intersection at 1.2V for a falling edge and at 1.6V for a rising edge does not reach the worst case input threshold of a second ABTC circuit. This is shown in the two figures below. However, an ETL driver located at one end of the backplane is able to provide incident wave switching because it has a higher drive and a tighter input threshold.

Estimated ETL/ABTC Initial Falling Edge Step



Incident Wave Switching (Continued)

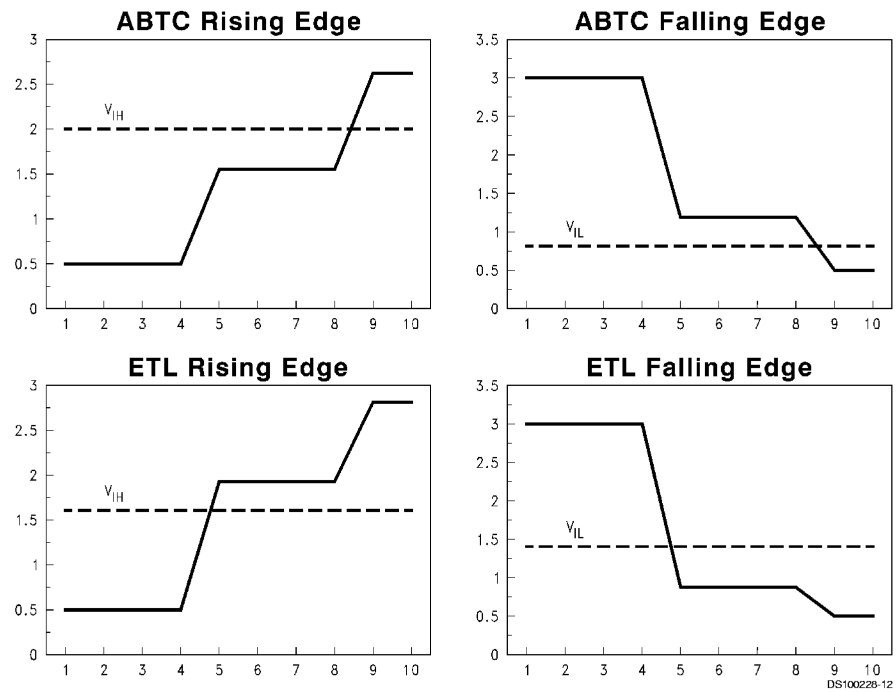
Estimated ETL/ABTC Initial Rising Edge Step



Because ETL has a much more precise input threshold region, an ETL receiver will interpret its predicted falling input of 0.85V as a logic ZERO and the initial rising edge of 1.9V as a logic ONE. This comparison is for the case of a 25Ω surge impedance backplane driven from one end.

The resulting ABTC and ETL waveform predictions and their input thresholds are compared below. This shows how ETL can achieve backplane speeds not always possible with conventional TTL compatible logic families.

Comparing the Incident Wave Switching of ETL with ABTC



Live Insertion Module Replacement

To allow a system module to be replaced without disturbing signals passing between other operating modules requires careful design of operating systems, applications software and hardware. ETL supports live insertion module replacement with features that minimize backplane signal disturbance while a module is inserted. As specified by VITA, live insertion requires several backward-compatible system enhancements including: an improved backplane connector with an embedded ground plane and differential length connector pins. The differential length connector pins allow power sequencing to the module so that the signal pins can be controlled to a biased high impedance before they make contact with the backplane.

VITA's ETL modules will use an early V_{CC} power input, called V_{CC} Bias, to control the ETL transceivers to a high impedance to minimize insertion disturbance. In addition, V_{CC}

Live Insertion Module Replacement (Continued)

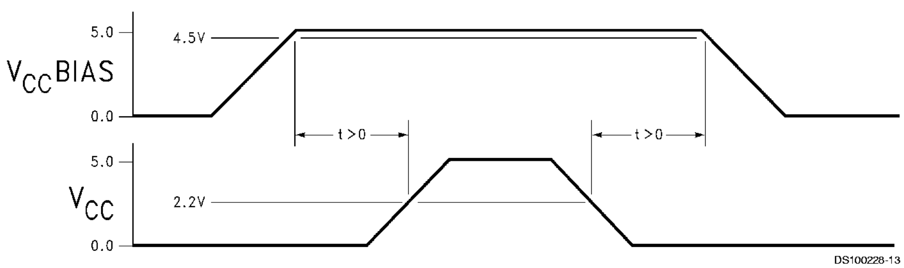
Bias is used to precharge the backplane driver output capacitance including the module connector pin and module etch. The precharge voltage is to 1.5V using a switched 40 kΩ resistor. This precharge will minimize the capacitive discharge onto an active backplane as the signal connection is made. To allow designers to maintain this condition

until after a module is fully powered and initialized, the $\overline{OE}$ pin can be used to maintain outputs in the high impedance, precharged state. Contact bounce during live insertion will charge each output pin to a logic ONE or ZERO. If the contact bounces open, the 40 kΩ resistor will reestablish the 1.5V level in a few microseconds.

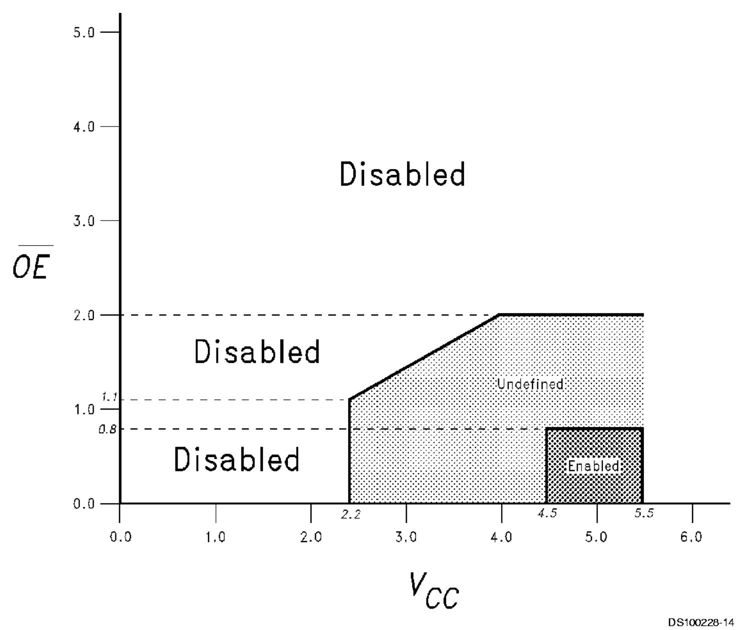
When applying power to a printed circuit board containing ETL transceivers, the system V_{CC} can be connected to V_{CC}. Bias without damage to the device.

If the advantages of Live Insertion are to be included in the system, then V_{CC} Bias should be allowed to reach normal operating levels before V_{CC} becomes higher than 2.2 volts. In addition, when removing a module, or turning off system power, V_{CC} should be reduced below 2.2 volts before V_{CC}. Bias is allowed to drop below normal operating limits. This sequencing is shown below.

The figure V_{CC} Power-up Critical Voltages shows the relationship between V_{CC} and $\overline{OE}$ while power is being applied and removed. This relationship holds if V_{CC} Bias is within normal operating conditions or if V_{CC} Bias is equal to V_{CC}.



Power Sequencing to Achieve Live Insertion Precharging



V_{CC} and $\overline{OE}$ Power-Up Relationship

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
Plastic	−55˚C to +150˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−50 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	128 mA
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Commercial	−40˚C to +85˚C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(Δt/ΔV)
Data Input	20 ns/V
Enable Input	50 ns/V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		VME01 Min	VME01 Typ	VME01 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	$\overline{OE}$	2.0			V		Recognized HIGH Signal
		Other Inputs	1.6					
V_{IL}	Input LOW Voltage	$\overline{OE}$			0.8	V		Recognized LOW Signal
		Other Inputs			1.4			
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}_n$, DIR)
V_{OH}	Output HIGH Voltage	B Port			V_{CC} − 1	V	Min	I_{OH} = −100 µA
			2.4			V		I_{OH} = −1 mA
			2.0			V		I_{OH} = −12 mA
		A Port			V_{CC} − 1	V	Min	I_{OH} = −1 mA
			2.4			V		I_{OH} = −32 mA
			2.0			V		I_{OH} = −60 mA
V_{OL}	Output LOW Voltage	B Port			0.4	V	Min	I_{OL} = 1 mA
					0.8	V		I_{OL} = 12 mA
		A Port			0.55	V	Min	I_{OL} = 64 mA
					0.9	V		I_{OL} = 90 mA
I_{HOLD}	Bus Hold Current	B Port	100			µA	Min	$\overline{OE}$ = HIGH, V_O = 0.8V
			−100					$\overline{OE}$ = HIGH, V_O = 2.0V
I_{CC}	V_{CC} Bias Supply Current				10	mA		V_{CC} = ≤ V_{CC} Bias V_{CC} Bias = 0 to 5.5V I_O = 0
I_{OFF}	Output Current, Power Down				100	µA	0.0	V_{CC} Bias = 0V V_I or V_O ≤ 4.5V
I_I	Input Current Control Pins	Military			±10	µA	5.5	V_{IN} = 0 or V_{CC}
		Commercial			±5	µA	5.5	V_{IN} = 0 or V_{CC}
I_{IH} + I_{OZH}	Output Leakage Current	A Port			50	µA	5.5	V_{OUT} = 2.7V, $\overline{OE}$ = 2.0V

DC Electrical Characteristics (Continued)

Symbol	Parameter		VME01 Min	VME01 Typ	VME01 Max	Units	V_{CC}	Conditions
I_{IL} + I_{OZL}	Output Leakage Current	A Port			–50	µA	5.5	V_{OUT} = 0.5V, $\overline{OE}$ = 2.0V
I_{CCH}	Power Supply Current				40	mA	Max	All Outputs HIGH, $\overline{OE}$ = LOW, DIR = HIGH or LOW
I_{CCL}	Power Supply Current				80	mA	Max	All Outputs LOW, $\overline{OE}$ = LOW, DIR = HIGH or LOW
I_{CCZ}	Power Supply Current				40	mA	Max	$\overline{OE}$ = HIGH All Others at V_{CC} or GND DIR = HIGH or LOW
I_{CCD}	Dynamic I_{CC} No Load (Note 3)				0.15	mA/ MHz	Max	Outputs Open $\overline{OE}_n$ = GND, DIR = HIGH One Bit Toggling, 50% Duty Cycle
V_{LI}	Output Live Insertion Voltage	A Port	1.3		1.7	V	5.0	I_{OUT} = 0 mA, $\overline{OE}$ = HIGH V_{CC} Bias = 5.0V
I_{PRE}	Precharge Current	A-Port	–20		–100	µA	5.0	$\overline{OE}$ = HIGH, V_O = 0V, V_{CC} Bias = 5.0V
			20		100	µA	5.0	V_O = 3V, V_{CC} Bias = 5.0V, $\overline{OE}$ = High
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}				1.0	V	5.0	T_A = 25˚C (Note 4) C_L = 50 pF; R_L = 500Ω
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		–1.4			V	5.0	T_A = 25˚C (Note 4) C_L = 50 pF; R_L = 500Ω
V_{OHV}	Minimum High Level Dynamic Output Voltage (Note 3)			2.7		V	5.0	T_A = 25˚C (Note 6) C_L = 50 pF; R_L = 500Ω
V_{IHD}	Minimum High Level Dynamic Input Voltage (Note 3)		2.0	1.5		V	5.0	T_A = 25˚C (Note 5) C_L = 50 pF; R_L = 500Ω
V_{ILD}	Maximum Low Level Dynamic Input Voltage (Note 3)			1.2	0.8	V	5.0	T_A = 25˚C (Note 5) C_L = 50 pF; R_L = 500Ω

Note 3: Guaranteed, but not tested.

Note 4: Max. number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 5: Max. number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 6: Max. number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	Commercial T_A = +25˚C V_{CC} = +5V			Military T_A = –55˚C to +125˚C V_{CC} = 4.5V–5.5V		Commercial T_A = –40˚C to +85˚C V_{CC} = 4.5V–5.5V		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation	1.5		7.0	1.5	7.0	1.5	7.0	ns	*Figures 1, 2, 3, 4, 6*
t_{PHL}	Delay A-Port to B-Port	1.5		7.0	1.5	7.0	1.5	7.0		
t_{PLH}	Propagation	1.5		7.0	1.5	7.0	1.5	7.0	ns	*Figures 1, 2, 3, 4, 6*
t_{PHL}	Delay B-Port to A-Port	1.5		7.0	1.5	7.0	1.5	7.0		
t_{PZH}	Output Enable	1.0		7.0	1.0	7.0	1.0	7.0	ns	*Figures 1, 2, 3, 4, 5*
t_{PZL}	Time	1.0		7.0	1.0	7.0	1.0	7.0		

AC Electrical Characteristics (Continued)

Symbol	Parameter	Commercial $T_A = +25^{\circ}C$ $V_{CC} = +5V$			Military $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $V_{CC} = 4.5V–5.5V$		Commercial $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $V_{CC} = 4.5V–5.5V$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PHZ}	Output Disable	1.0		7.0	1.0	7.0	1.0	7.0	ns	*Figures 1, 2, 3, 4, 5*
t_{PLZ}	Time	1.0		7.0	1.0	7.0	1.0	7.0		
t_r	Rise Time 1V → 2V, A-Port Outputs	1.2		3.0	0.8	4.0	1.2	3.0	ns	*Figures 1, 2, 3, 4, 6*
t_f	Fall Time 2V → 1V, A-Port Outputs	1.2		3.0	0.8	4.0	1.2	3.0	ns	*Figures 1, 2, 3, 4, 6*

Skew

Symbol	Parameter	Commercial $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching	Military $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching	Units	Conditions
		Max	Max		
t_{OHS} (Notes 7, 8)	Pin-to-Pin Skew LH/HL A-Port to B-Port	1.3	1.3	ns	*Figures 1, 2, 3, 4, 6*
t_{OHS} (Notes 7, 8)	Pin-to-Pin Skew LH/HL B-Port to A-Port	1.3	1.3	ns	*Figures 1, 2, 3, 4, 6*
t_{PS} (Notes 7, 8)	Duty Cycle Skew B-Port to A-Port	2.0	2.0	ns	*Figures 1, 2, 3, 4, 6*
t_{PS} (Notes 7, 8)	Duty Cycle Skew A-Port to B-Port	2.0	2.0	ns	*Figures 1, 2, 3, 4, 6*

VME Extended Skew

Symbol	Parameter	Commercial $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching	Military $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching	Units	Conditions
		Max	Max		
t_{PV} (Notes 7, 8)	Device-to-Device Skew LH/HL Transitions B-Port to A-Port	4.0	4.5	ns	*Figures 1, 2, 3, 4, 6*
t_{PV} (Notes 7, 8)	Device-to-Device Skew LH/HL Transitions A-Port to B-Port	2.5	3.0	ns	*Figures 1, 2, 3, 4, 6*
t_{CP} (Notes 7, 9)	Change in Propagation Delay with Load B-Port to A-Port	4.0	4.5	ns	*Figures 1, 2, 3, 4, 6*
t_{CPV} (Notes 7, 8, 9)	Device-to-Device, Change in Propagation Delay with Load B-Port to A-Port	6.0	7.0	ns	*Figures 1, 2, 3, 4, 6*

Note 7: Skew is defined as the absolute difference in delay between two outputs. The specification applies to any outputs switching HIGH to LOW, LOW to HIGH, or any combination switching HIGH-to-LOW or LOW-to-HIGH. This specification is guaranteed but not tested.

Note 8: This is measured with both devices at the same value of V_{CC} ±1% and with package temperature differences of 20°C from each other.

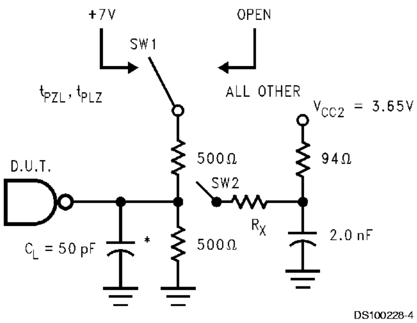
Note 9: This is measured with Rx in *Figure 1* at 13Ω for one unit and at 56Ω for the other unit.

Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions, $T_A = 25^\circ C$
C_{IN}	Input Capacitance	5	8	pF	$V_{CC} = 0.0V$ ($\overline{OE}_n$, DIR)
$C_{I/O}$ (Note 10)	Output Capacitance	9	12	pF	$V_{CC} = 5.0V$ (A_n)

Note 10: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

Note 11: Defined to emulate the range of VME bus transmission line loading as a function of board population and driver location. Rx = 13Ω, 26Ω or 56Ω depending on test.

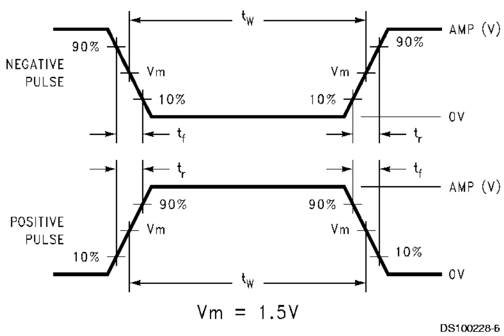


FIGURE 2. Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

Test	Port	SW1	SW2	Rx
t_{PHZ}, t_{PZH}	A, B	Open	Open	
t_{PLZ}, t_{PZL}	A, B	+7	Open	
t_{PLH}, t_{PHL}	A	Open	Closed	26
t_{PLH}, t_{PHL}	B	Open	Open	
t_r, t_f	A	Open	Closed	26
t_{PV}	A	Open	Closed	26
t_{PV}	B	Open	Open	
t_{CP}	A	Open	Closed	13 then 56
t_{CPV}	A	Open	Closed	13 and 56

FIGURE 4.

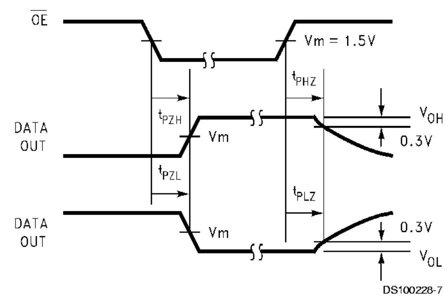


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

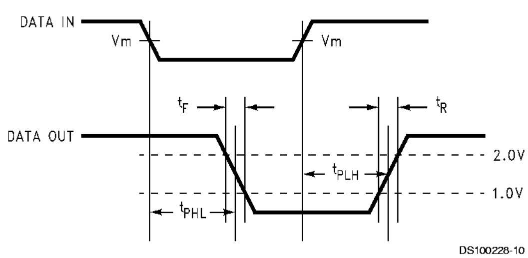
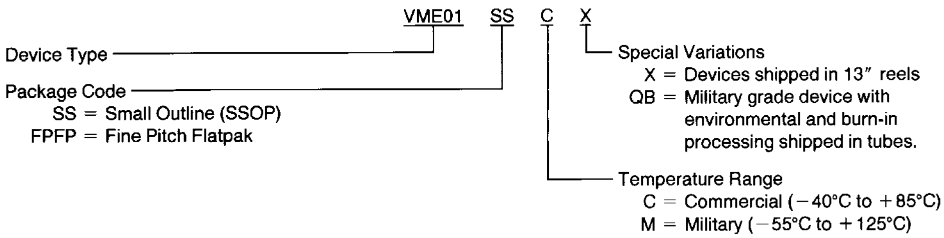


FIGURE 6. Rise, Fall Time and Propagation Delay Waveforms

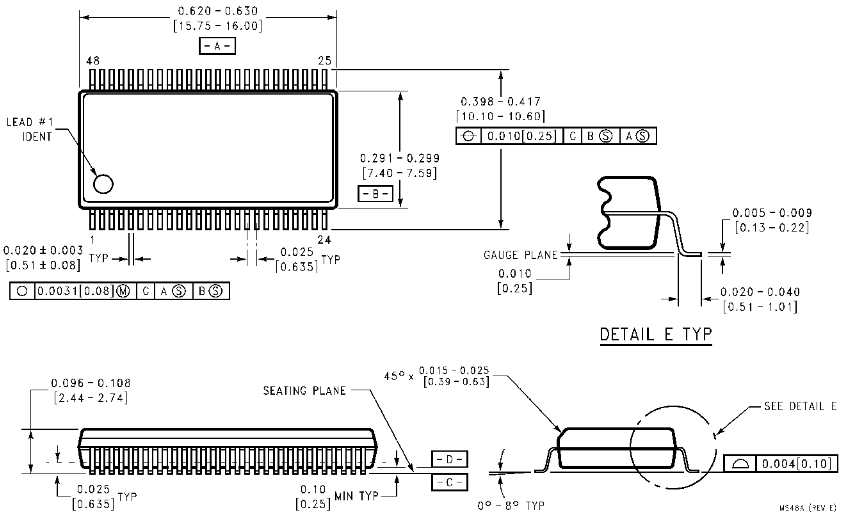
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

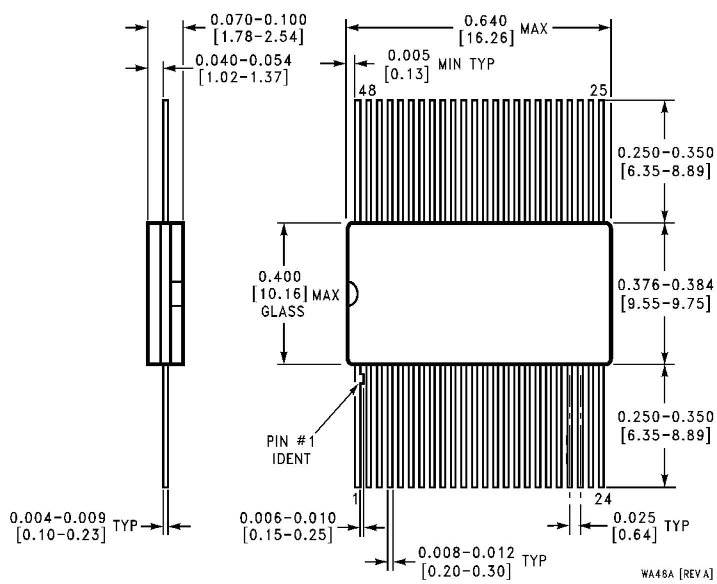


DS100228-15

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead SSOP (0.300" Wide) (SS)
NS Package Number MS48A



48-Pin Ceramic Flatpak (FPFP)
NS Package Number WA48A

LIFE SUPPORT POLICY

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