

TARGET SPECIFICATION

IS62Ux2568 Series 256K x 8 LOW VOLTAGE, LOW POWER CMOS STATIC RAM

FEATURES

- Voltage range options
 - 1.6V to 2.0V: IS62UT2568
 - 1.8V to 2.2V: IS62US2568
 - 2.3V to 2.7V: IS62UR2568
 - 2.7V to 3.3V: IS62UP2568
- Battery backup (SL/LL version)
 - 1.0V (min.) data retention
- Access times: 55, 70, and 100 ns
- Fully static operation and tri-state outputs
- Industrial temperature available
- Available in 36-ball mini BGA and 32-pin sTSSOP(I)

DESCRIPTION

The *ISSI* IS62Ux2568 series is a low voltage, 262,144 words by 8 bits, CMOS SRAM. It is fabricated using *ISSI*'s low voltage, six transistor (6T), CMOS technology. The series is targeted to satisfy the demands of the state-of-the-art technologies such as cell phones and pagers.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Additionally, easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS62Ux2568 series is packaged in a 36-ball mini BGA and a 32-pin TSOP (I).

PRODUCT SERIES OVERVIEW

Part No.	Voltage (V)	Speeds (ns)	Active I _{cc} (mA)	Standby Current (μA)		Temperature (°C)
				LL	SL	
IS62UP2568	3.0, ±0.3	55, 70, 100	25 @ 70 ns	10	2	0 to 70
IS62UP2568 ⁽¹⁾	3.0, ±0.3	55, 70, 100	25 @ 70 ns	10	2	40 to 85
IS62UR2568	2.5, ±0.2	55, 70, 100	15 @ 70 ns	10	2	0 to 70
IS62UR2568 ⁽¹⁾	2.5, ±0.2	55, 70, 100	15 @ 70 ns	10	2	40 to 85
IS62US2568	2.0, ±0.2	55, 70, 100	10 @ 70 ns	10	2	0 to 70
IS62US2568 ⁽¹⁾	2.0, ±0.2	55, 70, 100	10 @ 70 ns	10	2	40 to 85
IS62UT2568	1.8, ±0.2	55, 70, 100	10 @ 70 ns	10	2	0 to 70
IS62UT2568 ⁽¹⁾	1.8, ±0.2	55, 70, 100	10 @ 70 ns	10	2	40 to 85

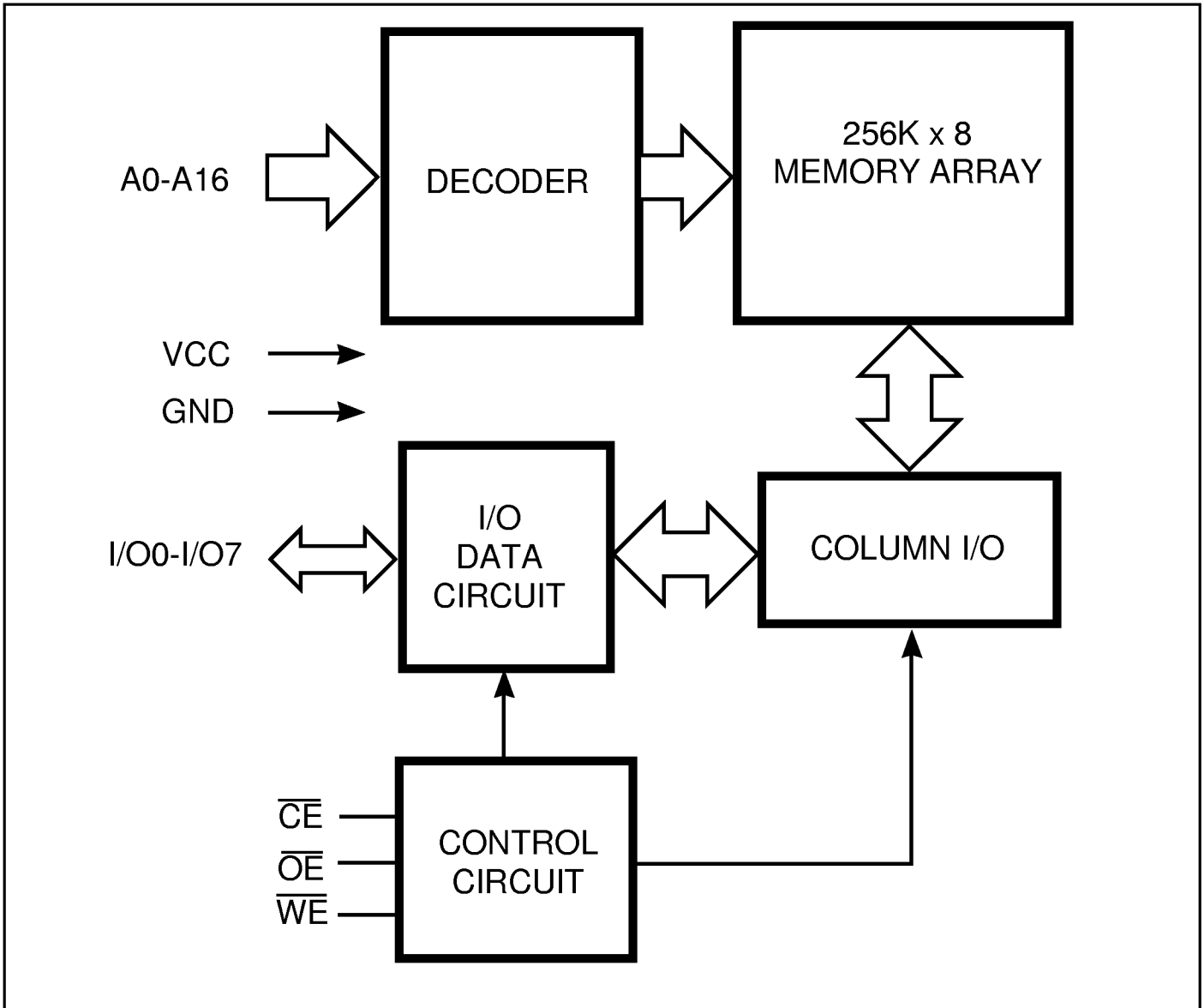
Note:

1. Current value is max.

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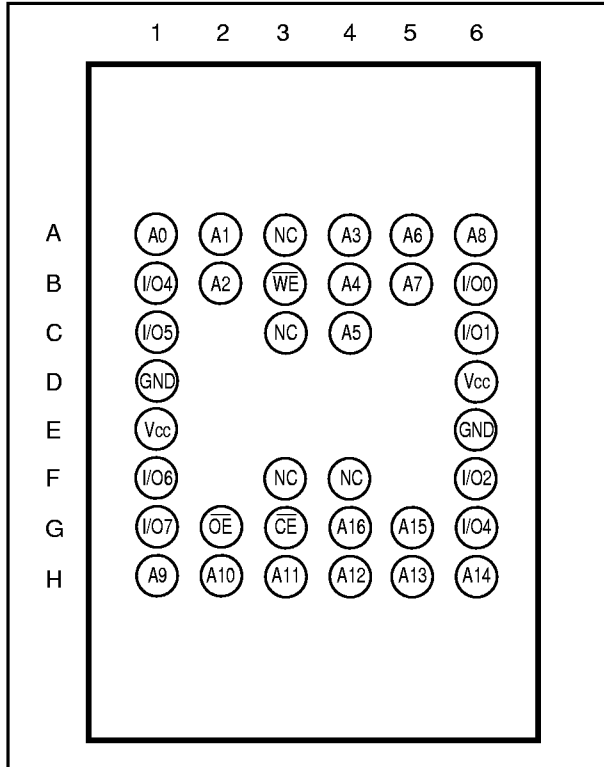
FUNCTIONAL BLOCK DIAGRAM



IS62Ux2568 SERIES

PIN CONFIGURATIONS

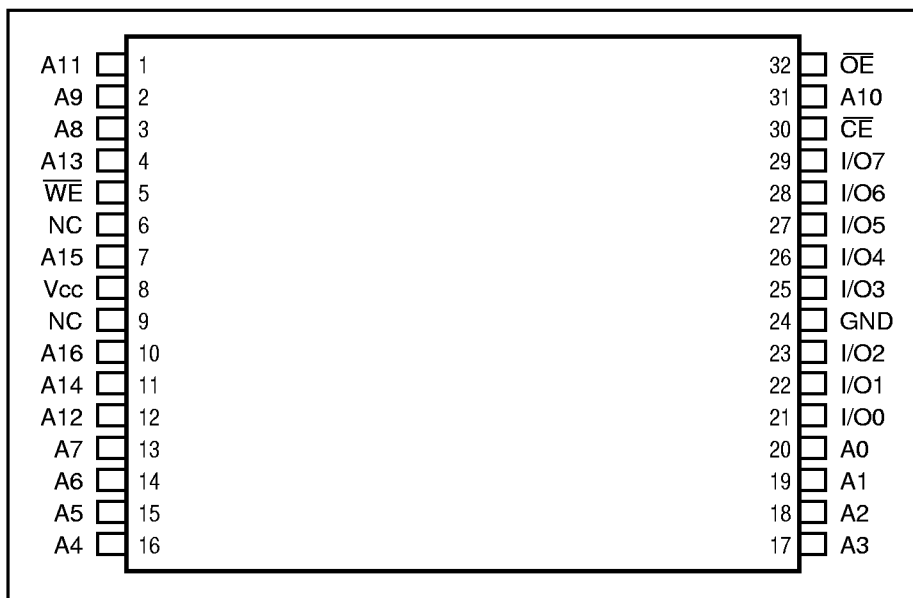
36-ball mini BGA (B)



PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O7	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
NC	No Connection
Vcc	Power
GND	Ground

32-pin sTSSOP (Type I): (H)



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TRUTH TABLE

Mode	\overline{WE}	\overline{CE}	\overline{OE}	I/O0-I/O7	Vcc Current
Not Selected	X	H	X	High-Z	IsB, IsB1
Output Disabled	H	L	H	High-Z	Icc, Icc1
Read	H	L	L	DO _{UT}	Icc, Icc1
Write	L	L	X	DI _N	Icc, Icc1

Note:

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

OPERATING RANGE

Range	Ambient Temperature
Commercial	0°C to +70°C
Industrial	-40°C to +85°C

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit	
V _{CC}	Power Supply Voltage Related to GND	-0.5 to +4.0	V	
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{CC} + 0.5	V	
T _{STG}	Storage Temperature	-65 to +150	°C	
T _{BIAS}	Temperature Under Bias	Com.	-10 to +85	°C
		Ind.	-45 to +90	°C
P _T	Power Dissipation	2.0	W	
I _{out}	DC Output Current	±20	mA	

Notes:

- Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Note:

- Tested initially and after any design or process changes that may affect these parameters.

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AC TEST CONDITIONS (Over Operating Range)

Parameter		Unit
Input Pulse Level ⁽¹⁾	IS62UP2568	0.4V to 2.2V
	IS62UR2568	0.4V to 2.2V
	IS62US2568	0.4V to 1.8V
	IS62UT2568	0.4V to 1.6V
Input Rise and Fall Times		5 ns
Input and Output Timing and Reference Level	IS62UP2568	1.5V
	IS62UR2568	1.1V
	IS62US2568	0.9V
	IS62UT2568	0.8V
Output Load (all test parameters except in Note 2) (see Figure 1)		CL1 = 30 pF + 1TTL Load
Output Load ⁽¹⁾ (all High-Z and Low-Z parameters) (see Figure 1)		CL2 = 5 pF

Notes:

1. Including jig and scope capacitance.
2. $V_{TM} = 2.8V$ for $V_{CC} = 3.0V \pm 0.3V$
 $V_{TM} = 2.3V$ for $V_{CC} = 2.5V \pm 0.2V$
 $V_{TM} = 1.8V$ for $V_{CC} = 2.0V \pm 0.2V$
 $V_{TM} = 1.6V$ for $V_{CC} = 1.8V \pm 0.2V$

AC TEST LOADS

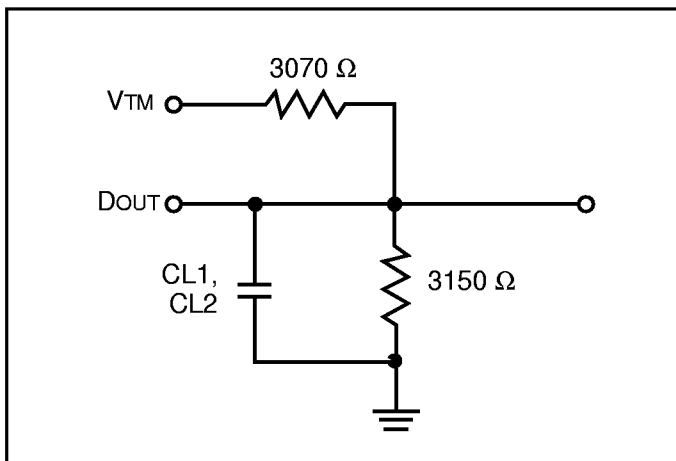


Figure 1

TARGET SPECIFICATION



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DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 3.0V ± 0.3V, I _{OH} = -2.1 mA	2.2	—	V
		V _{CC} = 2.5V ± 0.2V, I _{OH} = -0.5 mA	2.0	—	
		V _{CC} = 2.0V ± 0.2V, I _{OH} = -0.44 mA	1.6	—	
		V _{CC} = 1.8V ± 0.2V, I _{OH} = -0.44 mA	1.4	—	
V _{OL}	Output LOW Voltage	V _{CC} = 3.0V ± 0.3V, I _{OL} = 2.1 mA	—	0.4	V
		V _{CC} = 2.5V ± 0.2V, I _{OL} = 0.5 mA	—	—	
		V _{CC} = 2.0V ± 0.2V, I _{OL} = 0.33 mA	—	—	
		V _{CC} = 1.8V ± 0.2V, I _{OL} = 0.26 mA	—	—	
V _{IH}	Input HIGH Voltage	IS62UP2568	2.2	V _{CC} + 0.2	V
		IS62UR2568	2.0	V _{CC} + 0.2	
		IS62US2568	1.6	V _{CC} + 0.2	
		IS62UT2568	1.4	V _{CC} + 0.2	
V _{IL} ⁽¹⁾	Input LOW Voltage		-0.2	0.4	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	-1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1	1	μA

Note:

1. V_{IL} (min.) = -0.5V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
I _{CC}	Static Operating Power Supply Current	$\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0 mA, f = 0	V _{CC} = 3.0V ± 0.3V	—	15	mA
			V _{CC} = 2.5V ± 0.2V	—	10	
			V _{CC} = 2.0V ± 0.2V	—	8	
			V _{CC} = 1.8V ± 0.2V	—	6	
I _{CC1}	Dynamic Operating Power Supply Current (IS62UP2568)	V _{CC} = 3.0V ± 0.3V I _{OUT} = 0 mA, f = f _{MAX}	55 ns	—	35	mA
			70 ns	—	25	
			100 ns	—	20	
I _{CC1}	Dynamic Operating Power Supply Current (IS62UR2568)	V _{CC} = 2.5V ± 0.2V I _{OUT} = 0 mA, f = f _{MAX}	55 ns	—	20	mA
			70 ns	—	15	
			100 ns	—	8	
I _{CC1}	Dynamic Operating Power Supply Current (IS62US2568)	V _{CC} = 2.0V ± 0.2V I _{OUT} = 0 mA, f = f _{MAX}	55 ns	—	12	mA
			70 ns	—	10	
			100 ns	—	7	
I _{CC1}	Dynamic Operating Power Supply Current (IS62UT2568)	V _{CC} = 1.8V ± 0.2V I _{OUT} = 0 mA, f = f _{MAX}	55 ns	—	11	mA
			70 ns	—	9	
			100 ns	—	6	
I _{SB}	TTL Standby Current (TTL Inputs)	V _{CC} = 3.0V ± 0.3V, $\overline{CE} = V_{IH}$	IS62UP2568	—	0.5	mA
		V _{CC} = 2.5V ± 0.2V, $\overline{CE} = V_{IH}$	IS62UR2568	—	0.3	
		V _{CC} = 2.0V ± 0.2V, $\overline{CE} = V_{IH}$	IS62US2568	—	0.3	
		V _{CC} = 1.8V ± 0.2V, $\overline{CE} = V_{IH}$	IS62UT2568	—	0.3	
I _{SB1}	CMOS Standby	$\overline{CE} \geq V_{CC} - 0.2V$	LL Versions	—	10	μA
			SL Versions	—	2	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

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IS62Ux2568 SERIES

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

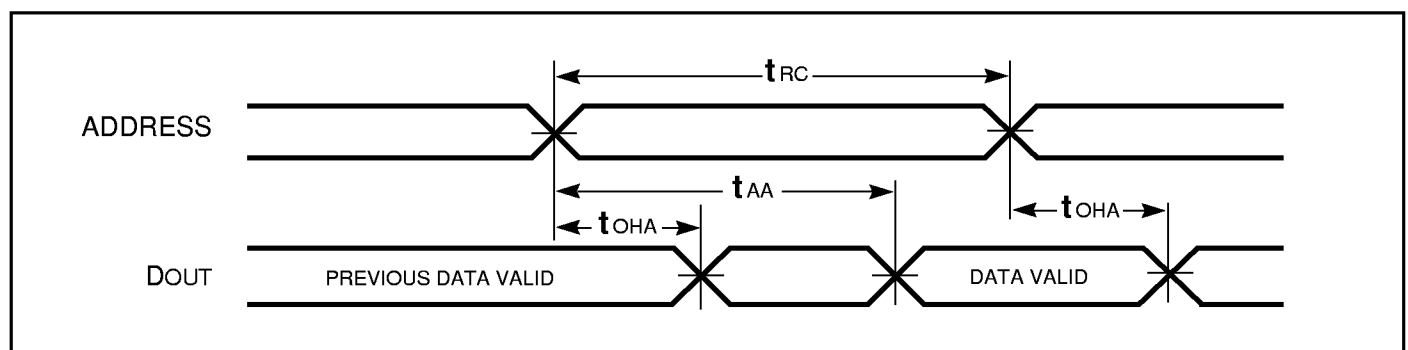
Symbol	Parameter	-55		-70		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55	—	70	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	100	ns
t_{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t_{ACE}	\overline{CE} Access Time	—	55	—	70	—	100	ns
t_{DOE}	\overline{OE} Access Time	—	30	—	35	—	50	ns
$t_{HZOE}^{(2)}$	\overline{OE} to High-Z Output	—	20	—	25	—	30	ns
$t_{LZOE}^{(2)}$	\overline{OE} to Low-Z Output	5	—	5	—	5	—	ns
$t_{HZCE}^{(2)}$	\overline{CE} to High-Z Output	0	20	0	25	0	30	ns
$t_{LZCE}^{(2)}$	\overline{CE} to Low-Z Output	10	—	10	—	10	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4 to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



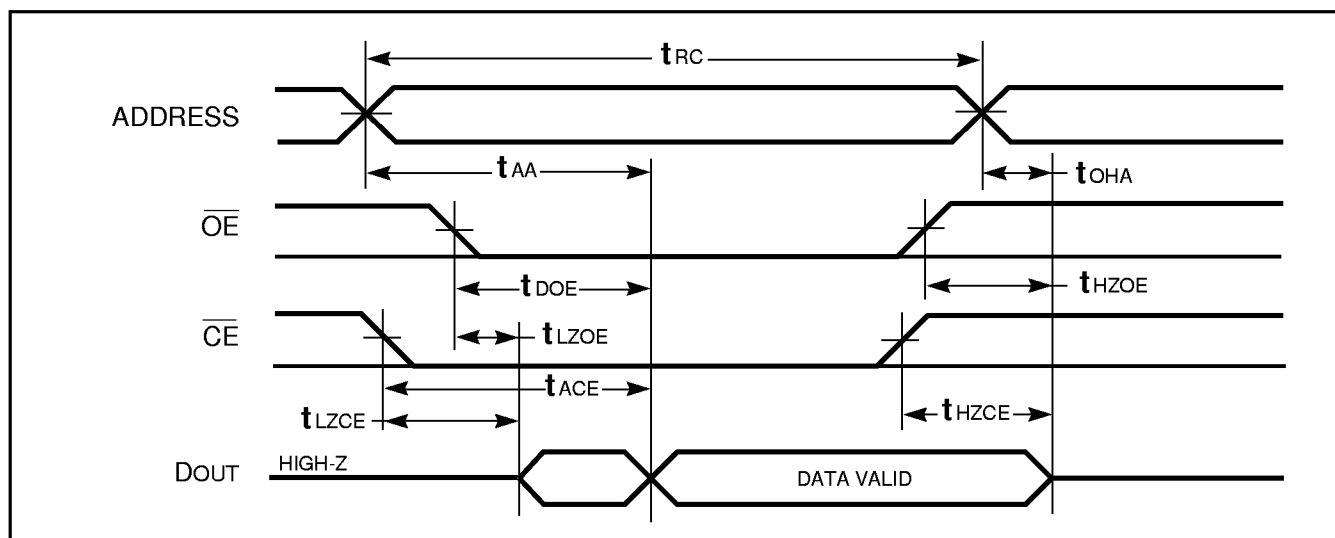
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IS62Ux2568 SERIES

AC WAVEFORMS

READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

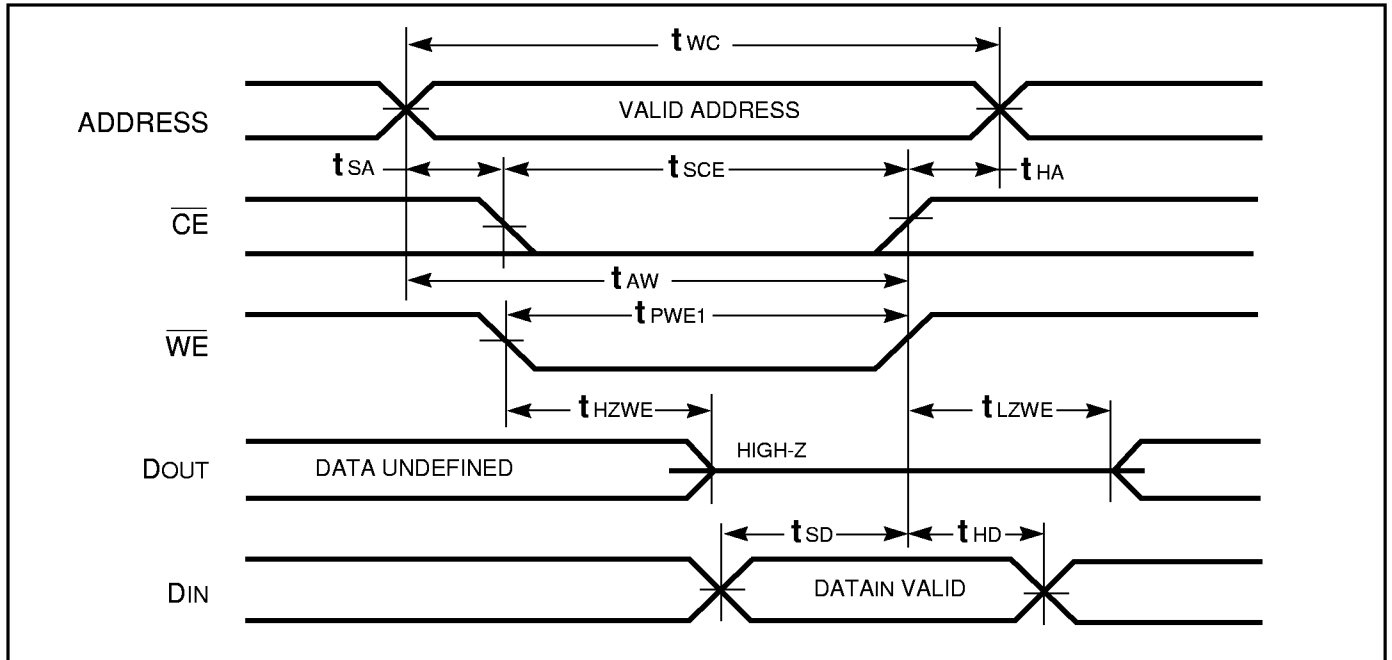
Symbol	Parameter	-55		-70		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{wc}	Write Cycle Time	55	—	70	—	100	—	ns
t _{sce}	\overline{CE} to Write End	45	—	60	—	80	—	ns
t _{aw}	Address Setup Time to Write End	45	—	60	—	80	—	ns
t _{ha}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{sa}	Address Setup Time	0	—	0	—	0	—	ns
t _{pwe1}	\overline{WE} Pulse Width	45	—	60	—	80	—	ns
t _{pwe2}	\overline{WE} Pulse Width	45	—	60	—	80	—	ns
t _{sd}	Data Setup to Write End	25	—	30	—	40	—	ns
t _{hd}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{hzwe} ⁽³⁾	\overline{WE} LOW to High-Z Output	—	30	—	30	—	40	ns
t _{lzwe} ⁽³⁾	\overline{WE} HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

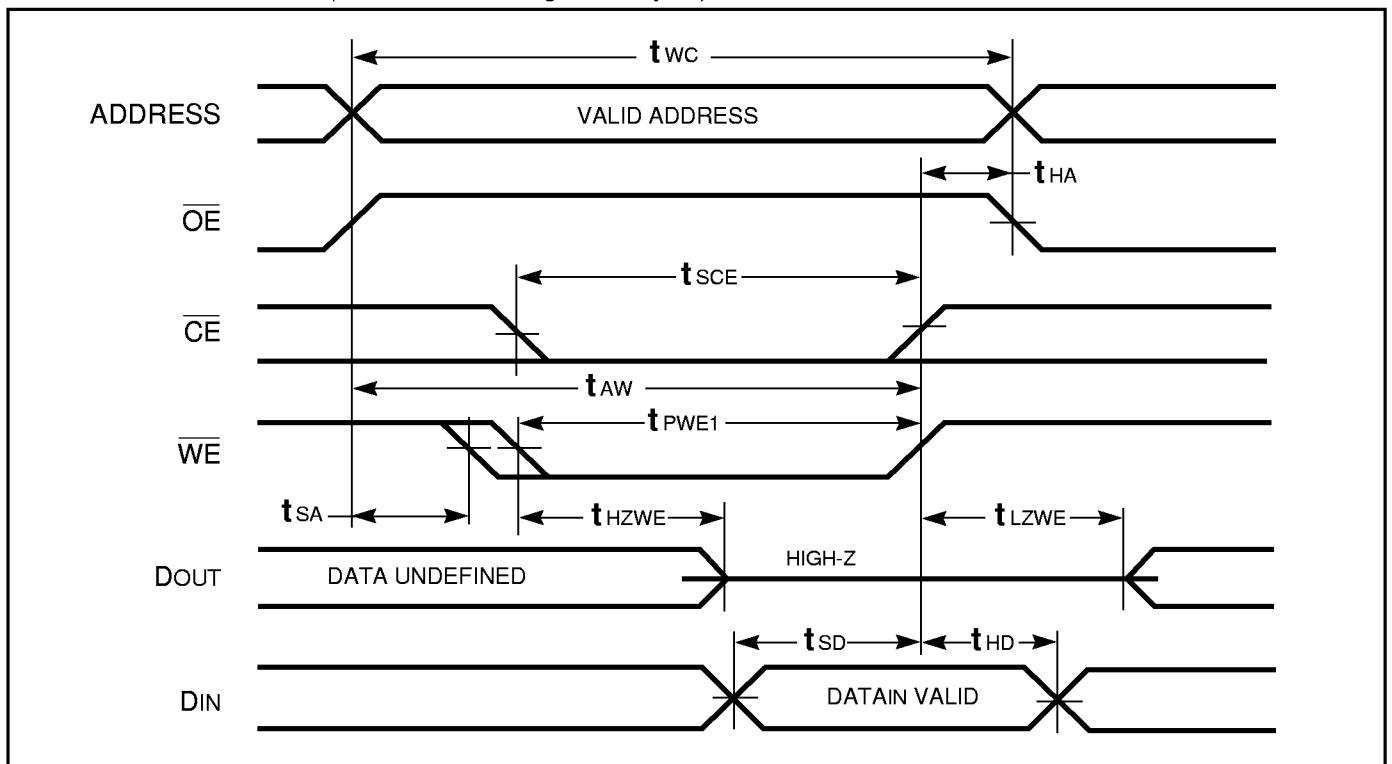
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 1. Transition is measured ± 200 mV from steady-state voltage. Not 100% tested.

IS62Ux2568 SERIES

WRITE CYCLE NO. 1 (\overline{CE} Controlled, \overline{OE} is HIGH or LOW) ⁽¹⁾



WRITE CYCLE NO. 2 (\overline{OE} is HIGH During Write Cycle) ^(1,2)

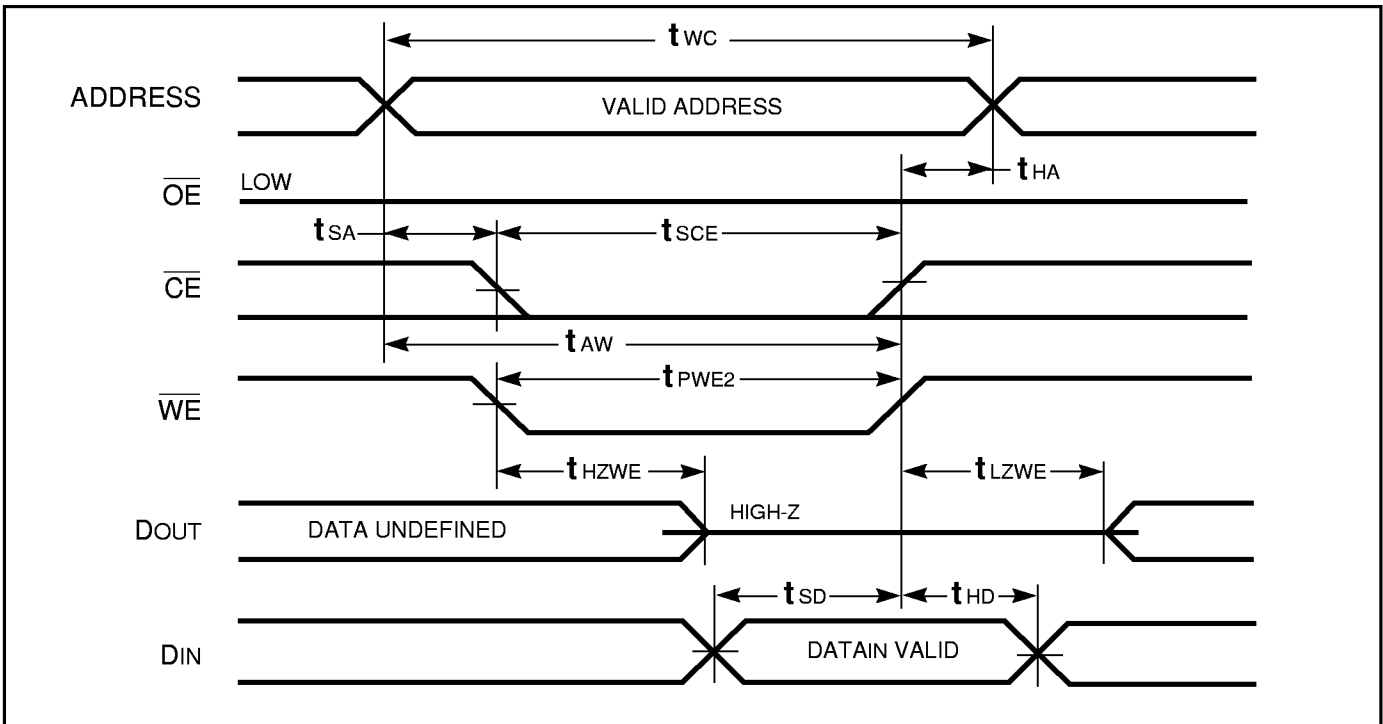


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IS62Ux2568 SERIES



WRITE CYCLE NO. 3 (\overline{OE} is LOW During Write Cycle) ⁽¹⁾



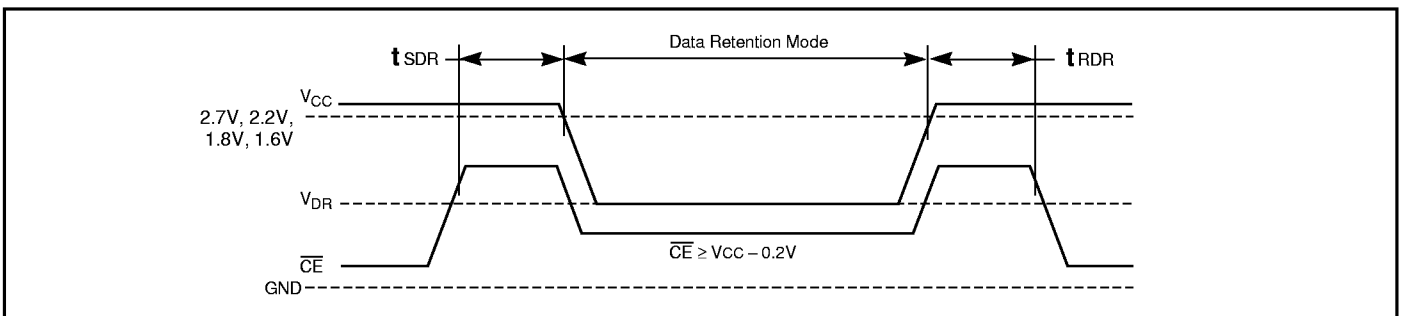
Notes:

1. The internal Write time is defined by the overlap of $\overline{CE} = \text{LOW}$ and $\overline{WE} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with \overline{OE} HIGH for a minimum of 4 ns before $\overline{WE} = \text{LOW}$ to place the I/O in a HIGH-Z state.

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	See Data Retention Waveform	1.0	3.3	V
I_{DR}	Data Retention Current	$V_{CC} = 1.0V$, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$. No input may exceed $V_{CC} + 0.2V$	—	2	μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



Note:

1. 2.7V: IS62UP2568; 2.2V: IS62UR2568; 1.8V: IS62US2568; 1.6V: IS62UT2568.

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IS62Ux2568 SERIES

ORDERING INFORMATION — SL SERIES

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS62UP2568SL-55H	sTSOP (I)
	IS62UP2568SL-55B	Mini BGA
	IS62UR2568SL-55H	sTSOP (I)
	IS62UR2568SL-55B	Mini BGA
	IS62US2568SL-55H	sTSOP (I)
	IS62US2568SL-55B	Mini BGA
	IS62UT2568SL-55H	sTSOP (I)
	IS62UT2568SL-55B	Mini BGA
70	IS62UP2568SL-70H	sTSOP (I)
	IS62UP2568SL-70B	Mini BGA
	IS62UR2568SL-70H	sTSOP (I)
	IS62UR2568SL-70B	Mini BGA
	IS62US2568SL-70H	sTSOP (I)
	IS62US2568SL-70B	Mini BGA
	IS62UT2568SL-70H	sTSOP (I)
	IS62UT2568SL-70B	Mini BGA
100	IS62UP2568SL-100H	sTSOP (I)
	IS62UP2568SL-100B	Mini BGA
	IS62UR2568SL-100H	sTSOP (I)
	IS62UR2568SL-100B	Mini BGA
	IS62US2568SL-100H	sTSOP (I)
	IS62US2568SL-100B	Mini BGA
	IS62UT2568SL-100H	sTSOP (I)
	IS62UT2568SL-100B	Mini BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62UP2568SL-55HI	sTSOP (I)
	IS62UP2568SL-55BI	Mini BGA
	IS62UR2568SL-55HI	sTSOP (I)
	IS62UR2568SL-55BI	Mini BGA
	IS62US2568SL-55HI	sTSOP (I)
	IS62US2568SL-55BI	Mini BGA
	IS62UT2568SL-55HI	sTSOP (I)
	IS62UT2568SL-55BI	Mini BGA
70	IS62UP2568SL-70HI	sTSOP (I)
	IS62UP2568SL-70BI	Mini BGA
	IS62UR2568SL-70HI	sTSOP (I)
	IS62UR2568SL-70BI	Mini BGA
	IS62US2568SL-70HI	sTSOP (I)
	IS62US2568SL-70BI	Mini BGA
	IS62UT2568SL-70HI	sTSOP (I)
	IS62UT2568SL-70BI	Mini BGA
100	IS62UP2568SL-100HI	sTSOP (I)
	IS62UP2568SL-100BI	Mini BGA
	IS62UR2568SL-100HI	sTSOP (I)
	IS62UR2568SL-100BI	Mini BGA
	IS62US2568SL-100HI	sTSOP (I)
	IS62US2568SL-100BI	Mini BGA
	IS62UT2568SL-100HI	sTSOP (I)
	IS62UT2568SL-100BI	Mini BGA

TARGET SPECIFICATION

ISSI[®]**IS62Ux2568 SERIES**

ORDERING INFORMATION — LL SERIES**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
55	IS62UP2568LL-55H	sTSOP (I)
	IS62UP2568LL-55B	Mini BGA
	IS62UR2568LL-55H	sTSOP (I)
	IS62UR2568LL-55B	Mini BGA
	IS62US2568LL-55H	sTSOP (I)
	IS62US2568LL-55B	Mini BGA
	IS62UT2568LL-55H	sTSOP (I)
	IS62UT2568LL-55B	Mini BGA
	70	IS62UP2568LL-70H
IS62UP2568LL-70B		Mini BGA
IS62UR2568LL-70H		sTSOP (I)
IS62UR2568LL-70B		Mini BGA
IS62US2568LL-70H		sTSOP (I)
IS62US2568LL-70B		Mini BGA
IS62UT2568LL-70H		sTSOP (I)
IS62UT2568LL-70B		Mini BGA
100		IS62UP2568LL-100H
	IS62UP2568SL-100B	Mini BGA
	IS62UR2568LL-100H	sTSOP (I)
	IS62UR2568LL-100B	Mini BGA
	IS62US2568LL-100H	sTSOP (I)
	IS62US2568LL-100B	Mini BGA
	IS62UT2568LL-100H	sTSOP (I)
	IS62UT2568LL-100B	Mini BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62UP2568LL-55HI	sTSOP (I)
	IS62UP2568LL-55BI	Mini BGA
	IS62UR2568LL-55HI	sTSOP (I)
	IS62UR2568LL-55BI	Mini BGA
	IS62US2568LL-55HI	sTSOP (I)
	IS62US2568LL-55BI	Mini BGA
	IS62UT2568LL-55HI	sTSOP (I)
	IS62UT2568LL-55BI	Mini BGA
	70	IS62UP2568LL-70HI
IS62UP2568LL-70BI		Mini BGA
IS62UR2568LL-70HI		sTSOP (I)
IS62UR2568LL-70BI		Mini BGA
IS62US2568LL-70HI		sTSOP (I)
IS62US2568LL-70BI		Mini BGA
IS62UT2568LL-70HI		sTSOP (I)
IS62UT2568LL-70BI		Mini BGA
100		IS62UP2568LL-100HI
	IS62UP2568LL-100BI	Mini BGA
	IS62UR2568LL-100HI	sTSOP (I)
	IS62UR2568LL-100BI	Mini BGA
	IS62US2568LL-100HI	sTSOP (I)
	IS62US2568LL-100BI	Mini BGA
	IS62UT2568LL-100HI	sTSOP (I)
	IS62UT2568LL-100BI	Mini BGA

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