CD74FCT841T, CD74FCT843T, CD74FCT845T, CD74FCT2841T

December 1996

Fast CMOS Bus Interface Latches

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (FCT2841 Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Description

These devices are buffered interface latches. These transparent latches with three-state outputs, are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. The CD74FCT841T and CD74FCT2841T are 10-bit latches, the CD74FCT843T is a 9-bit latch, and the CD74FCT845T is an 8-bit latch.

The CD74FCT2841T device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

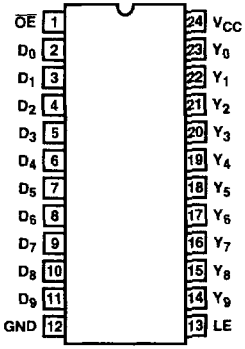
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT841ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT841BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT841CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841CTQM	-40 to 85	24 Ld QSOP	M24.15-P

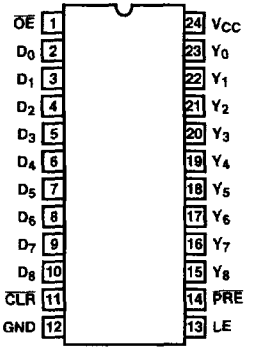
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

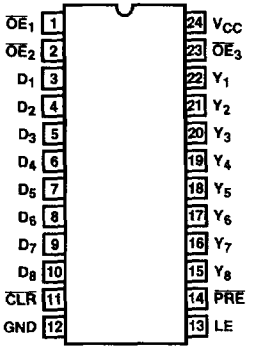
CD74FCT841T, CD74FCT2841T (QSOP, SOIC)
TOP VIEW



CD74FCT843T (QSOP, SOIC)
TOP VIEW



CD74FCT845T (QSOP, SOIC)
TOP VIEW

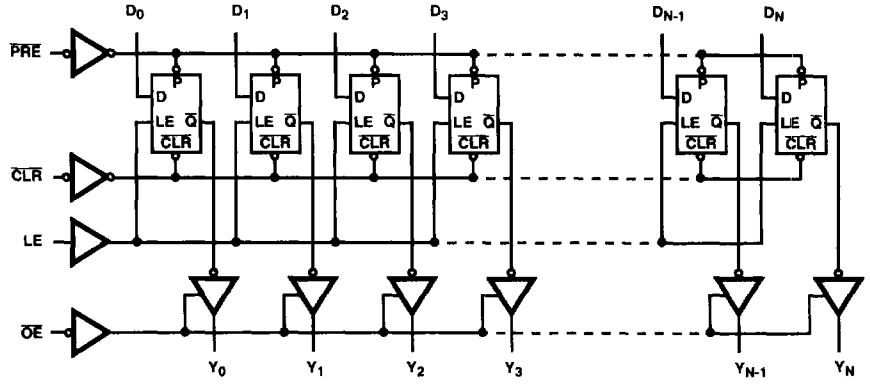


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4177.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS	INTERNAL
	$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_N	Y_N	Q_N
High-Z	H	H	H	X	X	Z	X
	H	H	H	H	L	Z	L
	H	H	H	H	H	Z	H
Latched (High Z)	H	H	H	L	X	Z	NC
Transparent	H	H	L	H	L	L	L
	H	H	L	H	H	H	H
Latched	H	H	L	L	X	NC	NC
Preset	H	L	L	X	X	H	H
Clear	L	H	L	X	X	L	L
Preset	L	L	L	X	X	H	H
Latched (High Z)	L	H	H	L	X	Z	L
Latched (High Z)	H	L	H	L	X	Z	H

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   NC = No Change
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
Y_N	Three-State Latch Outputs
D_N	Latch Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Control
$\overline{CLR}$	Clear Latch
$\overline{PRE}$	Preset Latch High, Preset Overrides CLR
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 75
QSOP Package 100
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Current	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Current	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz(Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND; LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} f_i ≈ 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} Eight Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.0	6.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	14.0 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 12) MIN	CT MAX	UNITS
CD74FCT841T, CD74FCT2841T									
Propagation Delay D_N to Y_N (LE = HIGH)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
Setup Time Data to LE	t_{SU}	C_L = 50pF R_L = 500Ω	2.5	-	2.5	-	2.5	-	ns
Hold Time Data to LE	t_H		2.5	-	2.5	-	2.5	-	ns
Propagation Delay LE to Y_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C_L = 300pF (Note 13) R_L = 500Ω	-	16.0	-	15.5	-	15.0	ns
LE Pulse Width (HIGH)(Note 3)	t_W	C_L = 50pF R_L = 500Ω	4.0	-	4.0	-	4.0	-	ns
Output Enable Time $\overline{OE}$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
Output Disable Time(Note 3) $\overline{OE}$ to Y_N	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns
		C_L = 5 pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns
CD74FCT843T, CD74FCT845T									
Propagation Delay D_N to Y_N (LE = HIGH)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
Setup Time Data to LE	t_{SU}	C_L = 50pF R_L = 500Ω	2.5	-	2.5	-	2.5	-	ns
Hold Time Data to LE	t_H		2.5	-	2.5	-	2.5	-	ns

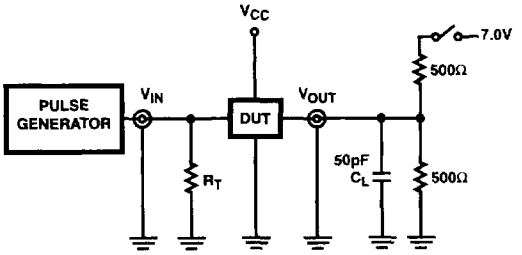
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 12) MIN	CT MAX	UNITS
Propagation Delay LE to Y_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
Propagation Delay $\overline{PRE}$ to Y_N	t_{PLH}	C_L = 50pF R_L = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
Recovery Time $\overline{PRE}$ to Y_N	t_{REM}		1.5	11.0	1.5	10.0	1.5	9.0	ns
Propagation Delay $\overline{CLR}$ to Y_N	t_{PLH}		1.5	11.0	1.5	10.0	1.5	9.0	ns
Recovery Time(Note 13) $\overline{CLR}$ to Y_N	t_{REM}		1.5	13.0	1.5	10.0	1.5	9.0	ns
LE Pulse Width (Note 13) (HIGH)	t_W		4.0	-	4.0	-	4.0	-	ns
$\overline{PRE}$ Pulse Width (Note 13) (LOW)	t_W		5.0	-	4.0	-	4.0	-	ns
$\overline{CLR}$ Pulse Width (Note 13) (LOW)	t_W		4.0	-	4.0	-	4.0	-	ns
Output Enable Time $\overline{OE}$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
Output Disable Time (Note 13) $\overline{OE}$ to Y_N	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		C_L = 5pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

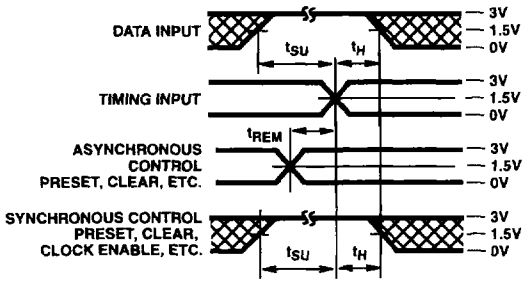


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

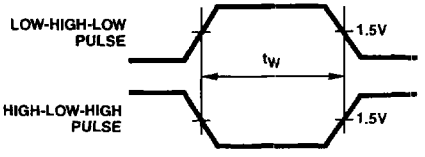


FIGURE 3. PULSE WIDTH

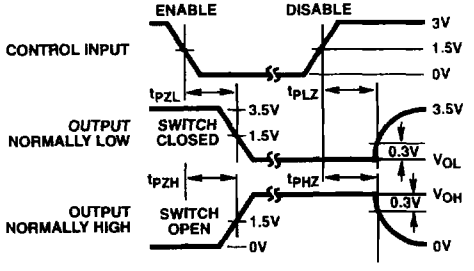


FIGURE 4. ENABLE AND DISABLE TIMING

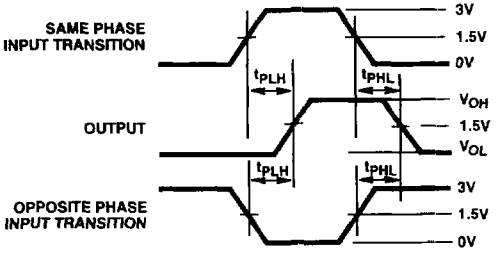


FIGURE 5. PROPAGATION DELAY