



PRELIMINARY

MTS1512K8CxxSJ2

# 4Mb Monolithic SRAM

## 4Mb, 512K x 8, Asynchronous SRAM Memory Array

### AVAILABILITY:

- DSCC SMD 5962-95600
- QML-Q Compliant
- Mil 883 Compliant

### FEATURES:

- High Speed, Asynchronous operation
- Fully Static, No Clocks required
- Center Power & Ground for improved noise immunity
- Easy Memory Array expansion with use of Chip Select (CS\ ) and Output Enable (OE\ )
- All Inputs/Outputs are TTL compatible
- Low Power with Data Retention Functionality available in our MTCS1512K8C-L & MTCS1512K8C-U product groupings
- Product Access Speed Options:
  - 12, 15, 17, 20, 25, 35 and 45ns
- Package Option:
  - 36LD-CSOJ

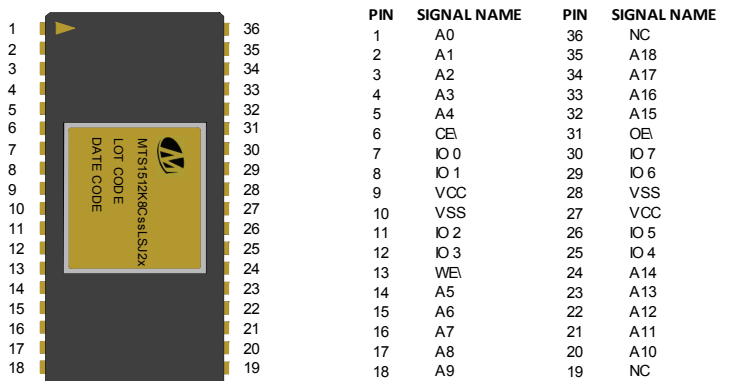
### FUNCTIONAL DESCRIPTION

The MTS1512K8C is a high-performance CMOS Static Random Access Memory (SRAM), organized as 512K words by 8-bits wide, containing a total density of 512K bytes. Memory expansion is easily achieved through use of the Chip-Select (CS\ ) and Output Enable (OE\ ) control inputs along with the tri-state output drivers. Writing to the device is accomplished by driving CS\ and WE\ LOW. Data on the eight IO pins (IO0-IO7) is then written into the addressed location specified on the Address Input pins (A0-A18).

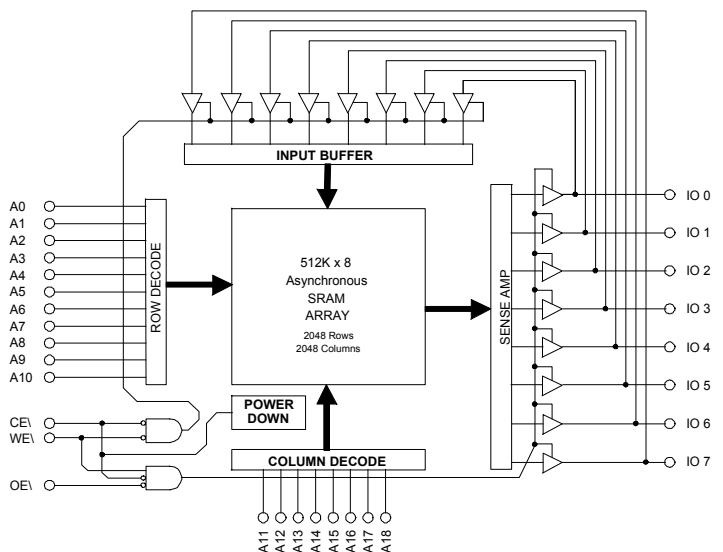
Reading from the MTS1512K8C is accomplished by driving Chip Select (CS\ ) and Output Enable (OE\ ) LOW, while forcing Write Enable (WE\ ) HIGH. Under these stimulus conditions, the contents of the addressed memory location (A0-A18) will be available on the Output pins (IO0-IO7).

The MTS1512K8C is placed into an inactive, High-Impedance state when the device has been de-selected by driving Chip-Select (CS\ ) HIGH. The eight Input-Output lines (IO0-IO7) are also in a High-Impedance state when the MTS1512K8C is placed into a WRITE operation by driving Chip-Select (CS\ ) and Write Enable (WE\ ) LOW.

### PIN DIAGRAM



### FUNCTIONAL BLOCK



### MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT	UNITS
Operating Temperature	T <sub>A</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Supply Voltage Relative to GND	V <sub>S</sub>	-0.5 to VCC+0.5	V
DC Voltage applied to Outputs in High-Z	V <sub>OZG</sub>	-0.5 to VCC+0.5	V
DC Input Voltage	V <sub>I</sub>	-0.5 to VCC+0.5	V



PRELIMINARY

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# 4Mb Monolithic SRAM

## CAPACITANCE

PARAMETER	SYMBOL	CONDITIONS	MAX	UNITS
Input Capacitance	$C_I$	$V_{IN}=0V, f=1.0MHz$	8	pf
Output Capacitance	$C_O$	$V_{IN}=0V, f=1.0MHz$	8	pf

## AC TEST CONDITIONS

PARAMETER	LIMIT	UNITS
Input Pulse Levels	VSS to 3.0	V
Input Rise & Fall times	$\leq 3$	ns
Input Timing Reference levels	1.5	V
Output Timing Reference levels	1.5	V
Output Test Load	Figure 1	
Output Test Load (Z testing)	Figure 2	

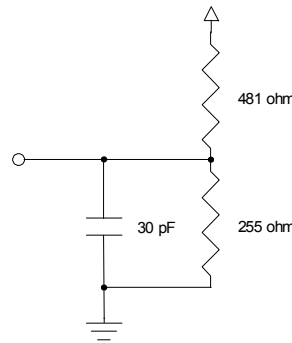


Figure 1

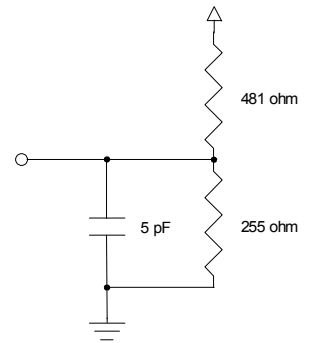


Figure 2

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTE(S)
Output HIGH Voltage	$V_{OH}$	$V_{CC}=\text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		V	1
Output LOW Voltage	$V_{OL}$	$V_{CC}=\text{Min.}, I_{OH} = 8.0\text{mA}$		0.4	V	1
Input HIGH Voltage	$V_{IH}$		2.2	$V_{CC}+0.5$	V	1
Input LOW Voltage	$V_{IL}$		-0.5	0.8	V	1,2
Input leakage current	$I_{IX}$	$GND < V_I < V_{CC}$	-10	10	$\mu\text{A}$	
Output leakage current	$I_{OZ}$	$GND < V_O < V_{CC}$ (Output disabled)	-10	10	$\mu\text{A}$	
Operating current	$I_{CC1}$	12ns		90	mA	3
		15ns		90	mA	3
		17ns		90	mA	3
		20ns		80	mA	3
		25ns		80	mA	3
		35ns		80	mA	3
		45ns		80	mA	3
Standby, TTL inputs	$I_{CC2}$	$CS \geq V_{IH}$ , all other inputs $\leq V_{IL}$ , $V_{CC} = \text{MAX}$ , $f = 0$ , Outputs Open		45	mA	
Standby, CMOS inputs	$I_{CC3}$	$CS \geq V_{CC}-0.2V$ ; $V_{CC} = \text{MAX}$ , $V_{IN} \leq V_{SS} + 0.2V$ or $V_{IH} \geq V_{CC}-0.2V$ ; $f = 0$		20	mA	



PRELIMINARY

MTS1512K8CxxSJ2

4Mb Monolithic SRAM

AC SWITCHING CHARACTERISTICS

READ

PARAMETER	SYMBOL	12ns		15ns		17ns		20ns		UNITS	NOTE(S)
		MTC1512K8C12		MTC1512K8C15		MTC1512K8C20		MTC1512K8C25			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
VCC to First Access	t <sub>POWER</sub>	100	-	100	-	100	-	100	-	us	15
READ Cycle Time	t <sub>RC</sub>	12	-	15	-	20	-	25	-	ns	
Address Access Time	t <sub>AC</sub>	-	12	-	15	-	17	-	20	ns	
Chip Enable Access Time	t <sub>ACS</sub>	-	12	-	15	-	17	-	20	ns	
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	3	-	ns	
Chip Enable to Output in Low-Z	t <sub>CLZ</sub>	3	-	3	-	3	-	3	-	ns	4,7
Chip Disable to Output in High-Z	t <sub>CHZ</sub>	0	6	0	7	0	8	0	8	ns	4,6,7
Output Enable Access Time	t <sub>OE</sub>	-	6	-	7	-	8	-	10	ns	
Output Enable to Output in Low-Z	t <sub>OLZ</sub>	0	-	0	-	0	-	0	-	ns	4,7
Output Disable to Output in High-Z	t <sub>OHZ</sub>	-	6	-	7	-	8	-	8	ns	4,6,7
Chip Enable to Power-Up	t <sub>PU</sub>	0	-	0	-	0	-	0	-	ns	
Chip Disable to Power-Down	t <sub>PD</sub>	-	12	-	15	-	17	-	20	ns	

PARAMETER	SYMBOL	25ns		35ns		45ns		UNITS	NOTE(S)
		MTS1512K8C25		MTS1512K8C35		MTS1512K8C45			
		MIN	MAX	MIN	MAX	MIN	MAX		
VCC to First Access	t <sub>POWER</sub>	100	-	100	-	100	-	us	15
READ Cycle Time	t <sub>RC</sub>	25	-	15	-	20	-	ns	
Address Access Time	t <sub>AC</sub>	-	25	-	15	-	20	ns	
Chip Enable Access Time	t <sub>ACS</sub>	-	25	-	15	-	20	ns	
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	ns	
Chip Enable to Output in Low-Z	t <sub>CLZ</sub>	3	-	3	-	3	-	ns	4,7
Chip Disable to Output in High-Z	t <sub>CHZ</sub>	0	10	0	12	0	15	ns	4,6,7
Output Enable Access Time	t <sub>OE</sub>	-	12	-	15	-	22	ns	
Output Enable to Output in Low-Z	t <sub>OLZ</sub>	0	-	0	-	0	-	ns	4,7
Output Disable to Output in High-Z	t <sub>OHZ</sub>	-	10	-	12	-	15	ns	4,6,7
Chip Enable to Power-Up	t <sub>PU</sub>	0	-	0	-	0	-	ns	
Chip Disable to Power-Down	t <sub>PD</sub>	-	25	-	35	-	45	ns	



**PRELIMINARY**

**MTS1512K8CxxSJ2**

**4Mb Monolithic SRAM**

**WRITE**

PARAMETER	SYMBOL	12ns		15ns		17ns		20ns		UNITS	NOTE(S)
		MTS1512K8C12		MTS1512K8C15		MTS1512K8C20		MTS1512K8C25			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
WRITE Cycle Time	$t_{WC}$	12	-	15	-	17	-	20	-	ns	
Chip Enable to End of WRITE	$t_{CW}$	8	-	10	-	12	-	14	-	ns	
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	0	-	ns	
Address Hold from End of WRITE	$t_{AH}$	0	-	0	-	0	-	0	-	ns	
Address Valid to End of WRITE	$t_{AW}$	8	-	10	-	12	-	14	-	ns	
WRITE Pulse Width	$t_{WP}$	8	-	10	-	12	-	14	-	ns	
Data Setup Time	$t_{DS}$	7	-	8	-	9	-	10	-	ns	
Data Hold Time	$t_{DH}$	0	-	0	-	0	-	0	-	ns	
WRITE Disable to Output in Low-Z	$t_{WLZ}$	3	-	4	-	4	-	5	-	ns	4,6,7
WRITE Enable to Output in High-Z	$t_{WHZ}$	-	5	-	7	-	8	-	8	ns	4,6,7

PARAMETER	SYMBOL	25ns		35ns		45ns		UNITS	NOTE(S)
		MTS1512K8C25		MTS1512K8C35		MTS1512K8C45			
		MIN	MAX	MIN	MAX	MIN	MAX		
WRITE Cycle Time	$t_{WC}$	25	-	35	-	45	-	ns	
Chip Enable to End of WRITE	$t_{CW}$	16	-	18	-	24	-	ns	
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	ns	
Address Hold from End of WRITE	$t_{AH}$	0	-	0	-	0	-	ns	
Address Valid to End of WRITE	$t_{AW}$	16	-	18	-	24	-	ns	
WRITE Pulse Width	$t_{WP}$	16	-	18	-	24	-	ns	
Data Setup Time	$t_{DS}$	10	-	12	-	15	-	ns	
Data Hold Time	$t_{DH}$	0	-	0	-	0	-	ns	
WRITE Disable to Output in Low-Z	$t_{WLZ}$	5	-	5	-	5	-	ns	4,6,7
WRITE Enable to Output in High-Z	$t_{WHZ}$	-	10	-	10	-	12	ns	4,6,7



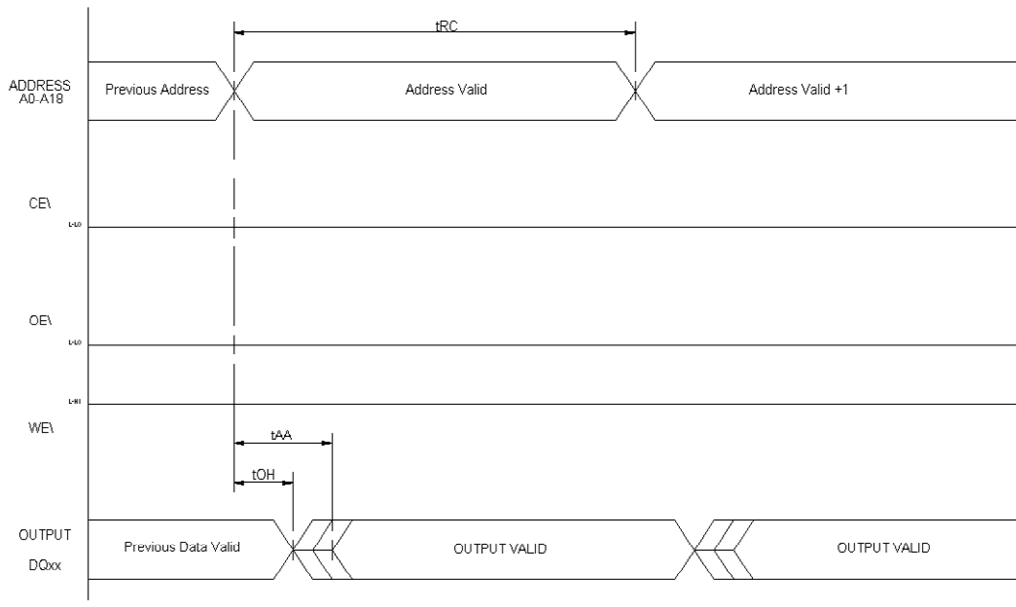
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MTS1512K8CxxSJ2

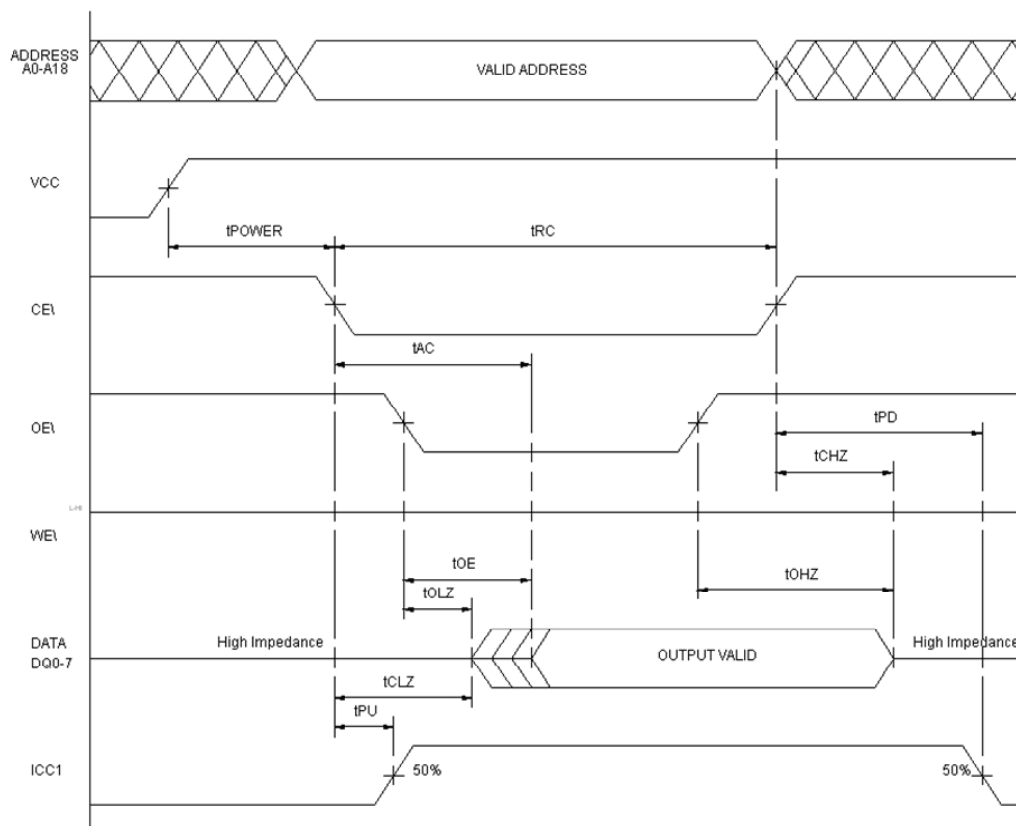
# 4Mb Monolithic SRAM

## AC READ Waveforms

READ Cycle #1: Continuous NOTE 8,9



READ Cycle #2: OE Controlled NOTE 2





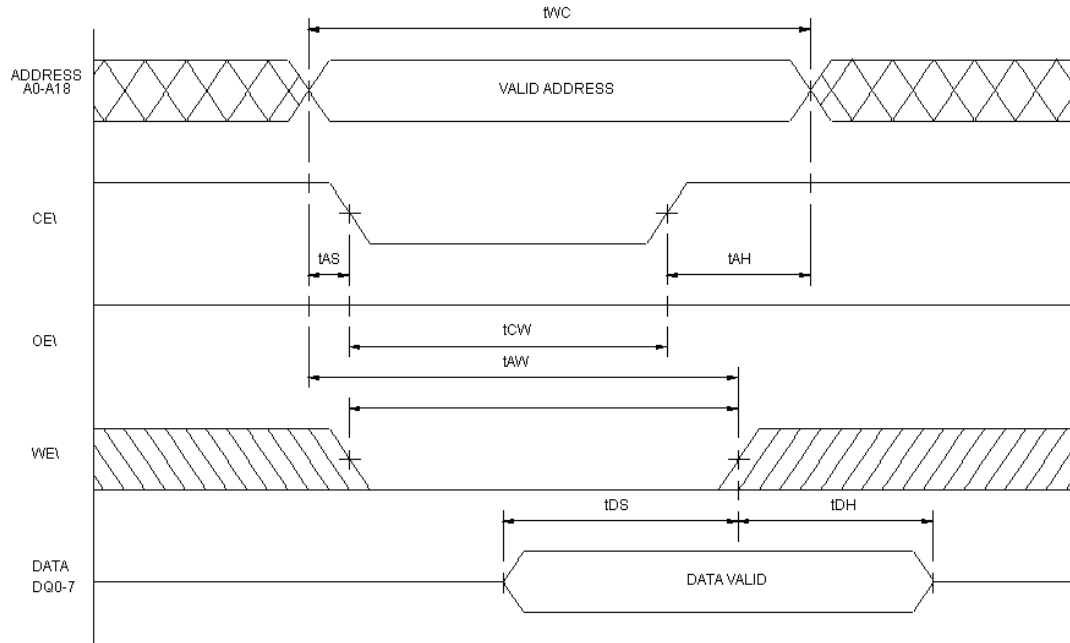
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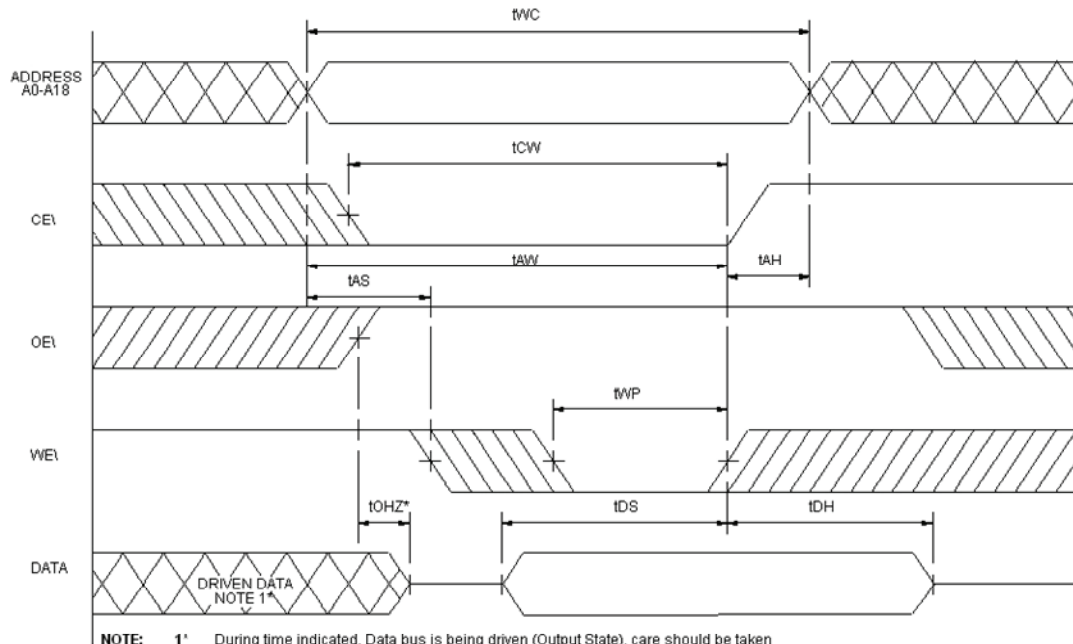
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## AC WRITE WAVEFORMS

WRITE Cycle #1: CE Controlled NOTE 12



WRITE Cycle #2: WE Controlled, OE HIGH during WRITE NOTE 12, 13



NOTE: 1\* During time indicated, Data bus is being driven (Output State), care should be taken to avoid bus contention, follow spec tOHZ\* prior to setting input Data

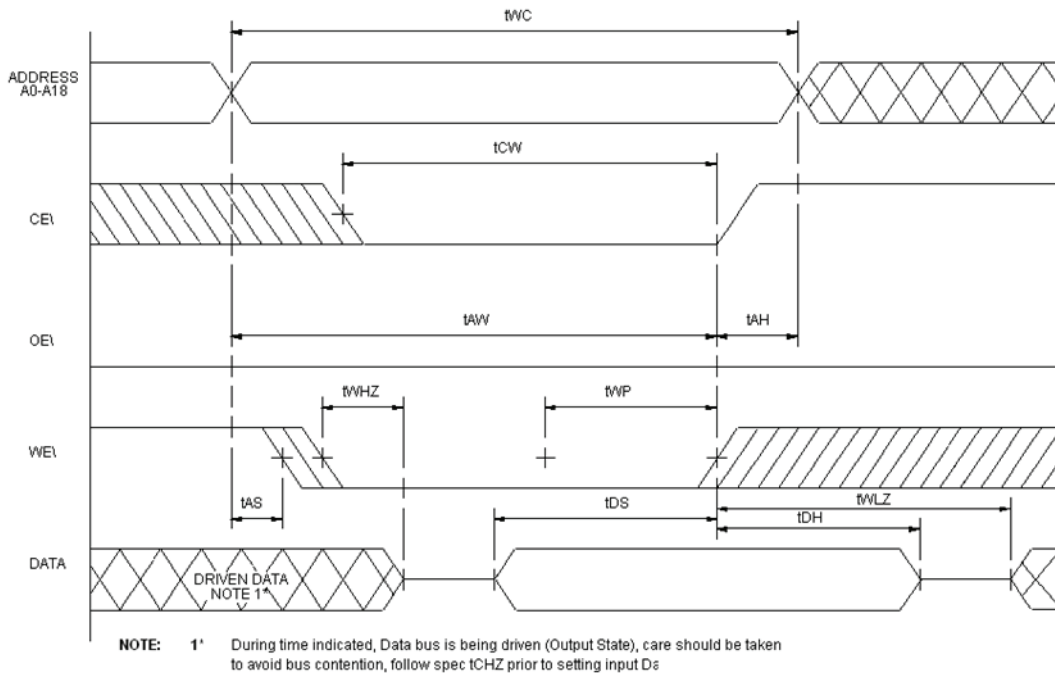


PRELIMINARY

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# 4Mb Monolithic SRAM

WRITE Cycle #3: WE Controlled, OE LOW during WRITE NOTE 7, 12, 14



**NOTES:**

- 1) All Voltages referenced to VSS (GND)
- 2) -2.0V for Pulse  $\leq 20\text{ns}$
- 3) ICC is dependent on output loading, specification testing per Output Load figures 1&2
- 4) This parameter is guaranteed but not tested
- 5) Test conditions as specified in Output Load figure 1
- 6) tCLZ, tCHZ, tOLZ, tOHZ, tV LZ and tVHZ are specified with use of Output Load figure 2
- 7) At any given voltage and/or temperature condition, tCHZ is less than tCLZ and tVHZ is less than tV LZ
- 8) WE is High for READ Cycles
- 9) Device is continuously selected. Chip Select and Output Enable are driven to their Active state
- 10) Address Valid prior to, or coincident with latest occurring Chip Select
- 11) Full device operation requires linear VCC ramp from VDR to VCC(MIN)  $\geq 50\mu\text{s}$  or statble at VCC(MIN)  $\geq 50\mu\text{s}$  Max
- 12) Chips Select and Write Enable can initiate and terminate a WRITE Cycle
- 13) Output Enable is Inactive when HIGH
- 14) Output Enable is Active when LOW
- 15) tPOWER gives the minimum amount of time that the power supply should be at typical VCC values until the first memory access can be performed

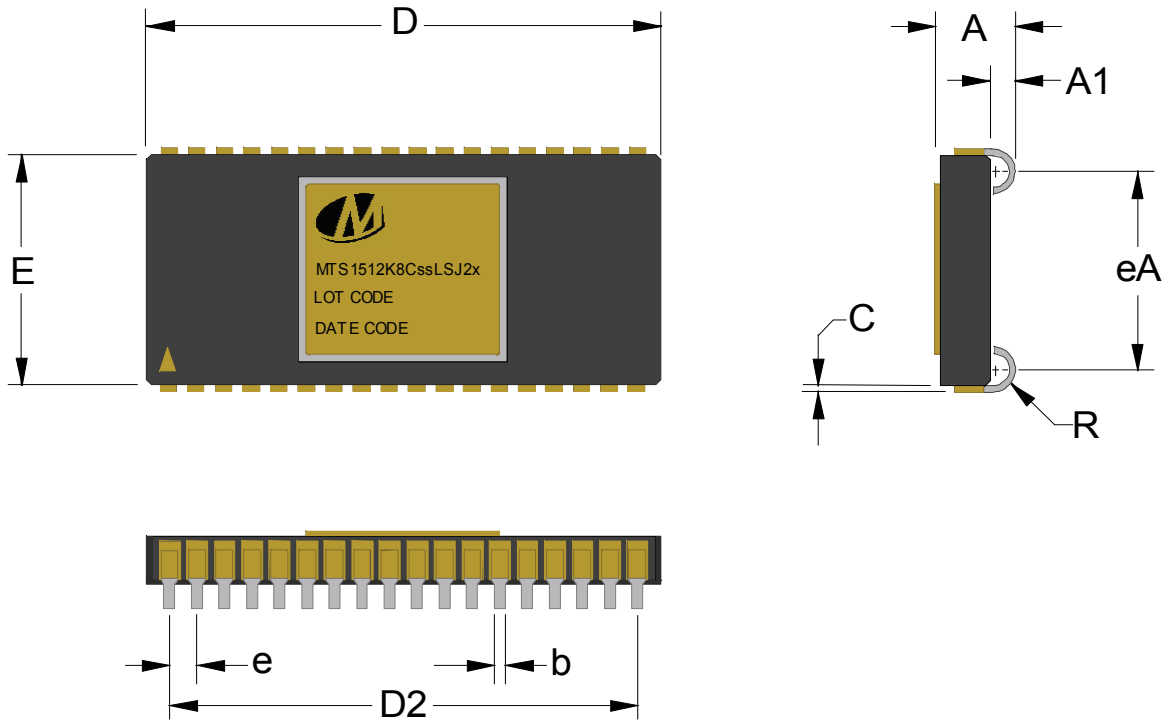


PRELIMINARY

MTS1512K8CxxSJ2

# 4Mb Monolithic SRAM

## MECHANICAL DIAGRAM



Symbol	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	2.920	3.680	0.115	0.145
A1	0.630	1.140	0.025	0.045
b	0.380	0.510	0.015	0.020
C	0.150	0.300	0.006	0.012
D	23.39	23.85	0.921	0.939
D2	21.46	21.71	0.845	0.855
E	10.54	10.92	0.415	0.430
e	1.270 BSC		0.050 BSC	
eA	9.420	9.830	0.371	0.387
R	0.760 TYP		0.030 TYP	





**PRELIMINARY**

**MTS1512K8CxxSJ2**

**4Mb Monolithic SRAM**

**ORDERING INFORMATION**

PART NUMBER	SPEED	PCK	LEAD	Vinput	Power	DR	TEMP / SCREENING
MTS1512K8C45SJ2SQ	45ns	36CSOJ	SnPb	Center	Std	NA	QML
5962-9560001QMA	45ns	36CSOJ	SnPb	Center	Std	NA	QML
MTS1512K8C45SJ2Q	45ns	36CSOJ	Au	Center	Std	NA	QML
5962-9560001QMC	45ns	36CSOJ	Au	Center	Std	NA	QML
MTS1512K8C45SJ2SB	45ns	36CSOJ	SnPb	Center	Std	NA	883
5962-9560001MMA	45ns	36CSOJ	SnPb	Center	Std	NA	883
MTS1512K8C45SJ2B	45ns	36CSOJ	Au	Center	Std	NA	883
5962-9560001MMC	45ns	36CSOJ	Au	Center	Std	NA	883
MTS1512K8C45SJ2SM	45ns	36CSOJ	SnPb	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C45SJ2M	45ns	36CSOJ	Au	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C45SJ2SE	45ns	36CSOJ	SnPb	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C45SJ2E	45ns	36CSOJ	Au	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C35SJ2SQ	35ns	36CSOJ	SnPb	Center	Std	NA	QML
5962-9560002QMA	35ns	36CSOJ	SnPb	Center	Std	NA	QML
MTS1512K8C35SJ2Q	35ns	36CSOJ	Au	Center	Std	NA	QML
5962-9560002QMC	35ns	36CSOJ	Au	Center	Std	NA	QML
MTS1512K8C35SJ2SB	35ns	36CSOJ	SnPb	Center	Std	NA	883
5962-9560002MMA	35ns	36CSOJ	SnPb	Center	Std	NA	883
MTS1512K8C35SJ2B	35ns	36CSOJ	Au	Center	Std	NA	883
5962-9560002MMC	35ns	36CSOJ	Au	Center	Std	NA	883
MTS1512K8C35SJ2SM	35ns	36CSOJ	SnPb	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C35SJ2M	35ns	36CSOJ	Au	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C35SJ2SE	35ns	36CSOJ	SnPb	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C35SJ2E	35ns	36CSOJ	Au	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C25SJ2SQ	25ns	36CSOJ	SnPb	Center	Std	NA	QML
5962-9560003QMA	25ns	36CSOJ	SnPb	Center	Std	NA	QML
MTS1512K8C25SJ2Q	25ns	36CSOJ	Au	Center	Std	NA	QML
5962-9560003QMC	25ns	36CSOJ	Au	Center	Std	NA	QML
MTS1512K8C25SJ2SB	25ns	36CSOJ	SnPb	Center	Std	NA	883
5962-9560003MMA	25ns	36CSOJ	SnPb	Center	Std	NA	883
MTS1512K8C25SJ2B	25ns	36CSOJ	Au	Center	Std	NA	883
5962-9560003MMC	25ns	36CSOJ	Au	Center	Std	NA	883
MTS1512K8C25SJ2SM	25ns	36CSOJ	SnPb	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C25SJ2M	25ns	36CSOJ	Au	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C25SJ2SE	25ns	36CSOJ	SnPb	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C25SJ2E	25ns	36CSOJ	Au	Center	Std	NA	Extended Temp (-40°C to +105°C)



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PART NUMBER	SPEED	PCK	LEAD	Vinput	Power	DR	TEMP / SCREENING
MTS1512K8C20SJ2SQ	20ns	36CSOJ	SnPb	Center	Std	NA	QML
5962-9560004QMA	20ns	36CSOJ	SnPb	Center	Std	NA	QML
MTS1512K8C20SJ2Q	20ns	36CSOJ	Au	Center	Std	NA	QML
5962-9560004QMC	20ns	36CSOJ	Au	Center	Std	NA	QML
MTS1512K8C20SJ2SB	20ns	36CSOJ	SnPb	Center	Std	NA	883
5962-9560004MMA	20ns	36CSOJ	SnPb	Center	Std	NA	883
MTS1512K8C20SJ2B	20ns	36CSOJ	Au	Center	Std	NA	883
5962-9560004MMC	20ns	36CSOJ	Au	Center	Std	NA	883
MTS1512K8C20SJ2SM	20ns	36CSOJ	SnPb	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C20SJ2M	20ns	36CSOJ	Au	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C20SJ2SE	20ns	36CSOJ	SnPb	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C20SJ2E	20ns	36CSOJ	Au	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C15SJ2SQ	15ns	36CSOJ	SnPb	Center	Std	NA	QML
5962-9560014QMA	15ns	36CSOJ	SnPb	Center	Std	NA	QML
MTS1512K8C15SJ2Q	15ns	36CSOJ	Au	Center	Std	NA	QML
5962-9560014QMC	15ns	36CSOJ	Au	Center	Std	NA	QML
MTS1512K8C15SJ2SB	15ns	36CSOJ	SnPb	Center	Std	NA	883
5962-9560014MMA	15ns	36CSOJ	SnPb	Center	Std	NA	883
MTS1512K8C15SJ2B	15ns	36CSOJ	Au	Center	Std	NA	883
5962-9560014MMC	15ns	36CSOJ	Au	Center	Std	NA	883
MTS1512K8C15SJ2SM	15ns	36CSOJ	SnPb	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C15SJ2M	15ns	36CSOJ	Au	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C15SJ2SE	15ns	36CSOJ	SnPb	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C15SJ2E	15ns	36CSOJ	Au	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C12SJ2SQ	12ns	36CSOJ	SnPb	Center	Std	NA	QML
5962-9560016QMA	12ns	36CSOJ	SnPb	Center	Std	NA	QML
MTS1512K8C12SJ2Q	12ns	36CSOJ	Au	Center	Std	NA	QML
5962-9560016QMC	12ns	36CSOJ	Au	Center	Std	NA	QML
MTS1512K8C12SJ2SB	12ns	36CSOJ	SnPb	Center	Std	NA	883
MTS1512K8C12SJ2B	12ns	36CSOJ	Au	Center	Std	NA	883
MTS1512K8C12SJ2SM	12ns	36CSOJ	SnPb	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C12SJ2M	12ns	36CSOJ	Au	Center	Std	NA	Mil-Temp (-55°C to +125°C)
MTS1512K8C12SJ2SE	12ns	36CSOJ	SnPb	Center	Std	NA	Extended Temp (-40°C to +105°C)
MTS1512K8C12SJ2E	12ns	36CSOJ	Au	Center	Std	NA	Extended Temp (-40°C to +105°C)