

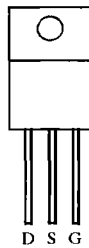
N-Channel Enhancement-Mode Transistors

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
500	0.515	12

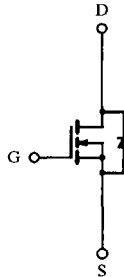
Parametric limits in accordance with MIL-S-19500/592 where applicable.

TO-254AA
Hermetic Package



Top View

Case Isolated



N-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	12
		$T_C = 100^\circ\text{C}$	8
Pulsed Drain Current	I_{DM}	48	A
Avalanche Current	I_{AR}	12	A
Maximum Power Dissipation	P_D	150	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

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N-/P-Channel
MOSFETS

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	0.83	$^\circ\text{C/W}$

2N7228JANTX/JANTXV

Siliconix

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ ^a	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1000\ \mu\text{A}$	500			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}, T_J = -55^\circ\text{C}$			5.0	
		$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}, T_J = 25^\circ\text{C}$	2.0		4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}, T_J = 125^\circ\text{C}$			± 200	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$			25	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			250	
		$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			1000	
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$			0.515	Ω
		$V_{GS} = 10\text{ V}, I_D = 8\text{ A}, T_J = 125^\circ\text{C}$			0.9	
Dynamic						
Total Gate Charge ^c	Q_g	$V_{DS} = 250\text{ V}, V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	55		120	nC
Gate-Source Charge ^c	Q_{gs}		5		19	
Gate-Drain Charge ^c	Q_{gd}		27		70	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 250\text{ V}, R_L = 20.8\ \Omega$ $I_D \cong 12\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.35\ \Omega$			35	ns
Rise Time ^c	t_r				190	
Turn-Off Delay Time ^c	$t_{d(off)}$				170	
Fall Time ^c	t_f				130	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				12	A
Pulsed Current	I_{SM}				48	
Diode Forward Voltage ^b	V_{SD}	$I_F = 12\text{ A}, V_{GS} = 0\text{ V}$			1.7	V
Reverse Recovery Time	t_{rr}	$I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$			1600	ns

Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Independent of operating temperature.