# DRAF124E

### Silicon PNP epitaxial planar type

For digital circuits Complementary to DRCF124E DRA3124E in ML3 type package

#### Features

- Low collector-emitter saturation voltage  $V_{CE(sat)}$
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

#### Packaging

DRAF124E0L Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

#### Absolute Maximum Ratings $T_a = 25^{\circ}C$

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	-50	V	
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	-50	V	
Collector current	I <sub>C</sub>	I <sub>C</sub> -100		
Total power dissipation *	P <sub>T</sub>	100	mW	
Junction temperature	Tj	T <sub>j</sub> 150		
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

Note) \*: Copper plate at the collector is  $5.0 \text{ mm}^2$  on substrate at  $10 \text{ mm} \times 12 \text{ mm} \times 0.8 \text{ mm}$ .

#### Electrical Characteristics $T_a = 25^{\circ}C \pm 3^{\circ}C$

Package
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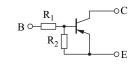
- Code
- ML3-N4-B
  - Package dimension clicks here.  $\!\!\!\!\rightarrow$

#### Pin Name

- 1: Base
- 2: Emitter
- 3: Collector

Marking Symbol: LE

Internal Connection



Resistance value	R <sub>1</sub>	22	kΩ
	R <sub>2</sub>	22	kΩ

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	$I_{\rm C} = -10 \ \mu {\rm A}, I_{\rm E} = 0$	-50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_{\rm C} = -2 \text{ mA}, I_{\rm B} = 0$	-50			V
Collector-base cutoff current (Emitter open)	I <sub>CBO</sub>	$V_{\rm CB} = -50$ V, $I_{\rm E} = 0$			- 0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{CE} = -50 \text{ V}, I_{B} = 0$			- 0.5	μΑ
Emitter-base cutoff current (Collector open)	I <sub>EBO</sub>	$V_{EB} = -6 \text{ V}, I_C = 0$			- 0.2	mA
Forward current transfer ratio	h <sub>FE</sub>	$V_{\rm CE} = -10$ V, $I_{\rm C} = -5$ mA	60			
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_{\rm C} = -10 \text{ mA}, I_{\rm B} = -0.5 \text{ mA}$			-0.25	V
Input voltage (ON)	V <sub>I(on)</sub>	$V_{CE} = -0.2 \text{ V}, I_C = -5 \text{ mA}$	-2.6			V
Input voltage (OFF)	V <sub>I(off)</sub>	$V_{CE} = -5 \text{ V}, I_C = -100 \mu\text{A}$			- 0.8	V
Input resistance	R <sub>1</sub>		-30%	22	+30%	kΩ
Resistance ratio	R <sub>1</sub> / R <sub>2</sub>		0.8	1.0	1.2	

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

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