TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74HC393AP,TC74HC393AF,TC74HC393AFN

#### **Dual Binary Counter**

The TC74HC393A is a high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

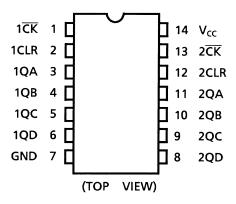
This device changes state on the negative going transition of the  $\overline{CK}$  pulse. The counter can be reset to "0" (QA to QD = "L") by a high at the CLR input regardless of other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

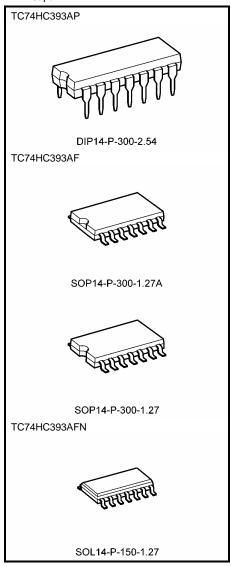
#### **Features**

- High speed:  $f_{max} = 72 \text{ MHz (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $ICC = 4 \mu A \text{ (max)}$  at  $Ta = 25^{\circ}C$
- High noise immunity: VNIH = VNIL = 28% VCC (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: |IOH| = IOL = 4 mA (min)
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: VCC (opr) = 2 to 6 V
- Pin and function compatible with 74LS393

#### **Pin Assignment**



Note: xxxFN (JEDEC SOP) is not available in Japan.

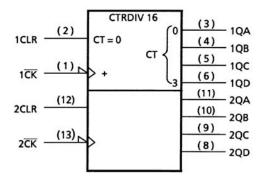


Weight

DIP14-P-300-2.54 : 0.96 g (typ.) SOP14-P-300-1.27A : 0.18 g (typ.) SOP14-P-300-1.27 : 0.18 g (typ.) SOL14-P-150-1.27 : 0.12 g (typ.)



# **IEC Logic Symbol**

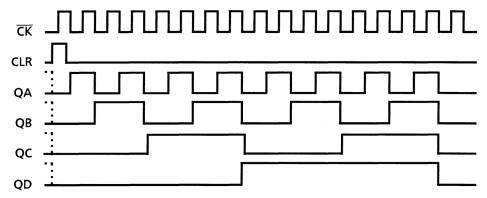


#### **Truth Table**

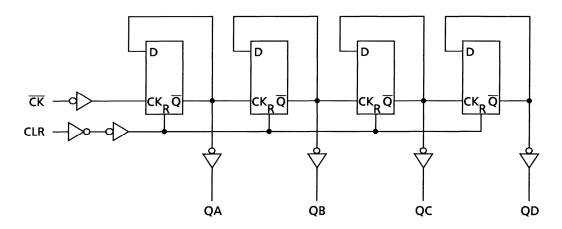
Inp	uts	Outputs								
CK	CLR	QA	QB	Q	QD					
Х	Н	L	L	L	L					
$\neg$	L	Count Up								
	L	No Change								

X: Don't care

# **Timing Chart**



#### **System Diagram**





#### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	Vcc	-0.5 to 7	V
DC input voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	−0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	lout	±25	mA
DC V <sub>CC</sub> /ground current	Icc	±50	mA
Power dissipation	P <sub>D</sub>	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

#### **Recommended Operating Conditions (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	Vcc	2 to 6	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>		V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
		0 to 1000 (V <sub>CC</sub> = 2.0 V)	
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0 to 500 (V <sub>CC</sub> = 4.5 V)	ns
		0 to 400 ( $V_{CC} = 6.0 \text{ V}$ )	

Note: The recommended operating conditions are required to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.



### **Electrical Characteristics**

#### **DC Characteristics**

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit	
Gridiaeterieuee	Cymbol				Min	Тур.	Max	Min	Max		
		_		2.0	1.50	_	_	1.50	_		
High-level input voltage	V <sub>IH</sub>			4.5	3.15	_	_	3.15	_	V	
Ŭ				6.0	4.20	_	_	4.20	_		
				2.0	_	_	0.50		0.50		
Low-level input voltage	VIL	_		4.5	_	_	1.35	_	1.35	V	
Ŭ				6.0		_	1.80	_	1.80		
	Vон	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0		1.9			
				4.5	4.4	4.5	_	4.4	_		
High-level output voltage				6.0	5.9	6.0		5.9		V	
			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31		4.13			
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80		5.63			
		V <sub>IN</sub> = V <sub>IH</sub> or		2.0		0.0	0.1	_	0.1		
			$I_{OL} = 20 \mu A$	4.5	_	0.0	0.1	_	0.1		
Low-level output voltage	V <sub>OL</sub>			6.0	_	0.0	0.1	_	0.1	V	
		$V_{IL}$	I <sub>OL</sub> = 4 mA	4.5	_	0.17	0.26	_	0.33		
			I <sub>OL</sub> = 5.2 mA	6.0	_	0.18	0.26	_	0.33		
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	_	_	±0.1		±1.0	μА	
Quiescent supply current	I <sub>CC</sub>	$V_{IN} = V_{C}$	<sub>C</sub> or GND	6.0	_	_	4.0	_	40.0	μА	

### Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Test Condition			Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Тур.	Limit	Limit	
Minimum pulpo width	4		2.0	_	75	95	
Minimum pulse width ( $\overline{\text{CK}}$ )	tw (H)	_	4.5	_	15	19	ns
(CK)	t <sub>W (L)</sub>		6.0	_	13	16	
Minimum pulse width	t <sub>W</sub> (H)		2.0	_	75	95	
(CLR)		_	4.5	_	15	19	ns
(CLK)			6.0	_	13	16	
	t <sub>rem</sub>		2.0	_	25	30	
Minimum removal time		_	4.5	_	5	6	ns
			6.0		5	5	
	f		2.0		6	5	
Clock frequency		_	4.5	_	32	27	MHz
			6.0		38	32	



# AC Characteristics (C<sub>L</sub> = 15 pF, V<sub>CC</sub> = 5 V, Ta = 25°C, input: $t_{\text{r}} = t_{\text{f}} = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Output transition time	tTLH	_	_	4	8	ns
Carpar manement anno	t <sub>THL</sub>					
Propagation delay time	t <sub>pLH</sub>			12	20	ns
( CK -QA)	t <sub>pHL</sub>	_		12	20	113
Propagation delay time	t <sub>pLH</sub>			16	31	ns
( CK -QB)	t <sub>pHL</sub>	_		10	31	113
Propagation delay time	t <sub>pLH</sub>			21	38	ns
( CK -QC)	t <sub>pHL</sub>	_	_	21	30	115
Propagation delay time	t <sub>pLH</sub>			25	40	
( CK -QD)	$t_{pHL}$	_	_	25	46	ns
Propagation delay time				15	26	20
(CLR-Qn)	t <sub>pHL</sub>	_	_	15	26	ns
Maximum clock frequency	f <sub>max</sub>	_	35	72		MHz



AC Characteristics ( $C_L = 50 \text{ pF}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
Situationionio	Symbol		V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	Offic
	<b>+</b>		2.0	_	25	75	_	95	
Output transition time	t <sub>TLH</sub>	_	4.5	_	7	15	_	19	ns
	t <sub>THL</sub>		6.0	_	6	13	_	16	
Propagation delay	tarri		2.0	_	45	120	_	150	
time	<sup>t</sup> pLH	_	4.5	_	15	24	_	30	ns
( CK -QA)	t <sub>pHL</sub>		6.0	_	13	20	_	26	
Propagation delay	<b>.</b>		2.0		60	180		225	
time	t <sub>pLH</sub>	_	4.5	_	20	36	_	45	ns
( CK -QB)	t <sub>pHL</sub>		6.0	_	17	31	_	38	
Propagation delay	t <sub>pLH</sub>		2.0	_	80	220	_	275	
time		_	4.5	_	25	44	_	55	ns
( CK -QC)	t <sub>pHL</sub>		6.0	_	21	37	_	47	
Propagation delay	t <sub>pLH</sub>		2.0		100	260		325	
time		_	4.5	_	30	52	_	65	ns
( CK -QD)	t <sub>pHL</sub>		6.0	_	26	44	_	55	
Propagation delay			2.0		55	150		190	
time	$t_{pHL}$	_	4.5	_	18	30	_	38	ns
(CLR-Qn)			6.0	_	15	26	_	33	
			2.0	6	22	_	5	_	
Maximum clock frequency	f <sub>max</sub>	_	4.5	32	67	_	27	_	MHz
·			6.0	38	77	_	32	_	
Input capacitance	C <sub>IN</sub>			_	5	10	_	10	pF
Power dissipation capacitance	C <sub>PD</sub> (Note)	_		_	40	_	_	_	pF

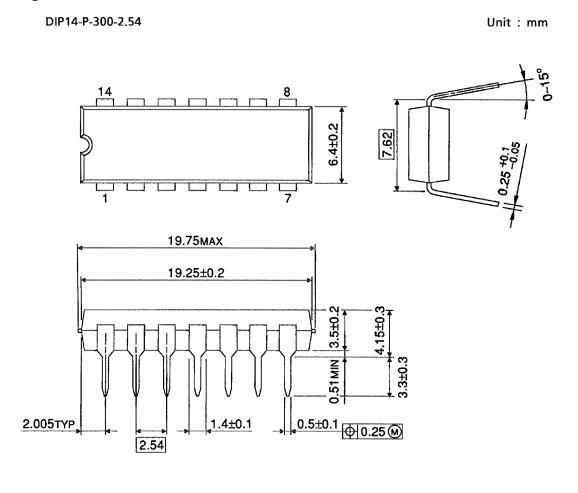
Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC}$  (opr) =  $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$  (per counter)



# **Package Dimensions**



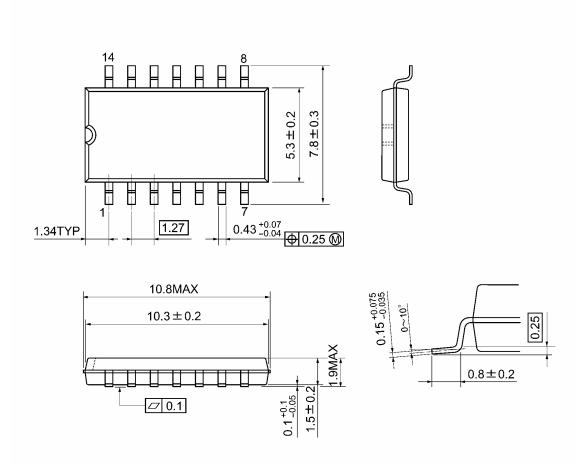
7

Weight: 0.96 g (typ.)



# **Package Dimensions**

SOP14-P-300-1.27A Unit: mm

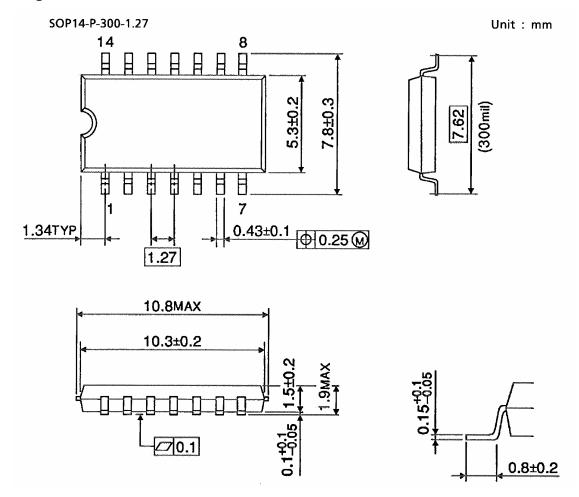


8

Weight: 0.18 g (typ.)



### **Package Dimensions**

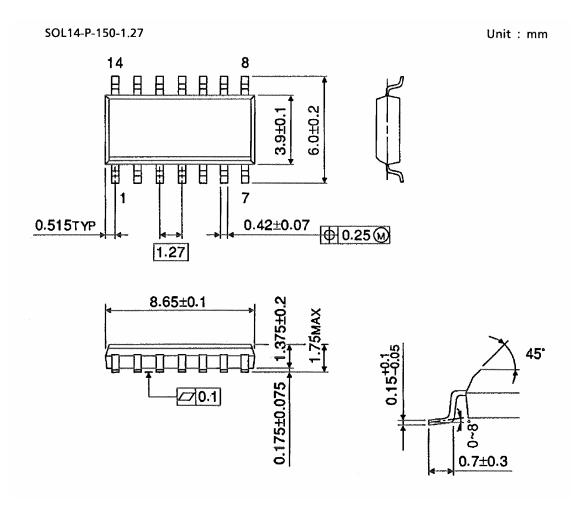


9

Weight: 0.18 g (typ.)



# **Package Dimensions (Note)**



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

Note: Lead (Pb)-Free Packages

DIP14-P-300-2.54 SOP14-P-300-1.27A SOL14-P-150-1.27

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