MH5128ABNA-70L,-85L,-10L,-12L,-15L / MH5128ABNA-70H,-85H,-10H,-12H,-15H

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The MH5128ABNA is a 4194304-bits CMOS static RAM module organized as 524288-words by 8-bits. It consists of four industry standard 128K × 8 static RAMs (M5M51008AVP, RV) and two decoders.

The stand-by current is low enough for a battery back-up application. It is mounted a TSOP package.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH5128ABNA-70L MH5128ABNA-85L MH5128ABNA-10L MH5128ABNA-12L MH5128ABNA-15L	70ns 85ns 100ns 120ns 150ns	180mA	250 μ A (Vcc = 3.0V)
MH5128ABNA-70H MH5128ABNA-85H MH5128ABNA-10H MH5128ABNA-12H MH5128ABNA-15H	70ns 85ns 100ns 120ns 150ns		90 μ A (Vcc = 3.0V)

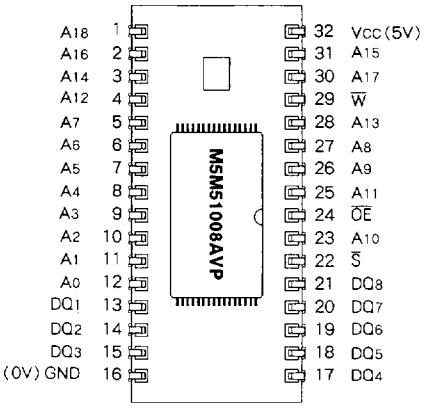
- Single + 5V power supply
- No clocks, no refresh
- Data-hold on + 2V power supply
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)

[Both side, 2-Layer]



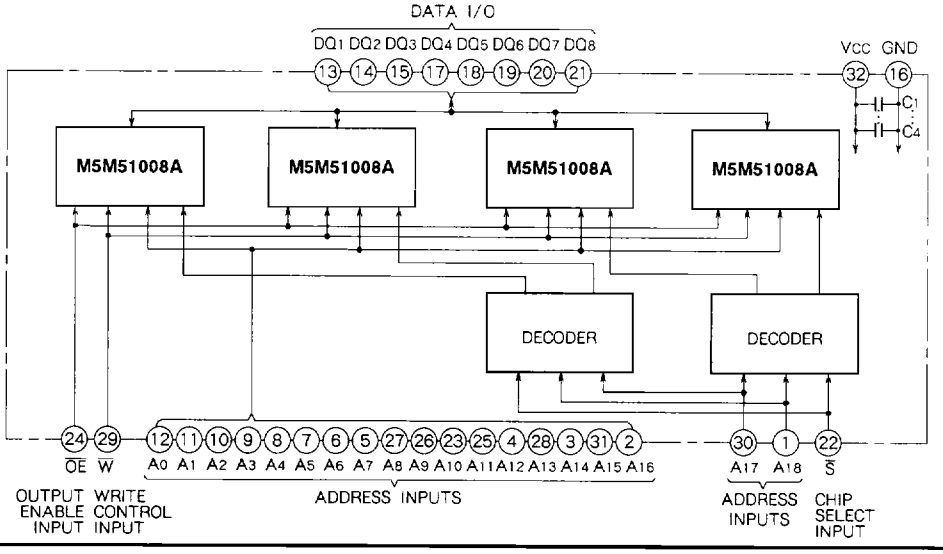
Outline 32N1B-M

FUNCTION

The operation mode of the MH5128ABNA is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.(see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output

BLOCK DIAGRAM



enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non-selection	High-impedance	Stand-by
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3 ~7	V
V_I	Input voltage		− 0.3~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	T_a = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 40~100	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	Low input voltage	− 0.3		0.8	V
V_{IH}	High input voltage	2.2		V_{CC}+0.3	V

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			− 0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = − 1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 4	μA
I_O	Output current in off-state	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 4	μA
I_{CC1}	Active supply current (AC. MOS level)	$\overline{S}$ ≦ 0.2V, output open other input ≦ 0.2V or ≧ V_{CC} − 0.2V Min. cycle			110	160	mA
I_{CC2}	Active supply current (AC. TTL level)	$\overline{S}$ = V_{IL}, output open other input = V_{IL} or V_{IH} Min. cycle			150	200	mA
I_{CC3}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V, A_{17}~A_{18} ≦ 0.2V or ≧ V_{CC} − 0.2V other inputs = 0~V_{CC}	ABNA-L			450	μA
			ABNA-H		12	130	μA
I_{CC4}	Stand-by supply current	$\overline{S}$ = V_{IH}, A_{17}~A_{18} = V_{CC} or GND other inputs = 0~V_{CC}				70	mA
C_I	Input capacitance (T_a = 25℃)	V_I = GND, V_i = 25mVrms, f = 1MHz				50	pF
C_O	Output capacitance (T_a = 25℃)	V_O = GND, V_o = 25mVrms, f = 1MHz				40	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark).
2. Typical value is V_{CC} = 5V, T_a = 25℃.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH} = 3.0V, V_{IL} = 0V

Input rise and fall time 5ns

Reference levels ..... V_{OH} = V_{OL} = 1.5V

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ..... Fig. 1, C_L = 100pF(-10L, -12L, -15L, -10H, -12H, -15H)

C_L = 30pF (-70L, -85L, -70H, -85H)

C_L = 5pF (for t_{en}, t_{dis})

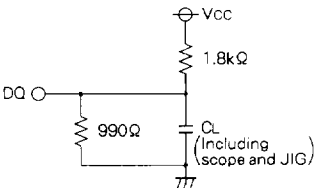


Fig. 1 Output load

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits										Unit
		MH5128-70		MH5128-85		MH5128-10		MH5128-12		MH5128-15		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		150		ns
$t_{a(A)}$	Address access time		70		85		100		120		150	ns
$t_{a(S)}$	Chip select access time		70		85		100		120		150	ns
$t_{a(OE)}$	Output enable access time		30		35		45		50		60	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		35		40		45		50		55	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		30		35		40	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5		5		5		5		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		5		ns
$t_{v(A)}$	Data valid time after address change	5		10		10		10		10		ns

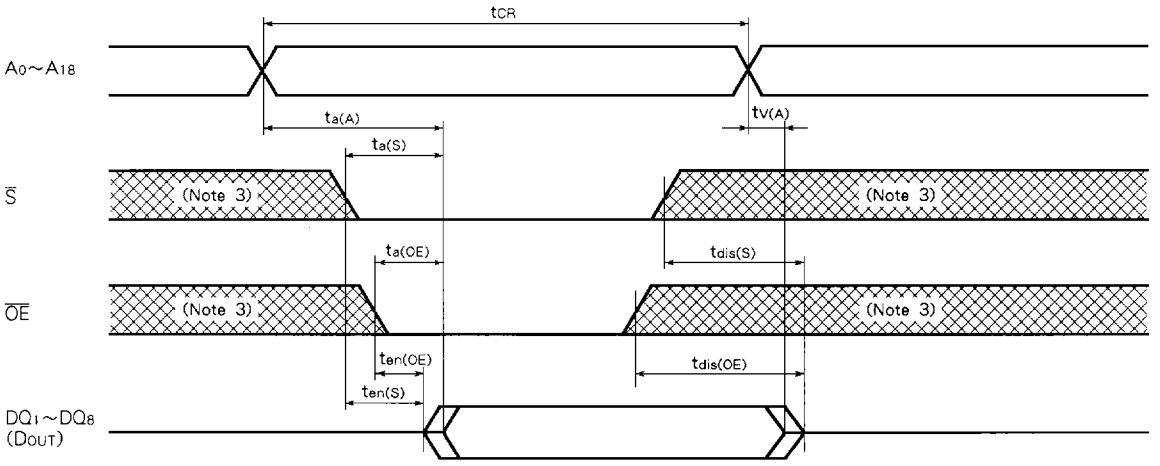
TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits										Unit
		MH5128-70		MH5128-85		MH5128-10		MH5128-12		MH5128-15		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		150		ns
$t_{w(W)}$	Write pulse width	45		55		65		75		85		ns
$t_{su(A)}$	Address set up time	0		0		0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address set up time with respect to $\overline{W}$ high	50		65		75		85		100		ns
$t_{su(S)}$	Chip select set up time	65		80		90		100		115		ns
$t_{su(D)}$	Data set up time	50		30		35		40		45		ns
$t_{h(D)}$	Data hold time	0		0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		20		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		30		35		40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		5		5		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		5		ns

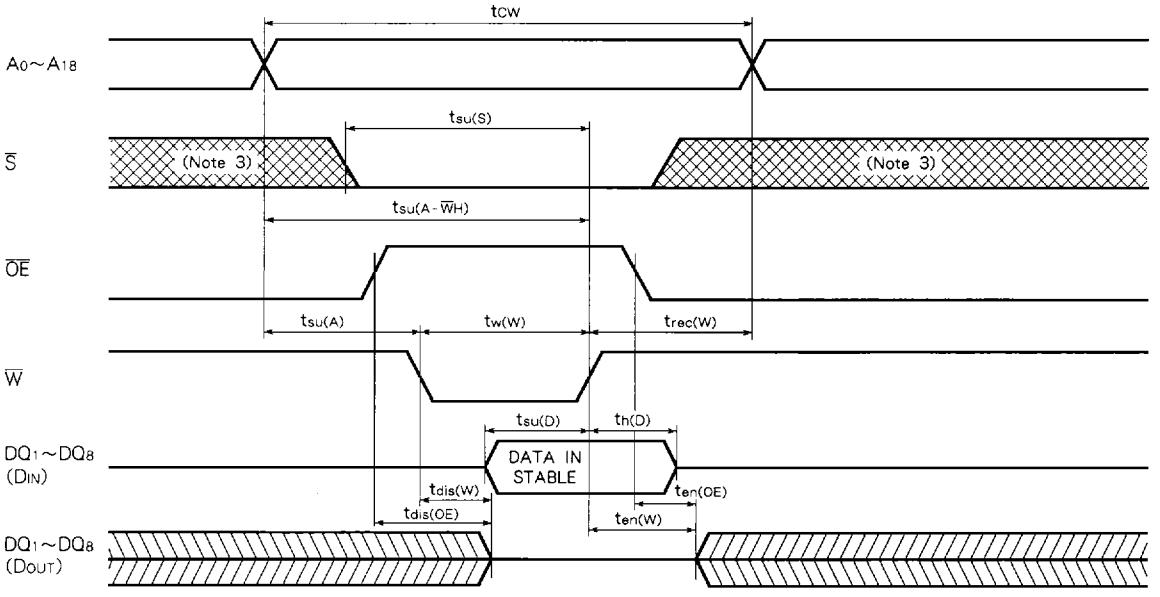
TIMING DIAGRM

Read cycle

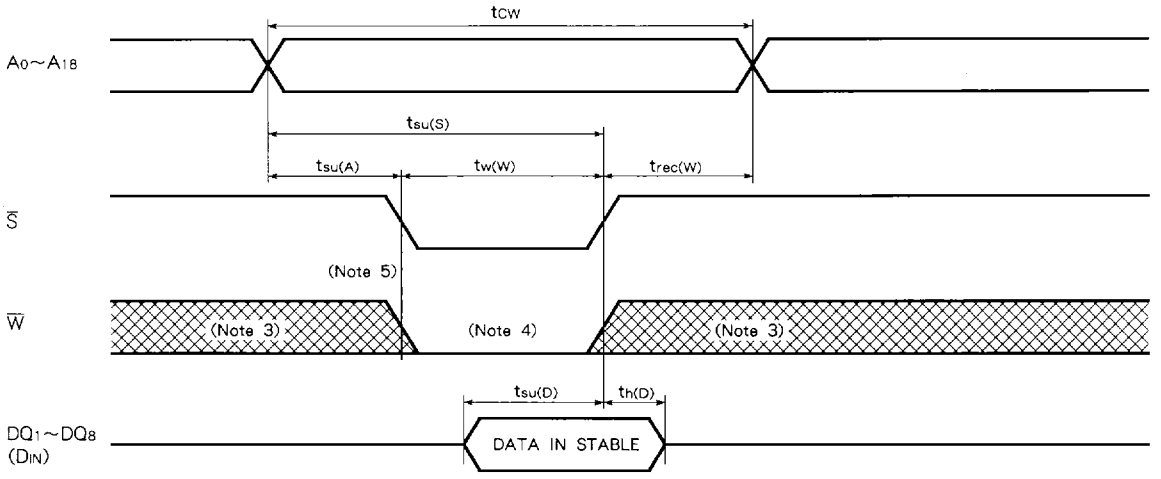


W = "H" level

Write cycle (W control)



Write cycle ($\overline{S}$ control)



Note 3. Hatching indicates the state is don't care.
4. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
5. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
6. Don't active inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, $\overline{S}$ ≧ V_{CC} − 0.2V, A_{17}~A_{18} = V_{CC} or GND Other inputs = 0~V_{CC}	ABNA-L			250	μA
			ABNA-H			90 (Note 7)	

Note 7. $I_{CC(PD)}$ = 20 μA at T_a = 25℃.
* When $\overline{S}$ is at 2.2V(V_{IH} min) and supply voltage is at any level between 4.5V and 2.4V, supply current is defined as I_{CC4}.

TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS