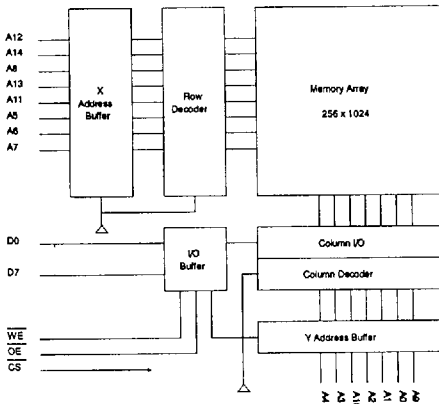


MONOLITHIC  
MEMORIES

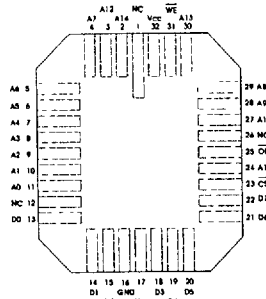
### Features

- Full military temperature range
- Very fast access times - 15/20/25ns
- Single 5V power supply
- Low power consumption - 120mA max
- Completely static operation
- Equal access and cycle times
- Battery back-up operation
- CECC approval pending

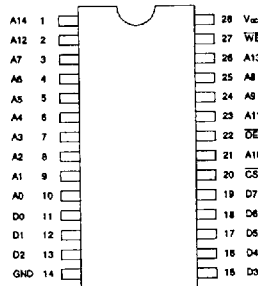
### Block Diagram



### Pin Assignments



32 pin LCC



28 pin DIL and 28 pin Flat-Pack

### Pin Functions

AO-A14	Address inputs
DO-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	Power(+5V)

### Ordering Information

MS5      832      J      BSS2 -      20

CMOS Ultra  
Fast Static  
RAM

32K X 8

Package Style

J - 28 pin 0.600 body ceramic DIL  
 SJ - 28 pin, 0.300 body ceramic DIL  
 W - 32 pin ceramic LCC  
 F - 28 pin ceramic Flat-Pack

Released to  
BBS9400

(Blank = Screened  
 in accordance with  
 MS8 Module Flow)

Speed:

-15ns  
 -20ns  
 -25ns



## 262,144 bit Ultra Fast CMOS Static RAM

Recommended DC Operating Conditions  
( $T_a = -55$  to  $+125^\circ\text{C}$ )

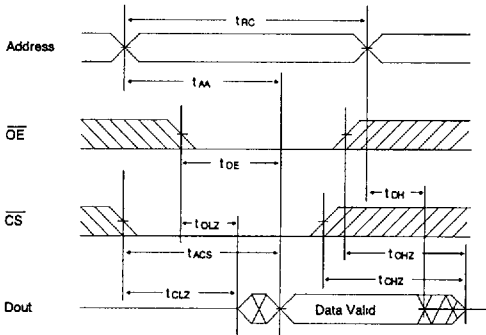
Item	Symbol	min.	typ.	max.	Unit	
Supply Voltage	-15	$V_{CC}$	4.75	5.0	5.25	V
	-20/25		4.5	5.0	5.5	
Input High Voltage	$V_{IH}$	2.2	-	$V_{CC} + 0.3$	V	
Input Low Voltage	$V_{IL}$	-0.3*	-	0.8	V	

\*  $V_{IL} = -3.0\text{V}$  Min. for pulse width less than 20ns

### Read Cycle (All units in ns)

Item	Symbol	-15		-20		-25	
		min.	max.	min.	max.	min.	max.
Read Cycle Time	$t_{RC}$	15	-	20	-	25	-
Address Access Time	$t_{AA}$	-	15	-	20	-	25
Chip Select Access Time	$t_{ACS}$	-	15	-	20	-	25
Output Enable to Output Valid	$t_{OE}$	-	8	-	10	-	12
Output Hold from Address Change	$t_{OH}$	5	-	5	-	5	-
Chip Selection to Output Low Z	$t_{CLZ}$	3	-	3	-	3	-
Output Enable to Output in Low Z	$t_{OLZ}$	2	-	2	-	2	-
Chip Deselection to Output in High Z	$t_{CHZ}$	-	8	-	9	-	10
Output Disable to Output in High Z	$t_{OHZ}$	-	7	-	8	-	9

### Timing Waveform of Read Cycle



### DC and Operating Characteristics

( $V_{CC} = 5\text{V} \pm 10\%$ ,  $GND = 0\text{V}$ ,  $T_a = -55$  to  $+125^\circ\text{C}$ )

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	$ I_{II} $	$V_{IN} = GND$ to $V_{CC}$	-1	-	1	$\mu\text{A}$
Output Leakage Current	$ I_{LO} $	$CS = V_{IH}$ or $OE = V_{IH}$ , $V_{ILO} = GND$ to $V_{CC}$	-1	-	1	$\mu\text{A}$
Operating Power Supply Current	$I_{CC1}$	$CS = V_{IL}$ , $I_{IO} = 0\text{mA}$	-	30	80	$\text{mA}$
Average Operating Supply Current	$I_{CC2}$	Min. Cycle, duty = 100%, $I_{IO} = 0\text{mA}$	-15	100	130	$\text{mA}$
			-20	85	120	
			-25	75	120	
Standby Power Supply Current	$I_{SB1}$	$CS \pm V_{CC} - 0.2\text{V}$	-	-	1	$\text{mA}$
	$I_{SB2}$	$CS = V_{IH}$	-	15	25	$\text{mA}$
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 8.0\text{mA}$	-	-	0.4	V
High Level Output Voltage	$V_{OH}$	$I_{OH} = -4.0\text{mA}$	2.4	-	-	V

MONOLITHIC MEMORIES

### Category S2 Screening Level B

PRE CAP INSPECTION  
BS9400 1.2.10 LEVEL B

HIGH TEMPERATURE STORAGE  
BS9400 1.2.6.3  
150°C For 24 Hours

RAPID CHANGE OF TEMPERATURE  
BS9400 1.2.6.13  
10 CYCLES -65°C TO +150°C

ACCELERATION STEADY STATE  
BS9400 1.2.6.9  
294000m/s<sup>2</sup> Direction Y1 \*

ELECTRICAL TESTS AT 25°C

BURN-IN SCREEN  
BS9400 1.2.9.2 160 Hours min at 125°C

FINAL ELECTRICAL TESTS,  
STATIC & DYNAMIC,  
AT 25°C, 125°C & -55°C

FINE AND GROSS LEAK TESTS  
BS9400 1.2.6.14

SAMPLE TESTS to Groups A,B,C  
as appropriate

\* Direction Y1 is the direction which tends to separate the bonds

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