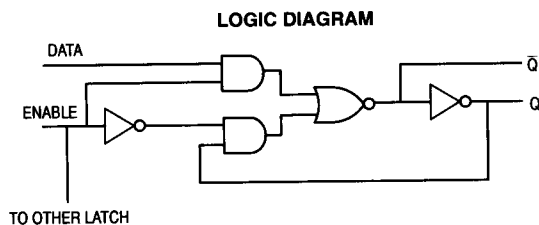




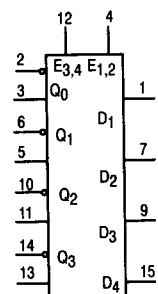
4-Bit Bistable Latch

ELECTRICALLY TESTED PER:
MIL-M-38510/31604

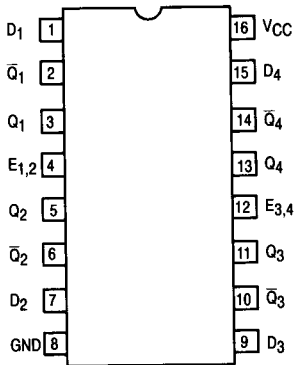
The 54LS375 is a 4-bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its setup time will be retained at the Q outputs.



LOGIC SYMBOL



CONNECTION DIAGRAM



Pin Names	Loading (Note a)	
	HIGH	LOW
D ₁ -D ₂ Data Inputs	0.5 U.L.	0.25 U.L.
E ₀ -E ₁ Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E ₂ -E ₃ Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q ₁ -Q ₄ Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
Q ₁ -Q ₄ Complementary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

- a. One TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for commercial (74) Temperature Ranges.

Military 54LS375



AVAILABLE AS:

- 1) JAN: JM38510/31604BXA
- 2) SMD: N/A
- 3) 883: 54LS375/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
D ₁	1	1	2	VCC
Q ₁ -bar	2	2	3	OPEN
Q ₁	3	3	4	VCC
E ₁ -E ₂	4	4	5	VCC
Q ₂	5	5	7	VCC
Q ₂ -bar	6	6	8	OPEN
D ₂	7	7	9	VCC
GND	8	8	10	GND
D ₃	9	9	12	VCC
Q ₃ -bar	10	10	13	OPEN
Q ₃	11	11	14	VCC
E ₃ -E ₄	12	12	15	VCC
Q ₄	13	13	17	VCC
Q ₄ -bar	14	14	18	OPEN
D ₄	15	15	19	VCC
VCC	16	16	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE (Each Latch)

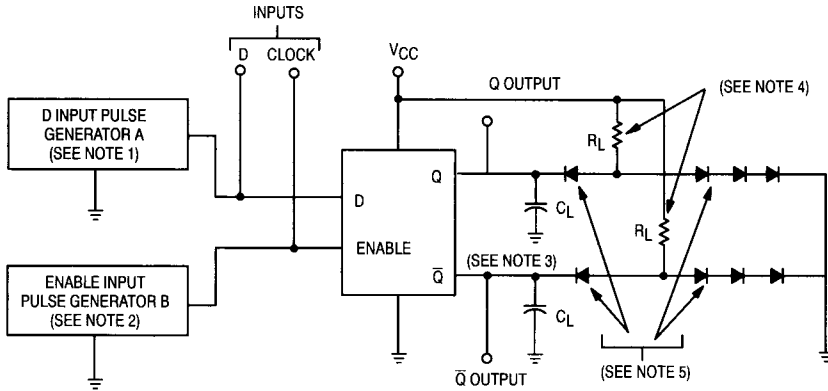
t _n	t _n + 1
D	Q
H	H
L	L

t_n = Bit time before enable negative-going transition
t_n + 1 = Bit time after enable negative-going transition.

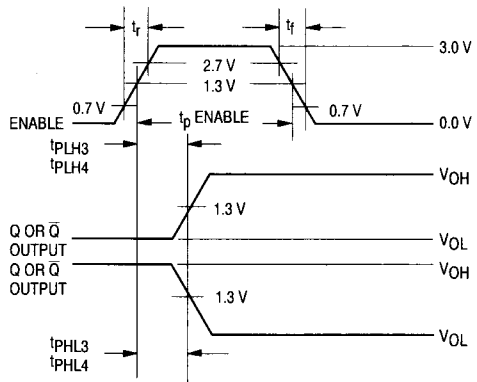
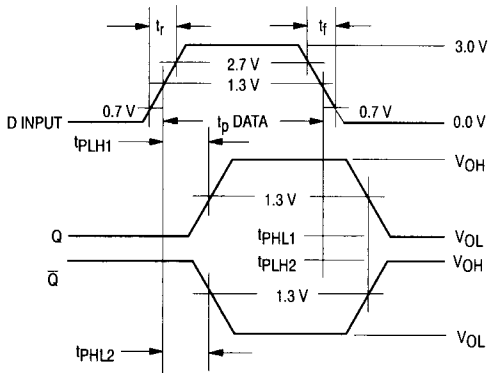
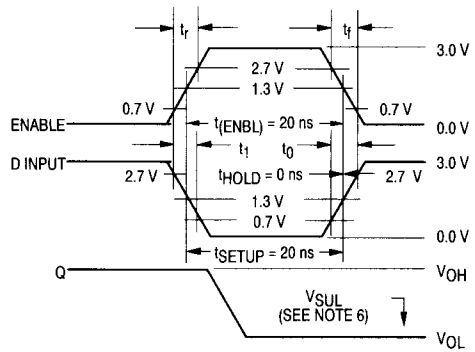
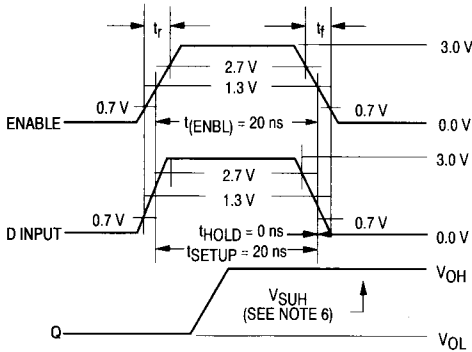


54LS375

SWITCHING TEST CIRCUIT



SETUP AND HOLD WAVEFORMS



REFERENCE NOTES ON PAGE 5-394

54LS375

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = - 0.4 mA, V _{IH} = 2.0 V or 0.7 V per truth table, Enable = (See Note 7).
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V or 2.0 V per truth table, Enable = (See Note 7).
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current (D inputs)		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other input is open.
I _{IHH}	Logical "1" Input Current (E _n inputs)		80		80		80	μA	V _{CC} = 5.5 V, V _{IH} = GND, V _{IN} (E _n) = 2.7 V.
I _{IH}	Logical "1" Input Current (D inputs)		100		100		100	μA	V _{CC} = 5.5 V, V _{IH} = 5.5 V, V _{IN} (E _n) = GND.
I _{IHH}	Logical "1" Input Current (E _n inputs)		400		400		400	μA	V _{CC} = 5.5 V, V _{IH} = GND, V _{IN} (E _n) = 5.5 V.
I _{IL}	Logical "0" Input Current (D inputs)	- 0.16	- 0.4	- 0.16	- 0.4	- 0.16	- 0.4	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, V _{IN} (E _n) = 4.5 V.
I _{IL}	Logical "0" Input Current (E _n inputs)	- 0.64	- 1.6	- 0.64	- 1.6	- 0.64	- 1.6	mA	V _{CC} = 5.5 V, V _{IN} (E _n) = 0.4 V, other input = 4.5 V.
I _{OS}	Output Short Circuit Current	- 15	- 100	- 15	- 100	- 15	- 100	mA	V _{CC} = 5.5 V, V _{IN} (E _n) = 4.5 V, other input = GND.
I _{CC}	Power Supply Current		12		12		12	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

54LS375

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay Data-Output Data to Q	3.0 —	22 17	3.0 —	29 24	3.0 —	29 24	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH1} t _{PLH1}	Propagation Delay Data-Output Data to Q	3.0 —	32 27	3.0 —	42 37	3.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PHL2} t _{PHL2}	Propagation Delay Data-Output Data to Q	3.0 —	20 15	3.0 —	26 21	3.0 —	26 21	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH2} t _{PLH2}	Propagation Delay Data-Output Data to Q̄	3.0 —	25 20	3.0 —	32 27	3.0 —	32 27	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PHL3} t _{PHL3}	Propagation Delay Data-Output Enable to Q	3.0 —	30 25	3.0 —	39 34	3.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH3} t _{PLH3}	Propagation Delay Data-Output Enable to Q	3.0 —	32 27	3.0 —	42 37	3.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PHL4} t _{PHL4}	Propagation Delay Data-Output Enable to Q̄	3.0 —	20 15	3.0 —	26 21	3.0 —	26 21	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH4} t _{PLH4}	Propagation Delay Data-Output Enable to Q	3.0 —	35 30	3.0 —	46 41	3.0 —	46 41	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
V _{SUH}	Logical "1" Setup Voltage	2.5		2.5		2.5		V	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.
V _{SUL}	Logical "0" Setup Voltage		0.4		0.4		0.4	V	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.

NOTES:

- The D input pulse generator has the following characteristics: V_{GEN} = 3.0 V, t_r ≤ 15 ns, t_f ≤ 6.0 ns, t_p = 30 ns and Z_{OUT} = 50 Ω except when measuring V_{SETUP}.
- The enable pulse generator is identical to the D input pulse generator.
- C_L = 50 pF ± 10%, which includes probe and jig capacitance.
- R_L = 2.0 kΩ ± 5%.
- All diodes are 1N3064 or equivalent.
- V_{SETUP} is to be measured 500 ns minimum after input transition to assure that the device has latched with minimum setup and maximum hold conditions applied to inputs.
- Apply 0.0 V/3.0 V – 5.0 V/0.0 V momentary pulse 500 ns minimum prior to making test.
- For all t_{PLH} and V_{SUH} tests, preset output into the ZERO states prior to making test.
- For all t_{PHL} and V_{SUL} tests, preset output into ONE states prior to making test.
- The limits specified for C_L = 15 pF are guaranteed but not tested.