

100331

Low Power Triple D Flip-Flop

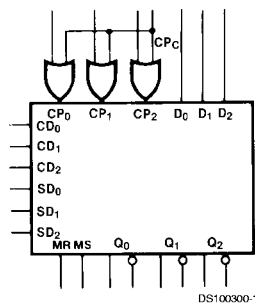
General Description

The 100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 k Ω pull-down resistors.

Features

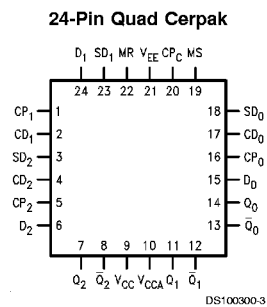
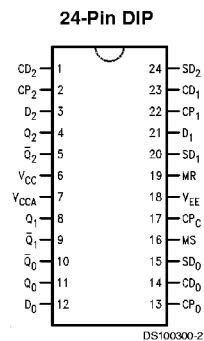
- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to Standard Microcircuit Drawing (SMD) 5962-9153601

Logic Symbol

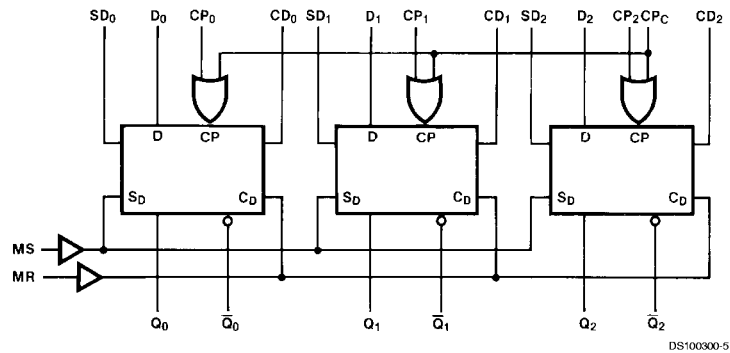


Pin Names	Description
CP_0 - CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0 - D_2	Data Inputs
CD_0 - CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0 - Q_2	Data Outputs
\bar{Q}_0 - \bar{Q}_2	Complementary Data Outputs

Connection Diagrams



Logic Diagram



Truth Tables

Synchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D_n	CP_n	CP_c	MS SD_n	MR CD_n	$Q_n(t + 1)$
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	L	L	L	L	$Q_n(t)$
X	H	X	L	L	$Q_n(t)$
X	X	H	L	L	$Q_n(t)$

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 U = Undefined
 t = Time before CP Positive Transition
 t + 1 = Time after CP Positive Transition
 ↗ = LOW to HIGH Transition

Asynchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D_n	CP_n	CP_c	MS SD_n	MR CD_n	$Q_n(t + 1)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Pin Potential to	
Ground Pin (V_{EE})	-7.0V to +0.5V

Input Voltage (DC)	V_{EE} to +0.5V
Output Current	
(DC Output HIGH)	-50 mA
ESD (Note 2)	≤ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	-55°C to +125°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55°C$ to $+125°C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085	-870	mV	-55°C			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C			
		-1830	-1555	mV	-55°C			
V_{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085		mV	-55°C			
V_{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C			
			-1555	mV	-55°C			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for all Inputs	(Notes 3, 4, 5, 6)	
V_{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for all Inputs	(Notes 3, 4, 5, 6)	
I_{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)	(Notes 3, 4, 5)	
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	(Notes 3, 4, 5)	
			340	μA	-55°C			
I_{EE}	Power Supply Current	-130	-50	mA	-55°C to +125°C	Inputs Open	(Notes 3, 4, 5)	

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7 and 8.

Note 5: Sampled tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	400		400		400		MHz	Figures 2, 3	(Note 10)
t_{PLH} t_{PHL}	Propagation Delay CP _C to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	Figures 1, 3	(Notes 7, 8, 9)
t_{PLH} t_{PHL}	Propagation Delay CP _n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns		
t_{PLH} t_{PHL}	Propagation Delay CD _n , SD _n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	CP _n , CP _C = L Figures 1, 4	
t_{PLH} t_{PHL}		0.50	2.40	0.60	2.10	0.50	2.50			
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	0.70	2.70	0.80	2.60	0.80	2.90	ns	CP _n , CP _C = L	
t_{PLH} t_{PHL}		0.70	2.90	0.80	2.80	0.80	3.10		CP _n , CP _C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.20	1.40	0.20	1.40	ns	Figures 1, 3, 4	
t_s	Setup Time								Figure 5	(Note 10)
	D _n	1.00		0.80		0.90		ns	Figure 4	
	CD _n , SD _n (Release Time) MS, MR (Release Time)	1.50		1.30		1.60				
t_h	Hold Time D _n	1.50		1.30		1.60		ns	Figure 5	
$t_{pw(H)}$	Pulse Width HIGH CP _n , CP _C , CD _n , SD _n , MR, MS	2.00		2.00		2.00		ns	Figures 3, 4	

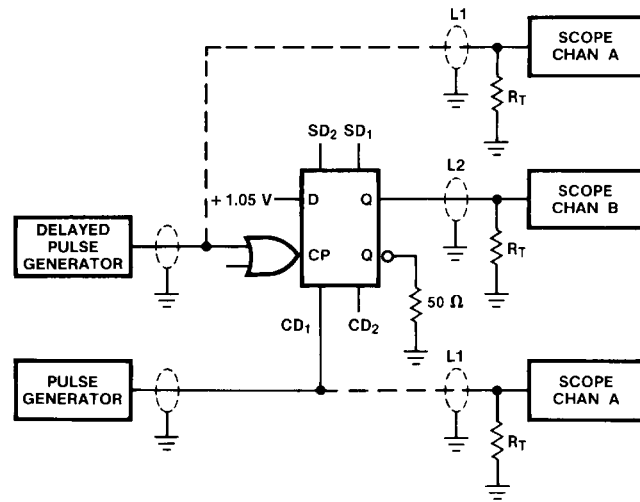
Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $+25^\circ C$. Temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each Mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$, and $-55^\circ C$ Temp., Subgroups A10 and A11.

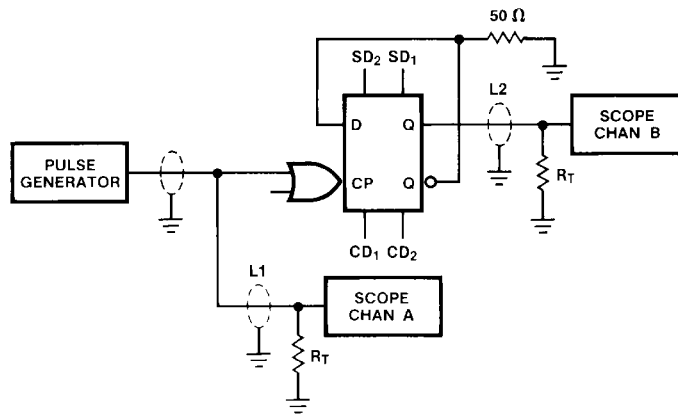
Note 10: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ Temperature (design characterization data).

Test Circuits



DS100300-6

FIGURE 1. AC Test Circuit



DS100300-7

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = Equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 2. Toggle Frequency Test Circuit

Switching Waveforms

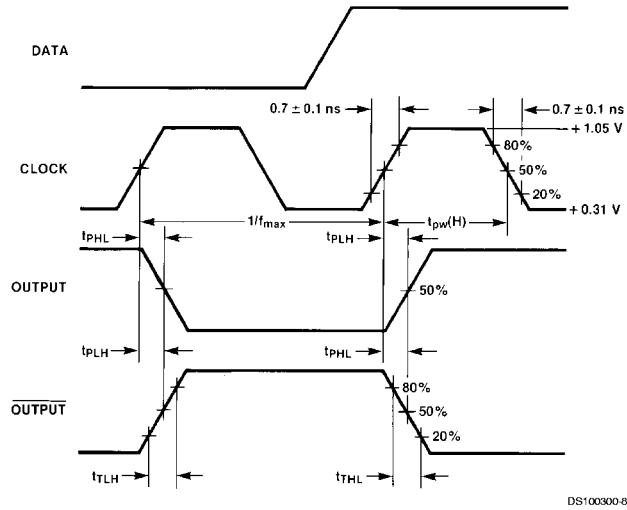


FIGURE 3. Propagation Delay (Clock) and Transition Times

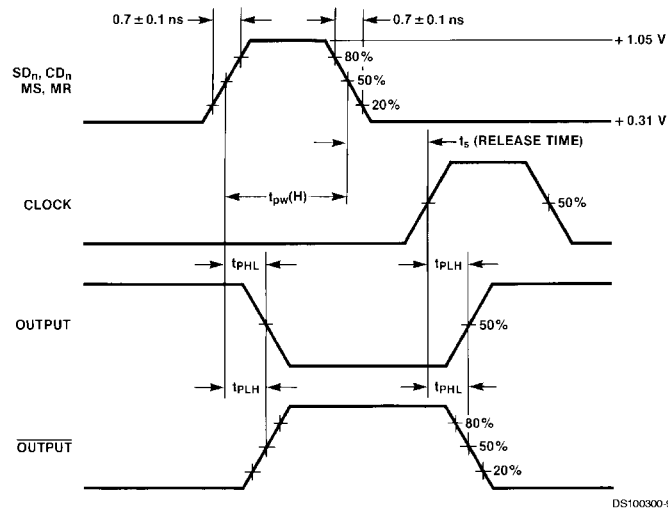


FIGURE 4. Propagation Delay (Resets)

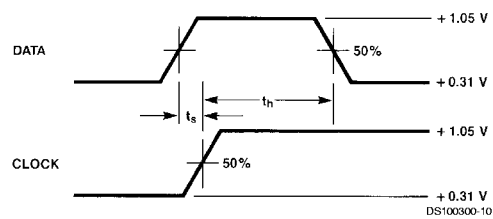
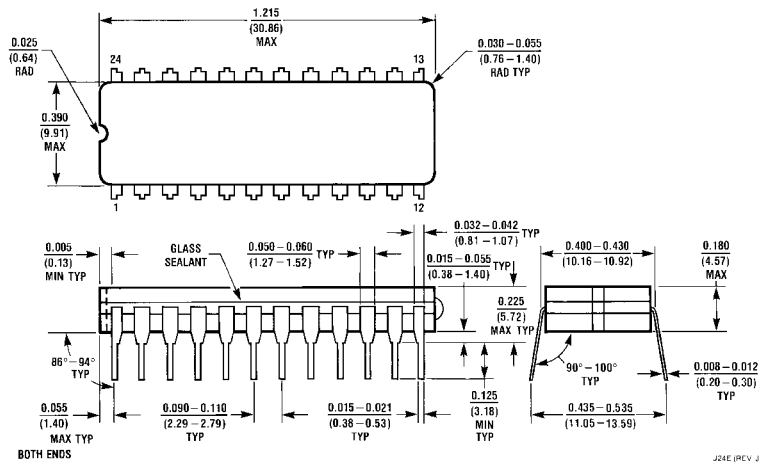


FIGURE 5. Data Setup and Hold Time

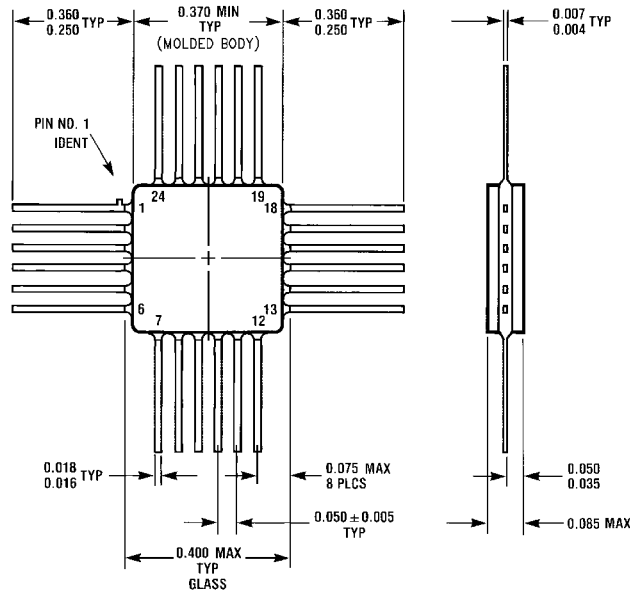
Note 11: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note 12: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B