CMOS Dual 8-Bit Buffered Multiplying DAC

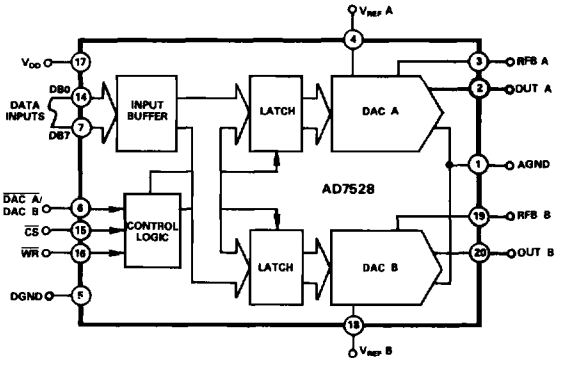
AD7528

FEATURES
- On-Chip Latches for Both DACs
- +5V to +15V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible
- Latch Free (Protection Schottkys not Required)

APPLICATIONS

Digital Control of:
- Gain/Attenuation
- Filter Parameters
- Stereo Audio Circuits
- X–Y Graphics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin DIP, SOIC, PLCC or LCCC.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7528—SPECIFICATIONS (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±½	±½	±½	±½	LSB max	
	L, C, U	±½	±½	±½	±½	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111.
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient[4]							
ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage							
V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage							
V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current							
I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time							
t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time							
t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time							
t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time							
t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time							
t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time							
t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2LSB. Out A/Out B load = 100Ω. $\overline{WR}$ = $\overline{CS}$ = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10V OUT A, OUT B Load = 100Ω C_{EXT} = 13pF $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL TO ANALOG GLITCH IMPULSE	All	160	–	440	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT} A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT} B		50	50	50	50	pF max	
C_{OUT} A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT} B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	@ 100kHz
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} B = 0V see Figure 6.
V_{REF} B to OUT A		−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} A = 0V see Figure 6.
DIGITAL CROSSTALK	All	30	–	60	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	−85	–	−85	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES
[1]Temperature Ranges are J, K, L Versions: −40°C to +85°C
A, B, C Versions: −40°C to +85°C
S, T, U Versions: −55°C to +125°C
[2]Specification applies to both DACs in AD7528.
[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.
[4]Guaranteed by design but not production tested.
[5]These characteristics are for design guidance only and are not subject to test.
[6]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, L) Grades	−40°C to +85°C
Industrial (A, B, C) Grades	−40°C to +85°C
Extended (S, T, U) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7528, ideal maximum output is V_{REF} − 1LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

Digital to Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Propagation Delay:
This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

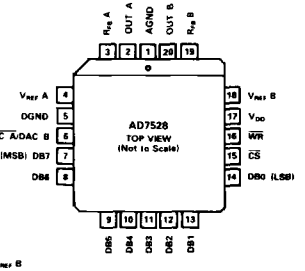
ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7528JN	−40°C to +85°C	±1LSB	±4LSB	N-20
AD7528KN	−40°C to +85°C	±1/2LSB	±2LSB	N-20
AD7528LN	−40°C to +85°C	±1/2LSB	±1LSB	N-20
AD7528JP	−40°C to +85°C	±1LSB	±4LSB	P-20A
AD7528KP	−40°C to +85°C	±1/2LSB	±2LSB	P-20A
AD7528LP	−40°C to +85°C	±1/2LSB	±1LSB	P-20A
AD7528JR	−40°C to +85°C	±1LSB	±4LSB	R-20
AD7528KR	−40°C to +85°C	±1/2LSB	±2LSB	R-20
AD7528LR	−40°C to +85°C	±1/2LSB	±1LSB	R-20
AD7528AQ	−40°C to +85°C	±1LSB	±4LSB	Q-20
AD7528BQ	−40°C to +85°C	±1/2LSB	±2LSB	Q-20
AD7528CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-20
AD7528SQ	−55°C to +125°C	±1LSB	±4LSB	Q-20
AD7528TQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-20
AD7528UQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-20
AD7528SE	−55°C to +125°C	±1LSB	±4LSB	E-20A
AD7528TE	−55°C to +125°C	±1/2LSB	±2LSB	E-20A
AD7528UE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A

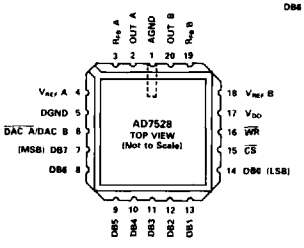
NOTES
[1]Analog Devices reserves the right to ship side-brazed ceramic in lieu of cerdip. Parts will be marked with cerdip designator "Q."
[2]Processing to MIL-STD-883C, Class B is available. To order, add suffix "/883B" to part number. For further information, see Analog Devices' 1990 Military Products Databook.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

PIN CONFIGURATIONS

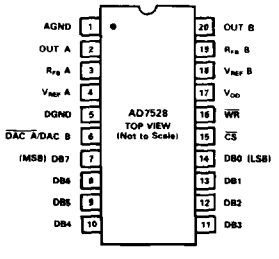
PLCC



LCCC



DIP, SOIC



INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{DAC\ A}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

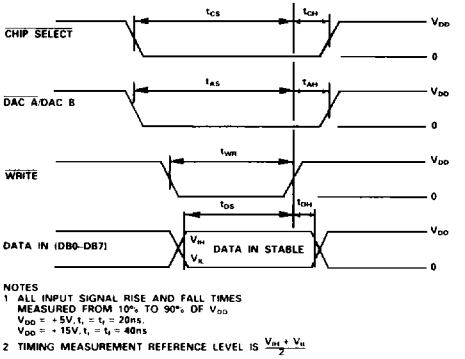
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{DAC\ A}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



CIRCUIT INFORMATION–D/A SECTION

The AD7528 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

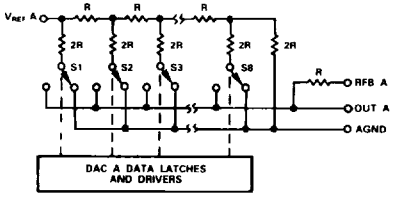


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. g(V_{REF} A, N) is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

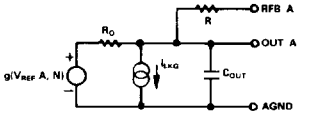


Figure 2. Equivalent Analog Output Circuit of DAC A

For further information on CMOS multiplying D/A converters refer to "Appplication Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

CIRCUIT INFORMATION–DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the AD7528 is operated with V_{DD} = 5V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7528 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

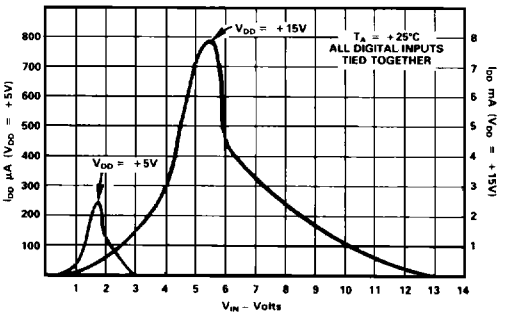


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V