



MOTOROLA

MC14028B

**BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER**

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or read-out decoding.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

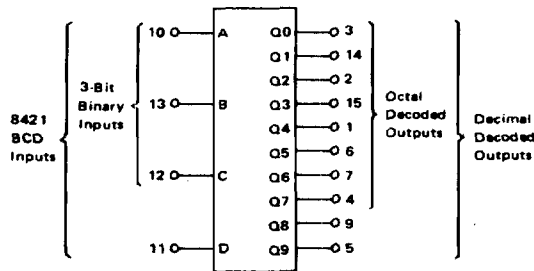
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	- 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" Package: - 12mW/°C from 65°C to 85°C

Ceramic "L" Package: - 12mW/°C from 100°C to 125°C

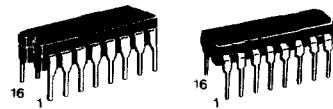
BLOCK DIAGRAM



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

**BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER**



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: - 55°C to + 125°C
MC14XXXBAL (Ceramic Package Only)

C Series: - 40°C to + 85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
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1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current (AL Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
		15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current (CL/CP Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-2.5	—	-2.1	-4.2	—	-1.7	—	mAdc
		10	-0.52	—	-0.44	-0.88	—	-0.36	—	
		15	-1.3	—	-1.1	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.52	—	0.44	0.88	—	0.36	—	mAdc
		10	1.3	—	1.1	2.25	—	0.9	—	
		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current (AL Device)	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Current (CL/CP Device)	I _{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current (CL/CP Device) (Per Package)	I _{DD}	5.0	—	20	—	0.005	20	—	150	μAdc
		10	—	40	—	0.010	40	—	300	
		15	—	80	—	0.015	80	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.3 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (0.6 μA/kHz) f + I _{DD}							
		15	I _T = (0.9 μA/kHz) f + I _{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

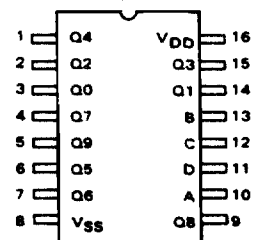
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001

**The formulas given are for the typical characteristics only at 25°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

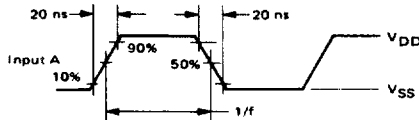
Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns	5.0	—	100	200	ns
	t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns	10	—	50	100	
	t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	15	—	40	80	
Propagation Delay Time	t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 215 ns	5.0	—	300	600	ns
	t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 97 ns	10	—	130	260	
	t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 65 ns	15	—	90	180	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

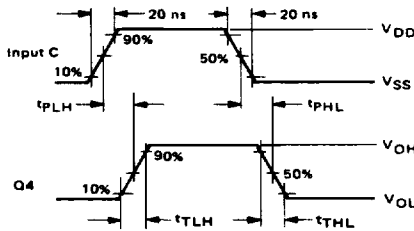
FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

Inputs B, C, and D switching in respect to a BCD code.



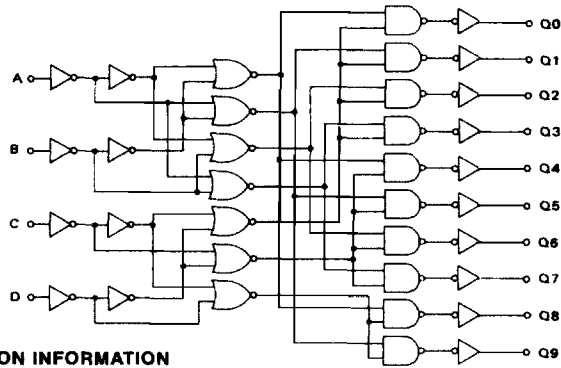
All outputs connected to respective C_L loads. f in respect to a system clock.

Inputs A, B, and D low.



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LOGIC DIAGRAM

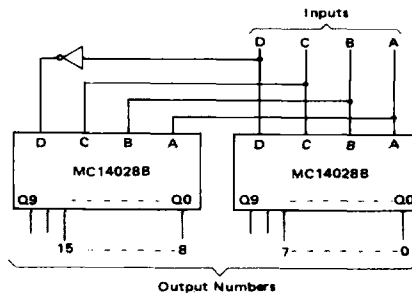


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 - CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS				OUTPUT NUMBERS																CODE AND REDEFINED OUTPUT NUMBERS					
																				Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	5	6	2		3	4
0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	8	15	5			8
1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	9	14	6			9
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	10	12	7			10
1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	11	13	8			11
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

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FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

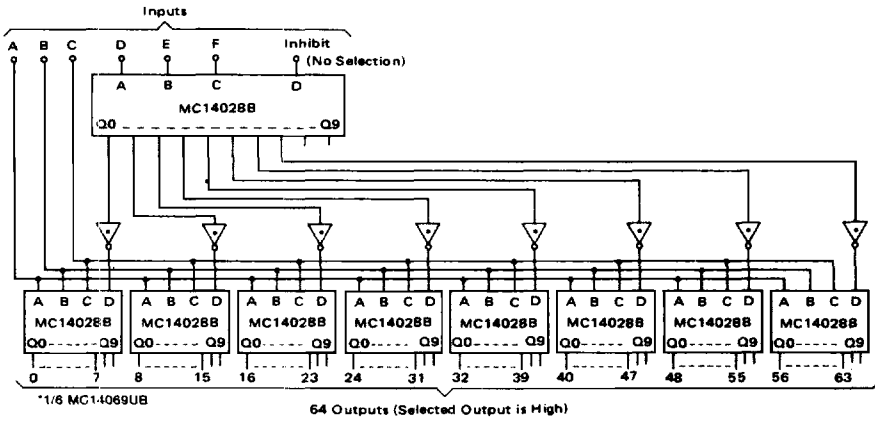


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION

