HARRIS SEMICONDUCTOR

CA3290

BiMOS Dual Voltage Comparator with MOSFET Input, Bipolar Output

March 1993

Features

- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}).....1.7TΩ (Typ.)
  - Very Low Input Current at V+ = 5V .....3.5pA (Typ.)
  - Wide Common Mode Input Voltage Range (V_{ICR}) can be swung 1.5V (Typ.) Below Negative Supply Voltage Rail
  - Virtually Eliminates Errors Due to Flow of Input Currents
- Output Voltage Compatible with TTL, DTL, ECL, MOS, and CMOS Logic Systems in Most Applications

Applications

- High Source Impedance Voltage Comparators
- Long Time Delay Circuits
- Square Wave Generators
- A/D Converters
- Window Comparators

Description

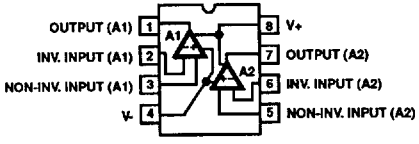
The CA3290A and CA3290 types consist of a dual voltage comparator on a single monolithic chip. The common mode input voltage range includes ground even when operated from a single supply. The low supply current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

Ordering Information

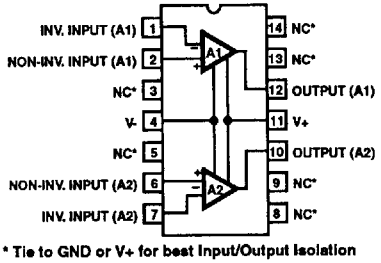
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3290AE	-55°C to +125°C	8 Lead Plastic DIP
CA3290AE1	-55°C to +125°C	14 Lead Plastic DIP
CA3290AT	-55°C to +125°C	8 Pin TO-5 Can
CA3290BT	-55°C to +125°C	8 Pin TO-5 Can
CA3290E	-55°C to +125°C	8 Lead Plastic DIP
CA3290E1	-55°C to +125°C	14 Lead Plastic DIP
CA3290T	-55°C to +125°C	8 Pin TO-5 Can

Pinouts

CA3290/A (PDIP)
TOP VIEW

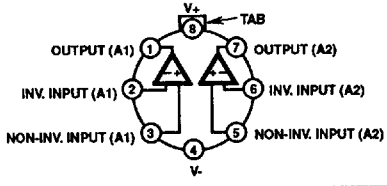


CA3290A, CA3290 (PDIP)
TOP VIEW



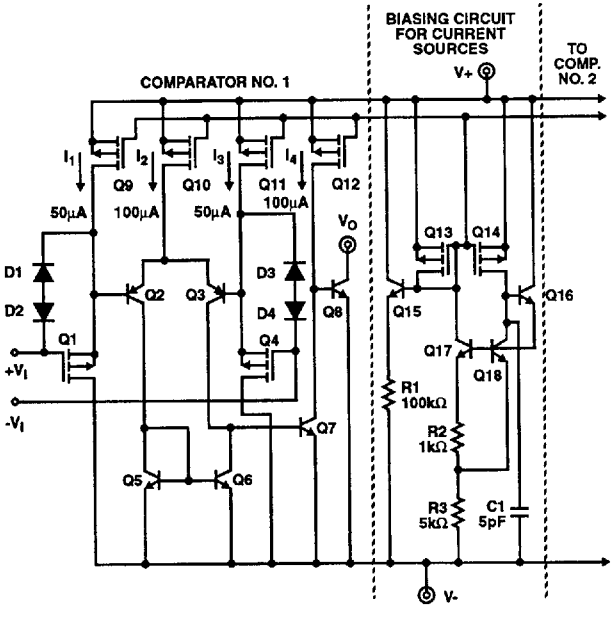
* Tie to GND or V+ for best Input/Output Isolation

CA3290A, CA3290, CA3290B (TO-5 CAN)
TOP VIEW



Schematic Diagram

(ONLY ONE IS SHOWN)



File Number 1049.1

Specifications CA3290, CA3290A

Absolute Maximum Ratings

Supply Voltage
- Single Supply ..... +36V
- Dual Supply ..... ±18V

Differential Input Voltage ..... 36V or [(V+ - V-) +5V] (whichever is less)
DC Input Voltage ..... V+ +5V to V- -5V
Output to V- Short Circuit Duration (Note 1) ..... Continuous
Input Current 1mA
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range ..... $-55°C \le T_A \le +125°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
8 Lead Plastic DIP Package	94	32
14 Lead Plastic DIP Package	107	38
TO-5 Can Package	114	35

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3290A			CA3290			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	T_A = -55°C to +125°C, $V_{CM} = V_O$ = 1.4V, V+ = 5V	-	4.5	-	-	8.5	-	mV
		T_A = -55°C to +125°C, $V_{CM} = V_O$ = 0V, V+ = +15V, V- = -15V	-	8.5	-	-	8.5	-	mV
		T_A = +25°C, $V_{CM} = V_O$ = 1.4V, V+ = 5V	-	4.0	10	-	7.5	20	mV
		T_A = +25°C, $V_{CM} = V_O$ = 0V, V+ = +15V, V- = -15V	-	4.0	10	-	7.5	20	mV
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$		-	8	-	-	8	-	µV/°C
Input Offset Current	I_{IO}	T_A = -55°C to +125°C, V_{CM} = 1.4V, V+ = 5V	-	2	28	-	2	32	nA
		T_A = -55°C to +125°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	7	28	-	7	32	nA
		T_A = +25°C, V_{CM} = 1.4V, V+ = 5V	-	2	25	-	2	30	pA
		T_A = +25°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	7	25	-	7	30	pA
Input Current	I_I	T_A = +125°C, V_{CM} = 1.4V, V+ = 5V	-	2.8	45	-	2.8	55	nA
		T_A = +125°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	13	45	-	13	55	nA
		T_A = +25°C, V_{CM} = 1.4V, V+ = 5V	-	3.5	40	-	3.5	50	pA
		T_A = +25°C, V_{CM} = 0V, V+ = +15V, V- = -15V	-	12	40	-	12	50	pA
Supply Current	I+	T_A = -55°C, R_L = ∞, V+ = 5V	-	0.85	1.0	-	0.85	1.6	mA
		T_A = -55°C, R_L = ∞, V+ = 30V	-	1.62	3.0	-	1.62	3.5	mA
		T_A = +25°C, R_L = ∞, V+ = 5V	-	0.8	1.4	-	0.8	1.4	mA
		T_A = +25°C, R_L = ∞, V+ = 30V	-	1.35	3.0	-	1.35	3.0	mA

Electrical Specifications $V^- = 0V$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA3290A			CA3290			
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain	A_{OL}	T_A = -55°C to +125°C, R_L = 15kΩ, V+ = +15V, V- = -15V	-	150	-	-	150	-	V/mV
			-	103	-	-	103	-	dB
		T_A = +25°C, R_L = 15kΩ, V+ = +15V, V- = -15V	25	800	-	25	800	-	V/mV
			88	118	-	88	118	-	dB
Saturation Voltage	V_{SAT}	T_A = +125°C, I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-	0.22	0.7	-	0.22	0.7	V
		T_A = -55°C, I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-	0.1	-	-	0.1	-	V
		T_A = +25°C, I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-	0.12	0.4	-	0.12	0.4	V
Output Leakage Current	I_{OL}	T_A = -55°C to +125°C, V+ = 15V	-	65	-	-	65	-	nA
		T_A = -55°C to +125°C, V+ = 36V	-	130	1k	-	130	1k	nA
		T_A = +25°C, V+ = 15V	-	100	-	-	100	-	pA
		T_A = +25°C, V+ = 36V	-	500	-	-	500	-	pA
Common Mode Input Voltage Range	V_{ICR}	T_A = +25°C, V_O = 1.4V, V+ = 5V	V+-3.5 V-	V+-3.1 V- -1.5	-	V+-3.5 V-	V+-3.1 V- -1.5	-	V
		T_A = +25°C, V_O = 0V, V+ = +15V, V- = -15V	V+-3.8 V-	V+-3.4 V- -1.6	-	V+-3.8 V-	V+-3.4 V- -1.6	-	V
Common Mode Rejection Ratio	CMRR	T_A = +25°C, V+ = +15V, V- = -15V	-	44	562	-	44	562	µV/V
		T_A = +25°C, V+ = 5V	-	100	562	-	100	562	µV/V
Power Supply Rejection Ratio	PSRR	T_A = +25°C, V+ = +15V, V- = -15V	-	15	316	-	15	316	µV/V
Output Sink Current		T_A = +25°C, V_O = 1.4V, V+ = 5V	6	30	-	6	30	-	mA
Response Time Rising Edge	T_R	T_A = +25°C, R_L = 5.1kΩ, V+ = 15V	-	1.2	-	-	1.2	-	µs
Response Time Falling Edge	T_F	T_A = +25°C, R_L = 5.1kΩ, V+ = 15V	-	200	-	-	200	-	ns
Large Signal Response Time		T_A = +25°C, R_L = 5.1kΩ, V+ = 15V	-	500	-	-	500	-	ns
		T_A = +25°C, R_L = 5.1kΩ, V+ = 5V	-	400	-	-	400	-	ns

NOTE:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction of the device.

Circuit Description

The Basic Comparator

Figure 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; Transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V+.

In essence, Q1 and Q4 function as source followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q4 is established at approximately 50μA by constant current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range.

As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink current capability.

The detailed schematic diagram for one comparator and the common current source biasing is shown on the front page. PMOS transistors Q9 through Q12 are the current source elements identified in Figure 1 as I_1 through I_4, respectively. Their gate source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right hand portion of the Schematic Diagram. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

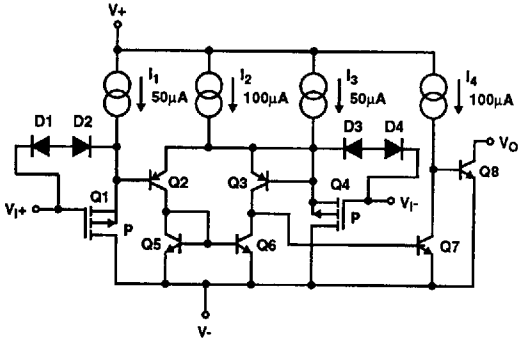
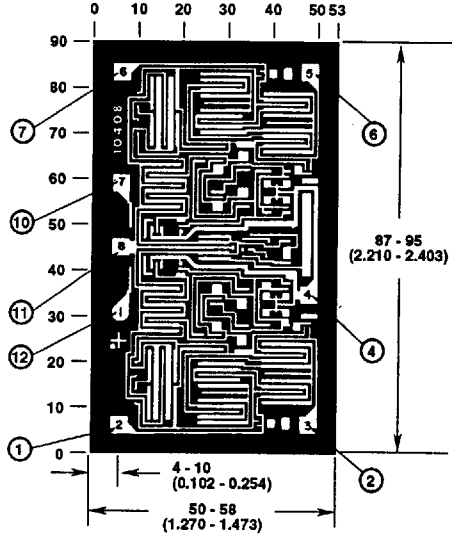


FIGURE 1. BASIC CIRCUIT DIAGRAM FOR ONE OF THE TWO COMPARATORS

Metallization Mask Layout

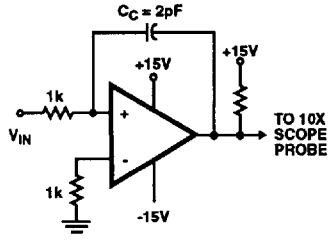


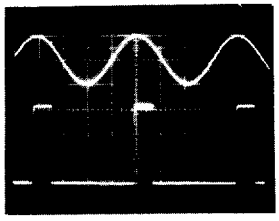
The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

NOTE: Numbers in pads are for 8 lead DIP and TO-5 Can and numbers outside of chip are for 14 lead DIP

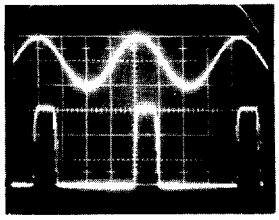
Test Circuits and Waveforms





WITH C_C

Top Trace = 4.5mV/Div = V_{IN}
Bottom Trace = 10V/Div = V_{OUT}
H = 5µs/Div



WITHOUT C_C

Top Trace = 4.5mV/Div
Bottom Trace = 10V/Div
H = 5µs/Div

FIGURE 2. PARASITIC OSCILLATIONS TEST CIRCUIT AND WAVEFORMS

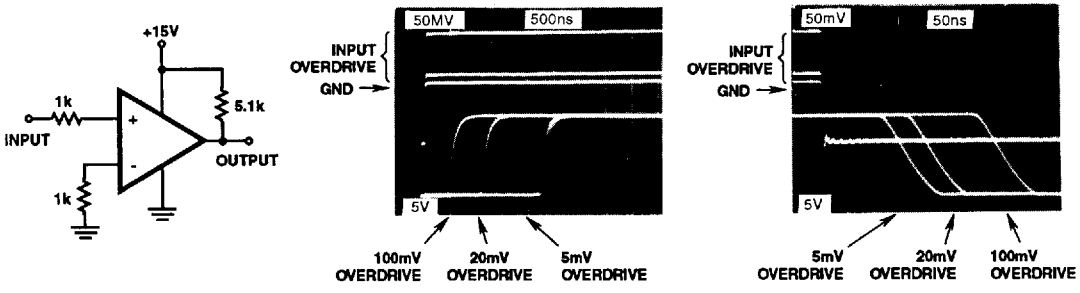


FIGURE 3. NON-INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS

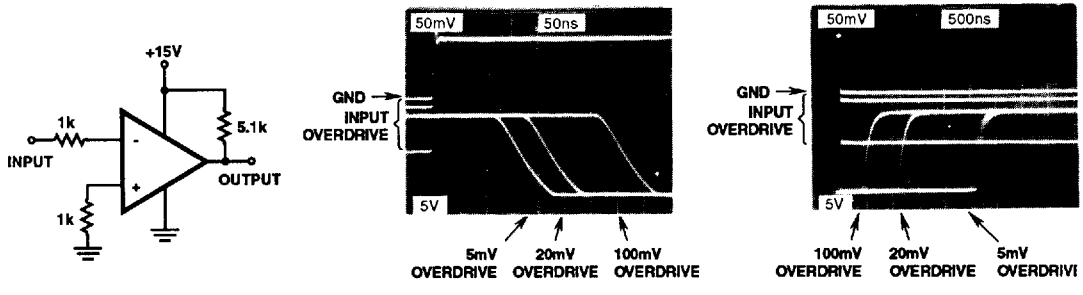


FIGURE 4. INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS

Typical Performance Curves

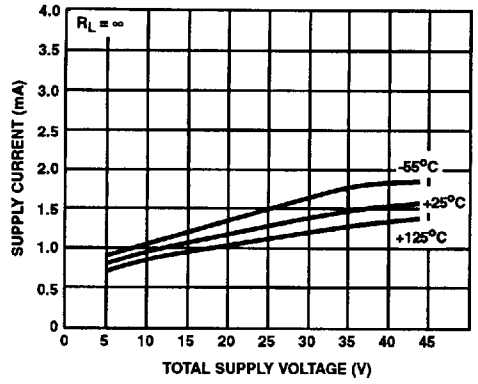


FIGURE 5. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE (BOTH AMPLIFIERS)

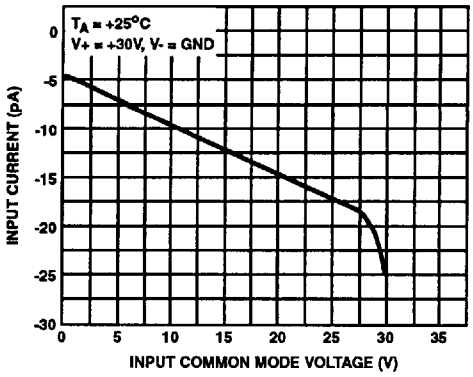


FIGURE 6. INPUT CURRENT AS A FUNCTION OF INPUT COMMON MODE VOLTAGE

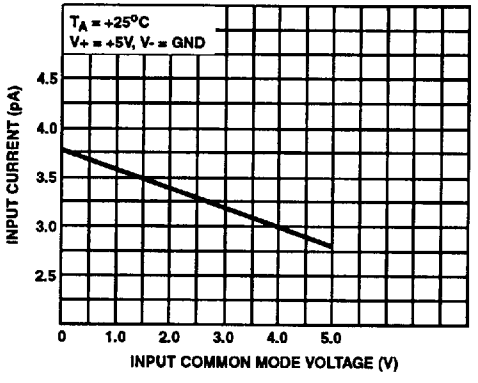


FIGURE 7. INPUT CURRENT AS A FUNCTION OF INPUT COMMON MODE VOLTAGE

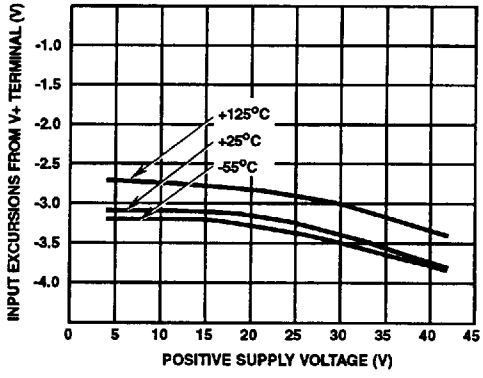


FIGURE 8. POSITIVE COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

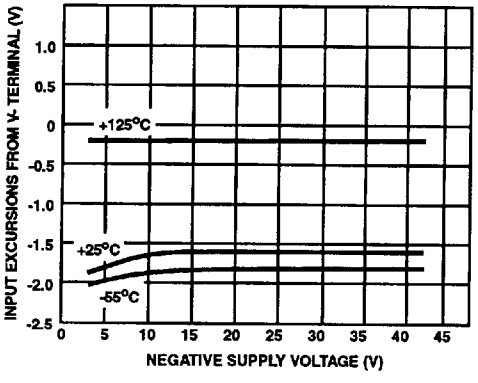


FIGURE 9. NEGATIVE COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

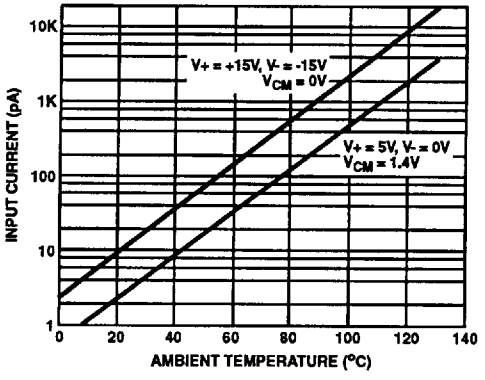


FIGURE 10. INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

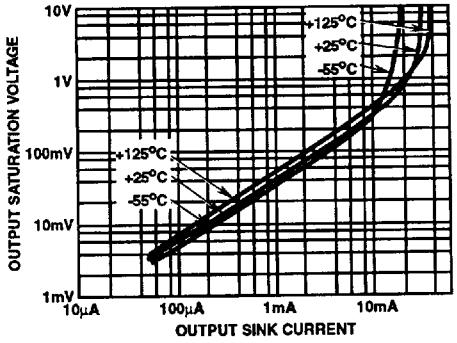


FIGURE 11. OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT

Operating Considerations

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra high input impedance (≅1.7TΩ);
2. The availability of common mode rejection for input signals at potentials below that of the negative power supply rail;
3. Retention of the in phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input terminal currents should not exceed 1mA. Appropriate series connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1mV to 10mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8 lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, switching rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1kΩ a capacitor (≥ 1pF - 2pF) be connected between the appropriate input terminal and the output terminal. (See Figure 2.)

The CA3290A and CA3290 are also supplied in a 14 lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V+ or V- supply rail. If either comparator is unused, its input terminals should also be tied to either the V+ or V- supply rail.

Typical Applications

Light Controlled One-Shot Timer

In Figure 12 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be constant to insure constant reverse voltage bias on the photo diode.

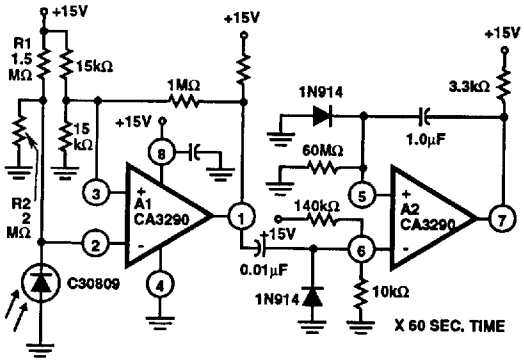


FIGURE 12. LIGHT CONTROLLED ONE-SHOT TIMER

Low-Frequency Multivibrator

In this application, one half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading. RP is the parallel combination of the two 1MΩ resistors connected between +15V and GND.

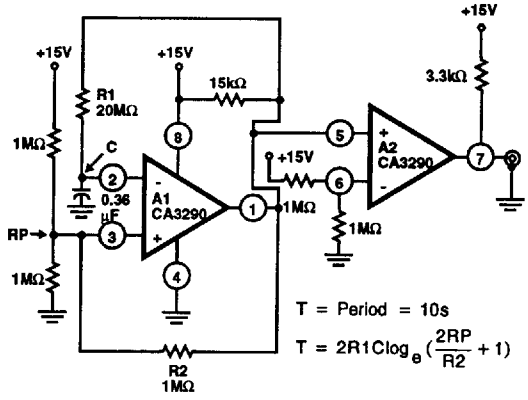


FIGURE 13. LOW FREQUENCY MULTIVIBRATOR

Window Comparator

Both halves of the CA3290 can be used in a high input impedance window comparator as shown in Figure 14. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the R1/R2/R3 resistor divider.

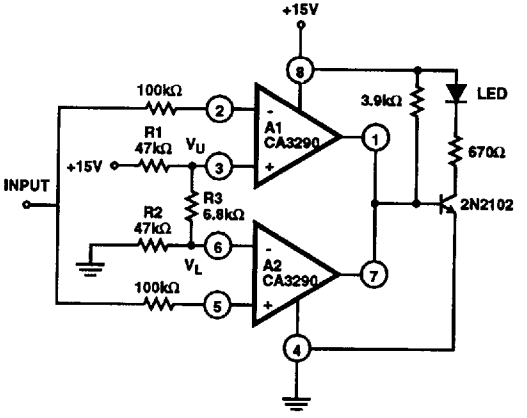


FIGURE 14. WINDOW COMPARATOR