1 Megabit Static RAM
128K x 8-Bit

Features

- High speed access times
  Com'l: 10, 12, 15, 17, 20 and 25 ns
  Ind'l: 15, 17, 20, and 25 ns
- Low power operation
  - PDM41024SA
    Active: 400 mW (typ.)
    Standby: 150 mW (typ.)
  - PDM41024LA
    Active: 350 mW (typ.)
    Standby: 100 mW (typ.)
- Single +5V (±10%) power supply
- Packages
  CerDIP (400 mil) - D
  Plastic SOJ (300 mil) - TSO
  Plastic SOJ (400 mil) - SO
  Plastic DIP (400 mil) - P
  Plastic TSOP - T

Description

The PDM41024 is a high-performance CMOS static RAM organized as 131,072 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE1}$) inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ are both LOW.

The PDM41024 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41024 comes in two versions, the standard power version PDM41024SA and a low power version the PDM41024LA. The two versions are functionally the same and only differ in their power consumption.

The PDM41024 is available in a 32-pin 400 mil cer-DIP, 400 mil Plastic DIP, plastic TSOP, 300 mil and 400 mil SOJ.

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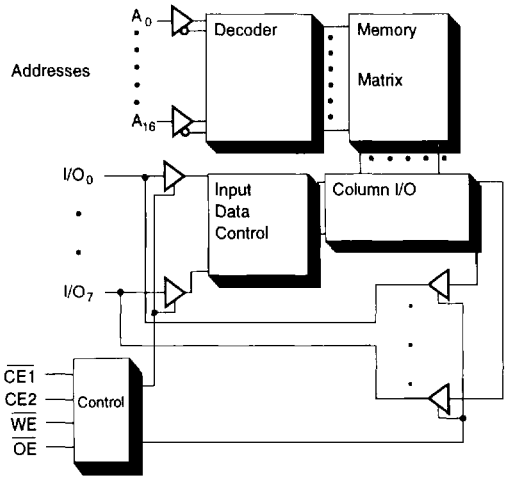
Functional Block Diagram



Pin Configuration

DIP, SOJ, TSOP

NC	1	32	Vcc
A16	2	31	A15
A14	3	30	CE2
A12	4	29	$\overline{WE}$
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE1}$
A0	12	21	I/O7
I/O0	13	20	I/O6
I/O1	14	19	I/O5
I/O2	15	18	I/O4
GND	16	17	I/O3

Truth Table[1]

$\overline{OE}$	$\overline{WE}$	$\overline{CE1}$	CE2	I/O	MODE
X	X	H	X	Hi-Z	Standby
X	X	X	L	Hi-Z	Standby
L	H	L	H	D_{OUT}	Read
X	L	L	H	D_{IN}	Write
H	H	L	H	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings [1]

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Military	Ambient Temperature	-55	25	125	°C
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	-0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V±10%)

Symbol	Parameter	Test Conditions		PDM41024SA		PDM41024LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	Com'l/ Ind.	–5	5	–2	5	µA
I_{LO}	Output Leakage Current	V_{CC} = MAX., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Com'l/ Ind.	–5	5	–2	5	µA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			–0.5(1)	0.8	–0.5(1)	0.8	V
V_{OL}	Output Low Voltage	I_{OL}=8 mA, V_{CC} = Min. I_{OL} = 10 mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns

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Power Supply Characteristics

Symbol	Parameter	Power	-10	-12	-15		-17		-20		-25		Unit
			Com'l.	Com'l.	Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	Com'l.	Ind.	
I_{CC}	Operating Current $\overline{CE}$ = V_{IL}, and CE2 = V_{IH}	SA	250	230	185	195	165	175	155	165	145	155	mA
	f = f_{MAX} = $1/t_{RC}$ V_{CC} = Max. I_{OUT} = 0 mA	LA	230	210	165	175	155	165	140	150	135	145	mA
I_{SB}	Standby Current $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}	SA	80	70	55	55	50	50	45	45	40	40	mA
	f = f_{MAX} = $1/t_{RC}$ V_{CC} = Max.	LA	75	65	50	50	45	45	40	40	35	35	mA
I_{SB1}	Full Standby Current $\overline{CE1}$ ≥ V_{HC} or CE2 ≤ V_{LC}	SA	20	20	10	15	10	15	10	15	10	15	mA
	f = 0 V_{CC} = Max., V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	LA	10	10	5	10	5	10	5	10	5	10	mA

SHADED AREA = PRELIMINARY DATA

NOTES: All values are maximum guaranteed values.

V_{LC} ≤ 0.2V, V_{HC} ≥ V_{CC} – 0.2V

Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

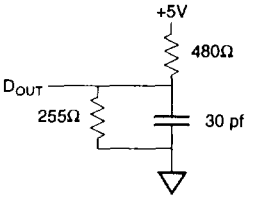


Figure 1. Output Load Equivalent

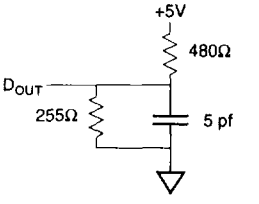


Figure 2. Output Load Equivalent
(for t_{LZCE}, t_{HZWE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

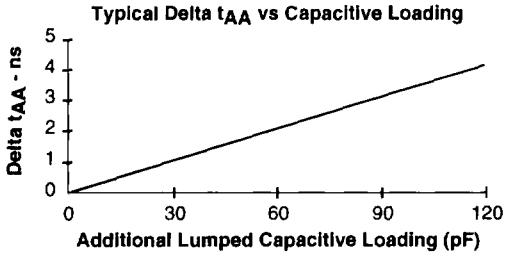
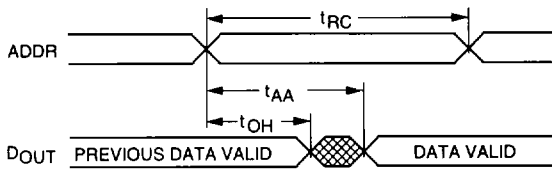
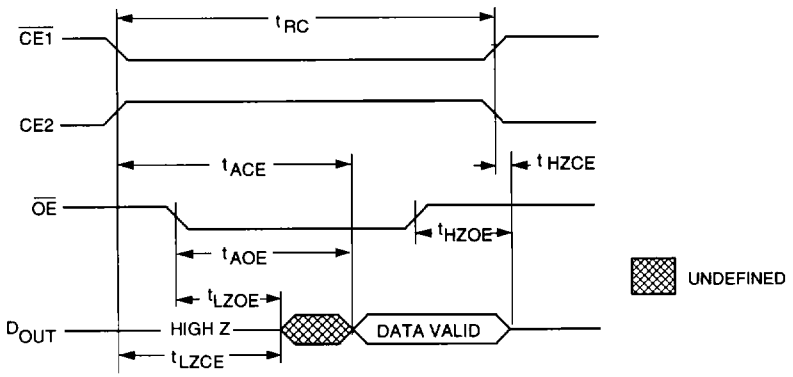


Figure 4.

Read Cycle No. 1[4, 5]



Read Cycle No. 2[2, 4, 6]

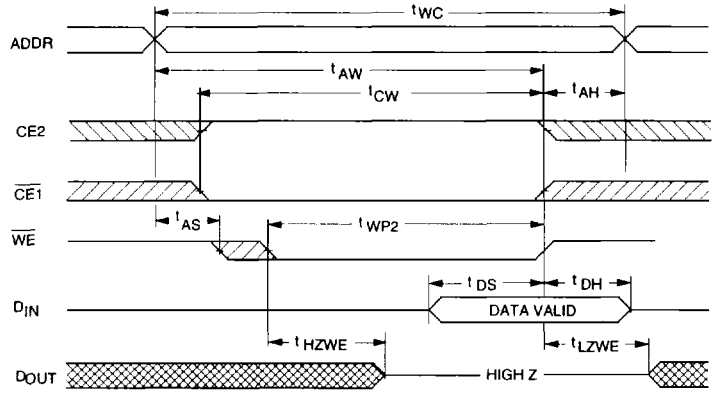


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

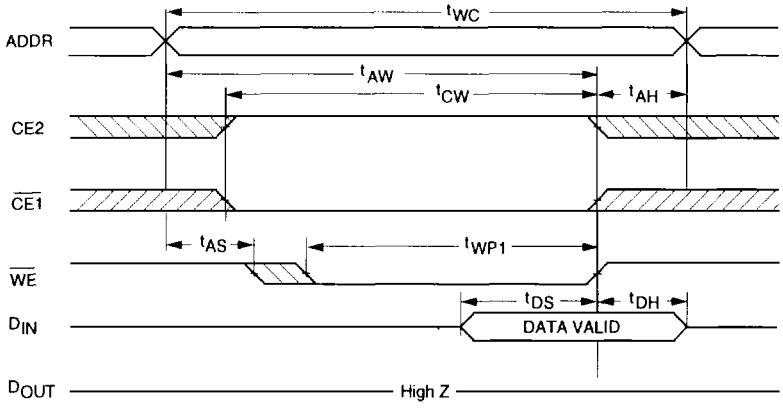
Description		-10[7]		-12[7]		-15		-17		-20		-25		
READ Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ cycle time	t_{RC}	10		12		15		17		20		25		ns
Address access time	t_{AA}		10		12		15		17		20		25	ns
Chip enable access time	t_{ACE}		10		12		15		17		20		25	ns
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns
Chip enable to output in low Z[1, 3]	t_{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z[1, 2, 3]	t_{HCZE}		6		6		7		7		8		10	ns
Chip enable to power up time[3]	t_{PU}	0		0		0		0		0		0		ns
Chip disable to power down time[3]	t_{PD}		10		12		15		17		20		25	ns
Output enable access time	t_{AOE}		6		6		6		6		6		8	ns
Output Enable to output in low Z [1,3]	t_{LZOE}	0		0		0		0		0		0		ns
Output disable to output in high Z[1,3]	t_{HZOE}		6		6		6		6		6		8	ns

SHADED AREA = PRELIMINARY DATA.
Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)

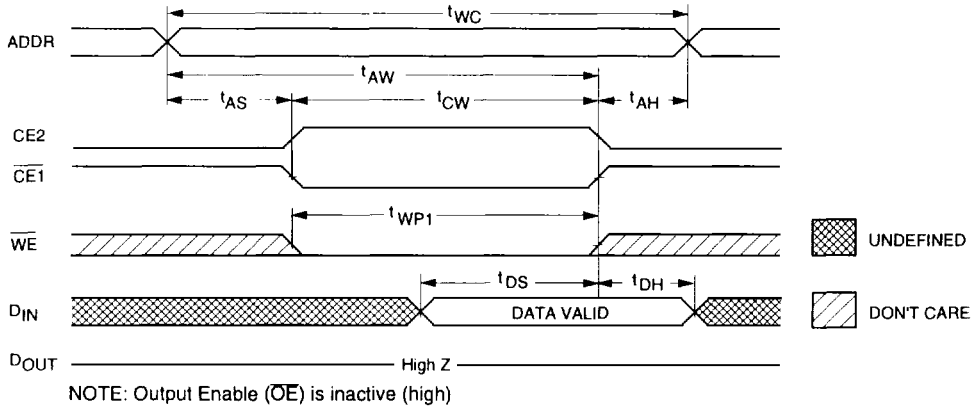


Write Cycle No. 2 (Write Enable Controlled)



NOTE: Output Enable ($\overline{OE}$) is inactive (high)

Write Cycle No. 3 (Chip Enable Controlled)



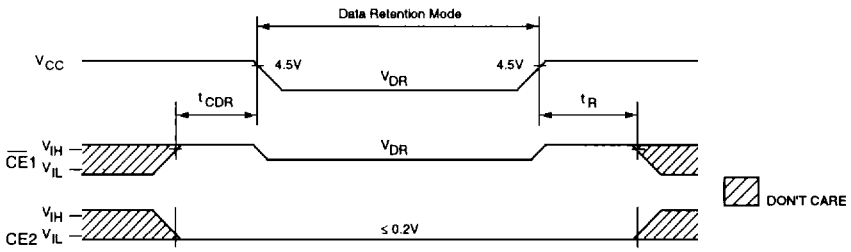
NOTE: Output Enable ($\overline{OE}$) is inactive (high)

AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-10[7]		-12[7]		-15		-17		-20		-25		
WRITE Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE Cycle time	t_{WC}	10		12		15		17		20		25		ns
Chip enable access time	t_{CW}	10		10		11		12		13		15		ns
Address Valid to end of write	t_{AW}	10		10		11		12		13		15		ns
Address setup time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP1}	9		10		11		12		13		15		ns
Write pulse width	t_{WP2}	10		11		12		13		14		15		ns
Data setup time	t_{DS}	7		7		7		8		8		10		ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns
Write disable to output in low Z[1, 3]	t_{LZ}	0		0		0		0		0		0		ns
Write enable to output in high[1, 3]	t_{HZWE}		7		7		7		7		8		10	ns

SHADED AREA = PRELIMINARY DATA

Low V_{CC} Data Retention Waveform



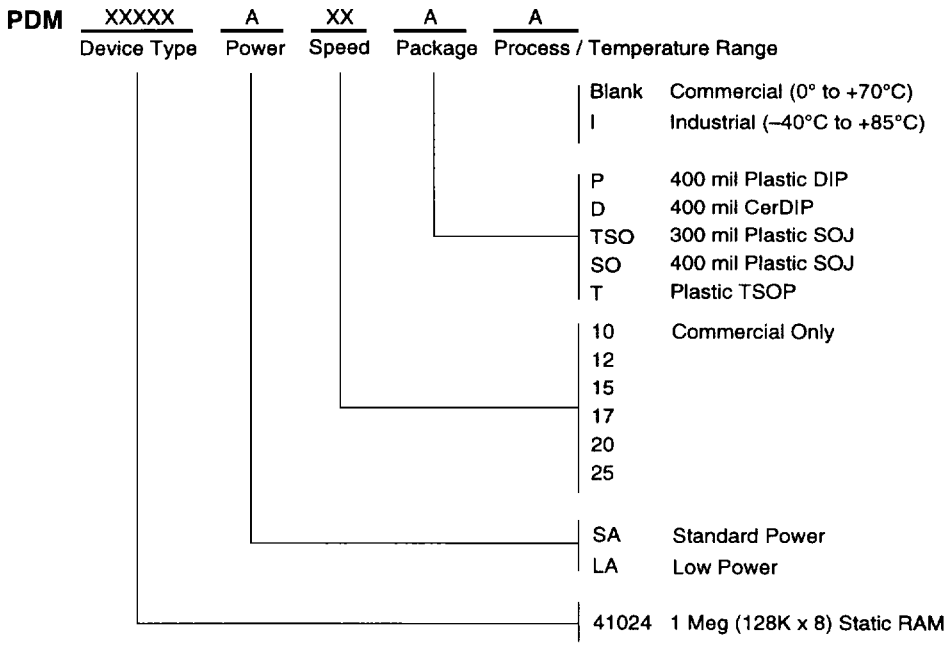
Data Retention Electrical Characteristics (LA Version Only) for JEDEC Version

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq V_{SS} + 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	V_{CC} = 2V	—	—	500	µA
			V_{CC} = 3V	—	—	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. The parameter is tested with CL = 5 pF as shown in Fig. #2. Transition is measured ±200 mV from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
3. This parameter is sampled.
4. $\overline{WE}$ is high for a READ cycle.
5. The device is continuously selected. All the Chip Enables are held in their active state.
6. The address is valid prior to or coincident with the latest occuring Chip Enable.
7. Vcc = 5V ±5%.

Ordering Information



Chip	Package Type
PDM41024	32-pin Plastic SOJ 300 Mil
	32-pin Plastic SOJ 400 Mil
	32-pin Plastic TSOP
	32-pin Plastic DIP 400 Mil
	32-pin CerDIP 400 Mil