Am2927/Am2928

Quad Three-State Bus Transceivers With Clock Enable

DISTINCTIVE CHARACTERISTICS

- Three-state bus driver outputs can sink 48mA, and Three-state receiver outputs sink 24mA — both at 0.5V max.
- D-type register on drivers
- Latch output on Am2927; Registered output on Am2928
- Output data to input wrap around gating; Input register to output transfer gating with or without driving data bus
- Clock enabled registers
- 3.0V minimum V_{OH} for direct interface to MOS microprocessors

GENERAL DESCRIPTION

The Am2927 and Am2928 are high-performance, low-power Schottky, quad bus transceivers intended for use in bipolar or MOS microprocessor system applications.

Both devices feature register enable lines which function as clock enables without introducing gate delay in the clock inputs. The four transceivers share common enables, clock, select and three-state control lines.

The Am2927 consists of four D-type edge-triggered flip-flops. Each flip-flop output is connected to a three-state data bus driver and separately to the input of a corresponding receiver latch input. The receiver latch can select input from the driver or the data bus. The select line determines the source of input data for the bus driver choosing between input data or data recirculated from the receiver output. The receiver output also has a three-state output buffer.

The combination of the select input, S, the driver input enable, $\overline{ENDR}$, and the receiver latch enable, $\overline{RLE}$, provide seven different data path operating modes not available in other transceivers. For example, transmitted data can be stored in the receiver for subsequent retransmission. Also, received data can be output to the system and simultaneously fed back to the driver input.

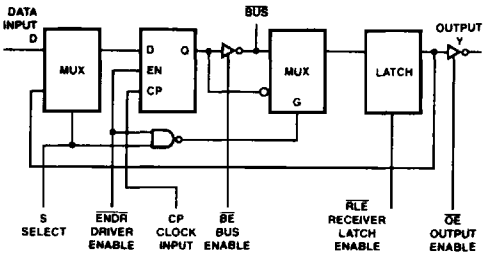
The Am2928 is similar to the Am2927, but with a D-type edge-triggered register in the receiver and a receiver enable, $\overline{ENREC}$, which functions as a common clock enable.

Data from each D input is inverted at the bus output. Likewise, data at the bus input is inverted at the receiver output.

All three-state controls and enable lines are active low (the Am2927 receiver latch is transparent when $\overline{RLE}$ is LOW). The select input, S, determines whether the enabled driver input accepts data from the data input, D, or from the corresponding receiver output, Y. Similarly, the select line determines whether the receiver accepts input data from the data bus, or the driver output.

BLOCK DIAGRAM

Am2927



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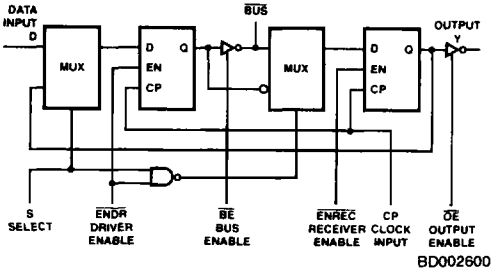
Am2928



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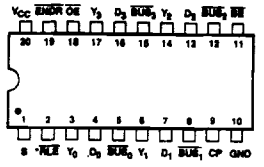
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-20-1



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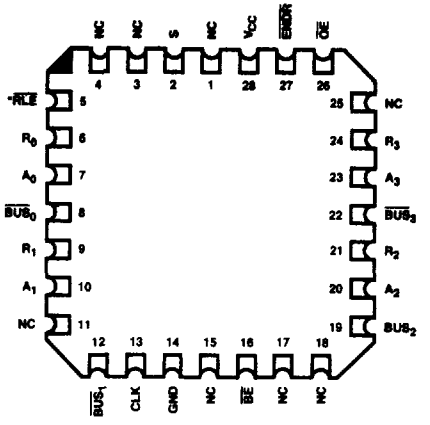

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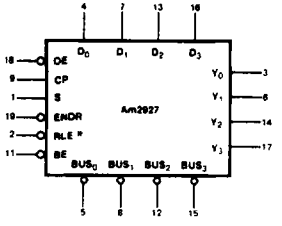
Note: Pin 1 is marked for orientation
*ENREC for Am2928

LOGIC SYMBOL



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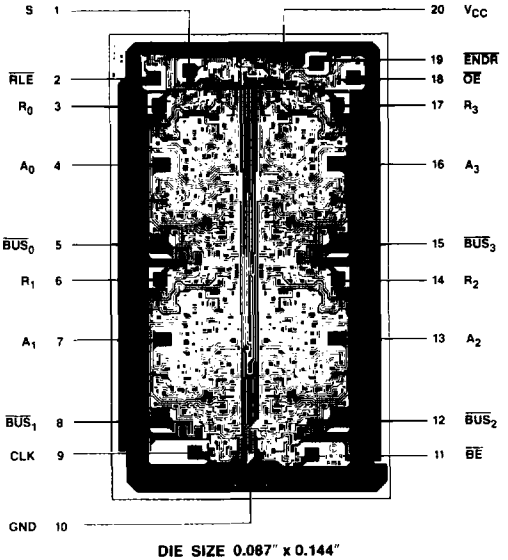
*ENREC for Am2928

METALLIZATION AND PAD LAYOUT
Am2927*

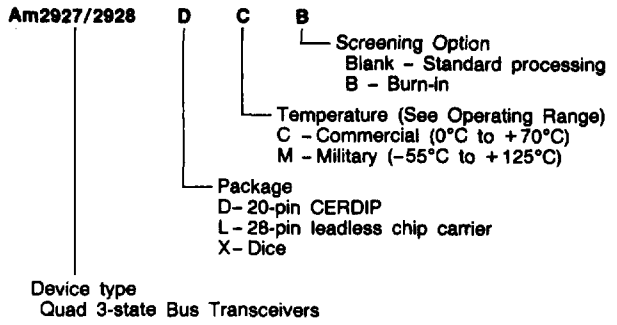


DIE SIZE 0.087" x 0.144"

NOTE: The Am2928 is similar to the Am2927, but with a D-type edge-triggered register in the receiver and a receiver enable, ENREC, which functions as a common clock enable.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am2927 Am2928	DC, DM LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
9	CP	I	Clock Pulse to internal registers enters data on the LOW-to-HIGH transition.
11	$\overline{BE}$	I	Bus Enable. When Bus Enable is LOW the four drivers drive the $\overline{BUS}$ outputs.
5, 8, 12, 15	$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$	I/O	The four driver outputs and receiver inputs.
4, 7, 13, 16	D_0, D_1, D_2, D_3	I	The four driver data inputs inverting from D to $\overline{BUS}$.
3, 6, 14, 17	Y_0, Y_1, Y_2, Y_3,	O	The four receiver data outputs inverting from $\overline{BUS}$ to Y.
1	S	I	Select input controls data path modes in conjunction with $\overline{ENDR}$ and $\overline{RLE}$ (or $\overline{ENREC}$).
18	$\overline{OE}$	I	Output Enable. When Output Enable is LOW the four receiver outputs Y are active.
19	$\overline{ENDR}$	I	Driver Enable. Common clock enable for the input register. Allows the data on the D inputs to be loaded into the driver register on the clock LOW-to-High transition.
2	$\overline{RLE}$	I	Receiver Latch Enable (Am2927 only). When Receiver Latch Enable is LOW, the four receiver latches are transparent.The latches hold received data when $\overline{RLE}$ is HIGH.
2	$\overline{ENREC}$	I	Receiver Enable (Am2928 only). Common clock enable for the receiver register. Allows the $\overline{BUS}$ driver or previous receiver data to enter the receiver register on the rising edge of the clock.

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Am2927 FUNCTION TABLES

Driver Register Control

$\overline{ENDR}$	S	$\overline{RLE}$	Driver Register
H	X	X	Hold Previous Data
L	L	X	Load from D Input
L	H	L	Load from $\overline{BUS}$
L	H	H	Load Latched Receiver Data

Receiver Latch Control

$\overline{ENDR}$	S	$\overline{RLE}$	Receiver Output
X	X	H	Data Latched
H	H	L	Driver Register Output at Y output (Latch Transparent)
X	L	L	Bus Data at Y Output (Latch Transparent)
L	X	L	

Am2928 FUNCTION TABLES

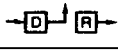
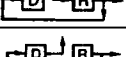
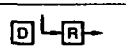
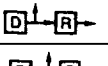
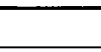
Driver Register Control

$\overline{ENDR}$	S	Driver Register
H	X	Hold Previous Data
L	L	Load from D input
L	H	Load from Receiver Register

Receiver Register Control

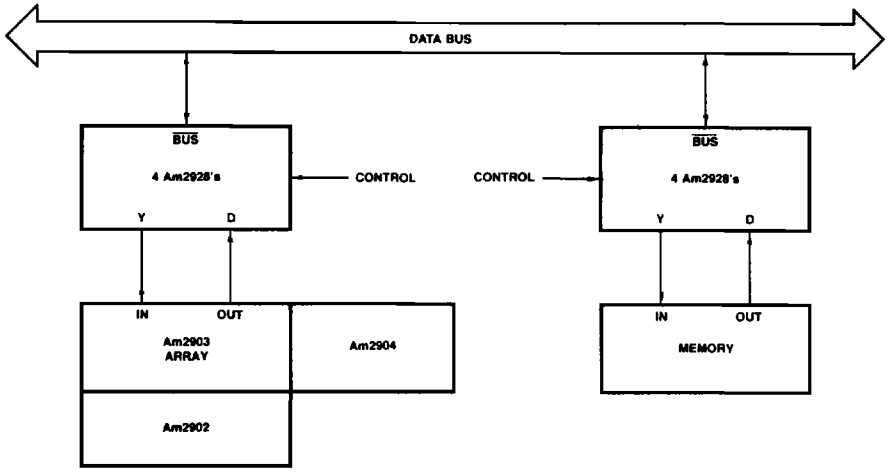
$\overline{ENDR}$	S	$\overline{ENREC}$	Receiver Output
X	X	H	Hold Previous Data
H	H	L	Load from Driver Register
X	L	L	Load from $\overline{BUS}$
L	X	L	

Am2927 AND Am2928 FUNCTION TABLE

Driver Input From	Receiver Input From	Control Input Condition			Signal Flow	$\overline{BE}$
		S	$\overline{ENDR}$	*		
D Input	BUS	L	L	L		H
	(No Load)	L	L	H		L
Receiver	BUS	H	L	L		H
	(No Load)	H	L	H		L
(No Load)	BUS	L	H	L		H
	Driver	H	H	L		X
	(No Load)	X	H	H		L

*$\overline{RLE}$ for Am2917 (asynchronous) or $\overline{ENREC}$ for Am2928 (⌐‾).

APPLICATION



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The Am2927 and Am2928 can be used to provide Data Bus, Address Bus and Control Bus Interface in a high-speed bipolar microprocessor system.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Output Current, Into Bus 100mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.4		
		V_{CC} = 5.0V	I_{OH} = −100μA	3.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 24mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	S, $\overline{ENDR}$			−2.8	mA
			All other inputs			−1.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	S, $\overline{ENDR}$			100	μA
			All other inputs			50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Off-State Output Current (Receiver Output)	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX	Receiver	−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2927		150	185	mA
			Am2928		153	190	

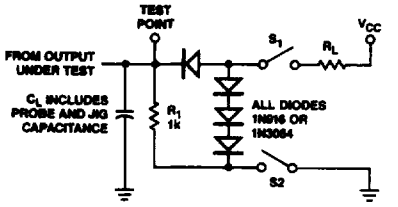
Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. This parameter is typical of device characterization data and is not tested in production.

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 12mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	I_{OH} = −20mA	2.4			Volts
			I_{OH} = −15mA	2.4			
V_{IH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus Enable = 2.4V				0.8	Volts
I_{OFF}	Bus Leakage Current (Power Off)	V_{CC} = 0V, V_O = 4.5V				100	µA
I_{OZL}	Bus Leakage Current (Three-State)	V_{CC} = MAX, BUS Enable = 2.4V	V_O = 0.4V			−1.4	mA
I_{OZH}			V_O = 2.5V			100	µA
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX, V_O = 0V		−50		−255	mA
C_S	Bus Capacitance (Note 4)	V_{CC} = 0V			8		pF

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. This parameter is typical of device characterization data and is not tested in production.

SWITCHING TEST CIRCUIT



Note: For standard totem-pole outputs, remove R_1; S_1 and S_2 closed.

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Am2927

Parameters	Description	Test Conditions (Note 2)	COMMERCIAL Am2927 Min	Typ	Max	MILITARY Am2927 Min	Typ	Max	Units
t_{PLH}	Driver Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L(BUS) = 130Ω		18	26		18	23	ns
t_{PHL}				18	26		18	23	
t_{ZH} • t_{ZL}	Bus Enable, $\overline{BE}$, to $\overline{BUS}$			14	26		1	23	ns
t_{HZ} • t_{LZ}		R_L = 130Ω, C_L = 5pF		12	18/23			16/23	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		18						ns
t_{PLH}	$\overline{BUS}$ to Receiver Output (Latch Enabled)	C_L = 5			23		16	20	ns
t_{PHL}					2		16	20	
t_{PLH}	Latch Enable, $\overline{RLE}$, to Receiver Output				26		18	23	ns
t_{PHL}					26		18	23	
t_{ZH} • t_{ZL}	Output Enable, $\overline{OE}$, to Receiver Output				23			21	ns
t_{HZ} • t_{LZ}		C_L = F, R_L = 270Ω			21		14	18	
t_s	Driver En , E R, Clock		10			9			ns
t_h			3			3			
t_s	Se o Clo (RLE = HIGH)		18			15			ns
t_h			3			2			
t_{PLH}	Select S, to Receiver Output	C_L = 50pF, R_L = 270Ω			26			23	ns
t_{PHL}					35			30	
t_s	Data Inputs D, to Clock		9			7			ns
t_h			5			4			
t_s	$\overline{BUS}$ to Latch Enable, $\overline{RLE}$		11			10			ns
t_h			4			3			

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2928

Parameters	Description	Test Conditions (Note 2)	COMMERCIAL Am2928 Min	COMMERCIAL Am2928 Typ (Note 1)	COMMERCIAL Am2928 Max	MILITARY Am2928 Min	MILITARY Am2928 Typ (Note 1)	MILITARY Am2928 Max	Units
t_{PLH}	Driver Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF		18	23			26	ns
t_{PHL}		R_L(BUS) = 130Ω		18	23			26	
t_{ZH} • t_{ZL}	Bus Enable, $\overline{BE}$, to $\overline{BUS}$			14	23			26	ns
t_{HZ} • t_{LZ}		R_L = 130Ω, C_L = 5pF		12	23			18/30	
t_{PLH}	Clock, CP, to Receiver Output				23			26	ns
t_{PHL}		C_L = 50p			23			26	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		5			18			ns
t_{ZH} • t_{ZL}	Output Enable, $\overline{OE}$, to Receiver Out			14	21			23	ns
t_{HZ} • t_{LZ}		C_L = 5p		21	18			26	
t_s	Driver En		9			10			ns
t_h			3			3			
t_s	$\overline{BUS}$ Clock (Receiver Register)		7			8			ns
t_h			4			5			
t_s	Receiver Enable, $\overline{ENMREC}$, to Clock		8			10			ns
t_h			4			5			
t_s	S to Clock		10			12			ns
t_h			4			5			
t_s	Data Inputs, D, to Clock (Driver Register)		7			9			ns
t_h			4			5			

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.