CD54/74HCT112
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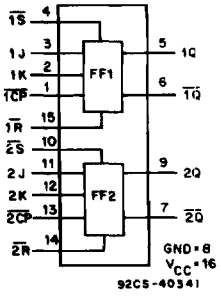
File Number **1843**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual J-K Flip-Flop with Set and Reset

Negative-Edge Trigger

Type Features:

- *Hysteresis on clock inputs for improved noise immunity and increased input rise and fall times*
- *Asynchronous set and reset*
- *Complementary outputs*
- *Buffered inputs*
- *Typical f_{max} = 60 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC112 and CD54/74HCT112 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Set, Reset, and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. Set and Reset are accomplished asynchronously by low-level inputs.

The 54HCT/74HCT logic family is functionally as well as pin-compatible with the standard 54LS/74LS logic family.

The CD54HC112 and CD54HCT112 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC112 and CD74HCT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H *	H *
H	H	↘	L	L	No Change	
H	H	↘	H	L	H	L
H	H	↘	L	H	L	H
H	H	↘	H	H	Toggle	
H	H	H	X	X	No Change	

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

* Output states unpredictable if $\overline{S}$ and $\overline{R}$ go High simultaneously after both being low at the same time.
H = High steady state.
L = Low steady state.
X = Irrelevant.
↘ = High-to-Low transition.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

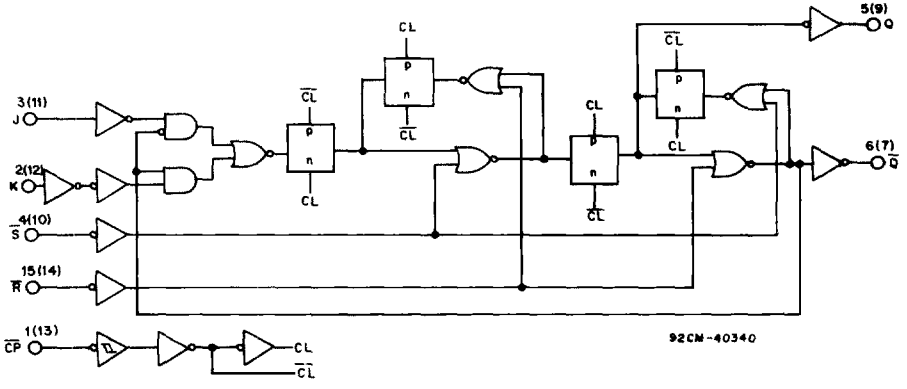

Fig. 1 - Flip-flop logic diagram.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f •			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.
• Applicable for all inputs except clock.

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STATIC ELECTRICAL CHARACTERISTICS

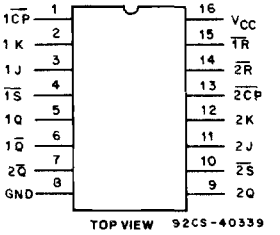
CHARACTERISTICS	CD74HC112, CD54HC112										CD74HCT112, CD54HCT112									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage CMOS Loads V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage CMOS Loads V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
$\overline{1S}$, $\overline{2S}$	0.5
1K, 2K	0.6
$\overline{1R}$, $\overline{2R}$	0.65
1J, 2J, $\overline{1CP}$, $\overline{2CP}$	1

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay					
$\overline{CP}$ to Q, $\overline{Q}$	t_{PLH}, t_{PHL}	15	14	14	ns
$\overline{S}$ to Q, $\overline{Q}$			13	13	ns
$\overline{R}$ to Q, $\overline{Q}$			15	14	ns
$\overline{CP}$ Frequency	f_{max}	15	60	60	MHz
Power Dissipation Capacitance *	C_{PD}	—	12	20	pF

* C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where: f_i = input frequency, C_L = output load capacitance, f_o = output frequency, V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{CP}$		4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{R}$, $\overline{S}$		4.5	16	—	18	—	20	—	23	—	24	—	27	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	
J, K to $\overline{CP}$		4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	
J, K to $\overline{CP}$		4.5	0	—	3	—	0	—	3	—	0	—	3	—	ns
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Removal Time	t_{REM}	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{R}$ to $\overline{CP}$		4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
$\overline{S}$ to $\overline{CP}$		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{CP}$ Frequency	f_{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	
		4.5	30	—	30	—	25	—	25	—	20	—	20	—	MHz
		6	35	—	—	—	29	—	—	—	23	—	—	—	

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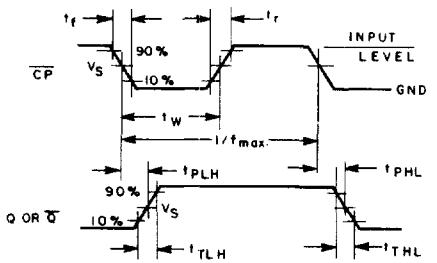
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay $\overline{CP}$ to Q, $\overline{Q}$	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{S}$ to Q, $\overline{Q}$		2	—	155	—	—	—	195	—	—	—	235	—	—	
		4.5	—	31	—	32	—	39	—	40	—	47	—	48	ns
		6	—	26	—	—	—	33	—	—	—	40	—	—	
$\overline{R}$ to Q, $\overline{Q}$		2	—	180	—	—	—	225	—	—	—	270	—	—	
		4.5	—	36	—	37	—	45	—	46	—	54	—	56	ns
		6	—	31	—	—	—	38	—	—	—	46	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



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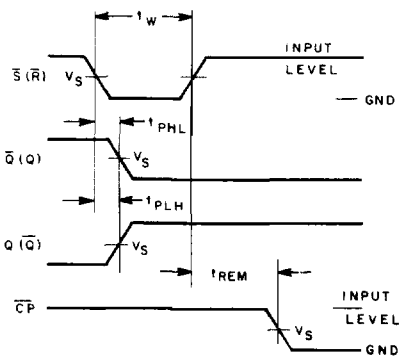

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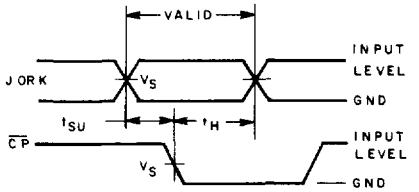

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	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times, propagation delay times, and setup and hold times.