NEC

MOS INTEGRATED CIRCUIT
μPD42S16165L, 4216165L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM
1 M-WORD BY 16-BIT, HYPER PAGE MODE(EDO),
BYTE READ/WRITE MODE

Description

The μPD42S16165L, 4216165L are 1,048,576 words by 16 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S16165L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S16165L, 4216165L are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 16 bits organization
- Single +3.3 V ±0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S16165L-A60, 4216165L-A60	396 mW	60 ns	104 ns	25 ns
μPD42S16165L-A70, 4216165L-A70	360 mW	70 ns	124 ns	30 ns

- The μPD42S16165L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

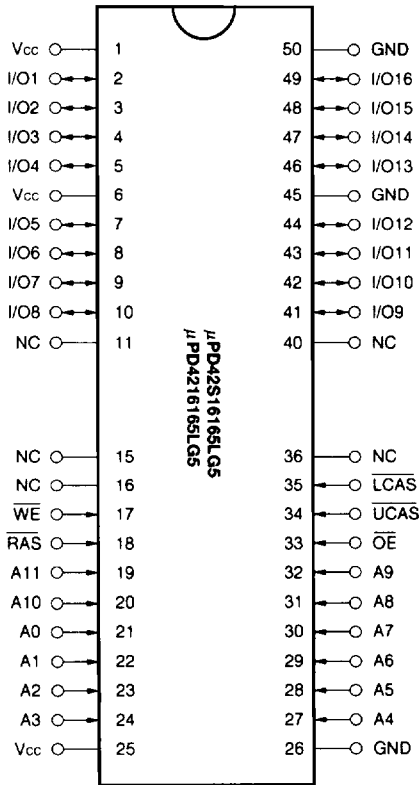| Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16165L	4,096 cycles / 128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD4216165L	4,096 cycles / 64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

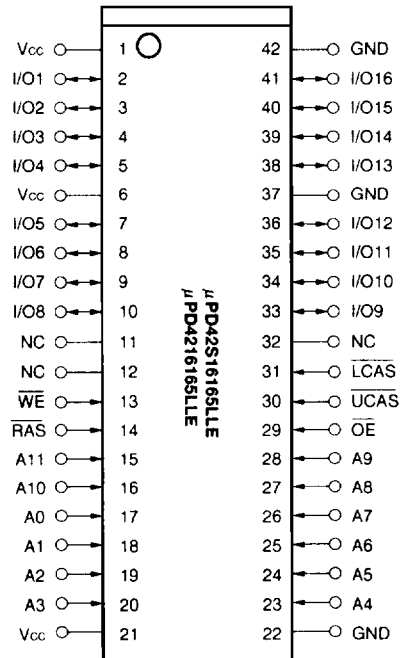**The information in this document is subject to change without notice.**

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S16165LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S16165LG5-A70	70 ns		
μPD42S16165LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD42S16165LLE-A70	70 ns		
μPD4216165LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4216165LG5-A70	70 ns		
μPD4216165LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD4216165LLE-A70	70 ns		

Pin Configurations (Marking Side)
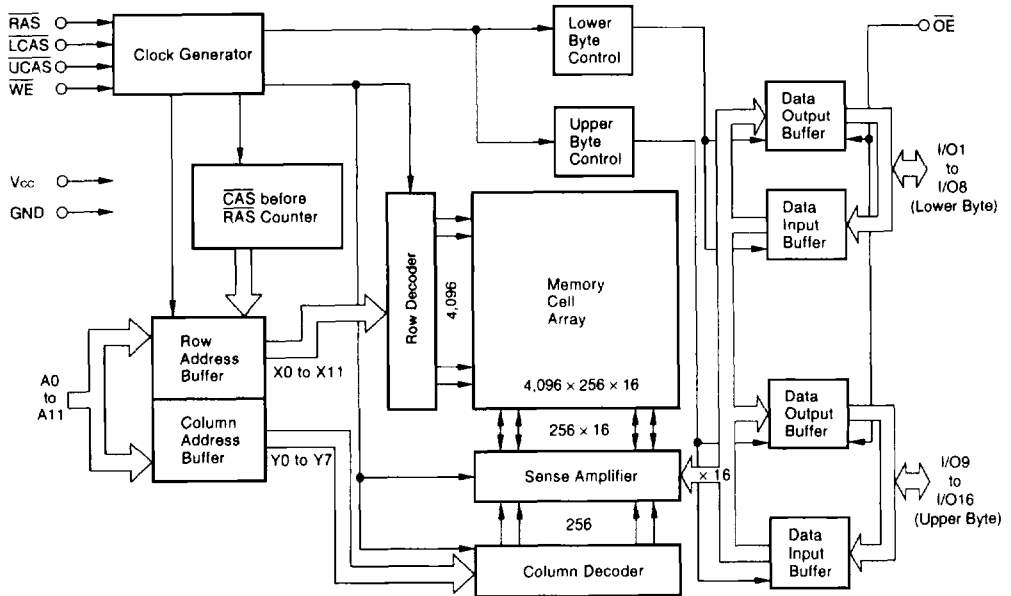
50-pin Plastic TSOP (II) (400 mil)

Pin		Pin	
Vcc	1	50	GND
I/O1	2	49	I/O16
I/O2	3	48	I/O15
I/O3	4	47	I/O14
I/O4	5	46	I/O13
Vcc	6	45	GND
I/O5	7	44	I/O12
I/O6	8	43	I/O11
I/O7	9	42	I/O10
I/O8	10	41	I/O9
NC	11	40	NC
NC	15	36	NC
NC	16	35	LCAS
WE	17	34	UCAS
RAS	18	33	OE
A11	19	32	A9
A10	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
Vcc	25	26	GND

μPD42S16165LG5
μPD4216165LG5

42-pin Plastic SOJ (400 mil)

Pin		Pin	
Vcc	1	42	GND
I/O1	2	41	I/O16
I/O2	3	40	I/O15
I/O3	4	39	I/O14
I/O4	5	38	I/O13
Vcc	6	37	GND
I/O5	7	36	I/O12
I/O6	8	35	I/O11
I/O7	9	34	I/O10
I/O8	10	33	I/O9
NC	11	32	NC
NC	12	31	LCAS
WE	13	30	UCAS
RAS	14	29	OE
A11	15	28	A9
A10	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
Vcc	21	22	GND

μPD42S16165LLE
μPD4216165LLE

A0 to A11	: Address Inputs
I/O1 to I/O16	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{UCAS}$	: Column Address Strobe (upper)
$\overline{LCAS}$	: Column Address Strobe (lower)
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply
GND	: Ground
NC	: No Connection

Block Diagram

```
RAS ──○──►┐
LCAS ──○──►│ Clock Generator ──────────────────────► Lower Byte Control                    OE ○──
UCAS ──○──►│                                                                    Data Output Buffer ──► I/O1 to I/O8 (Lower Byte)
WE ──○──►┘                          ──────────────► Upper Byte Control
                                                                               Data Input Buffer

Vcc ──○──►          CAS before RAS Counter

GND ──○──►

A0 to A11    Row Address Buffer    X0 to X11    Row Decoder    4,096    Memory Cell Array    4,096 × 256 × 16
                                                                                             256 × 16

             Column Address Buffer    Y0 to Y7                                               Sense Amplifier    × 16    Data Output Buffer ──► I/O9 to I/O16 (Upper Byte)
                                                                                             256                        Data Input Buffer

                                                                 Column Decoder
```

Input/Output Pin Functions

The μPD42S16165L, 4216165L have input pins $\overline{RAS}$, $\overline{CAS}$^{Note}, $\overline{WE}$, $\overline{OE}$, A0 to A11 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 12-bit and lower 8-bit in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle
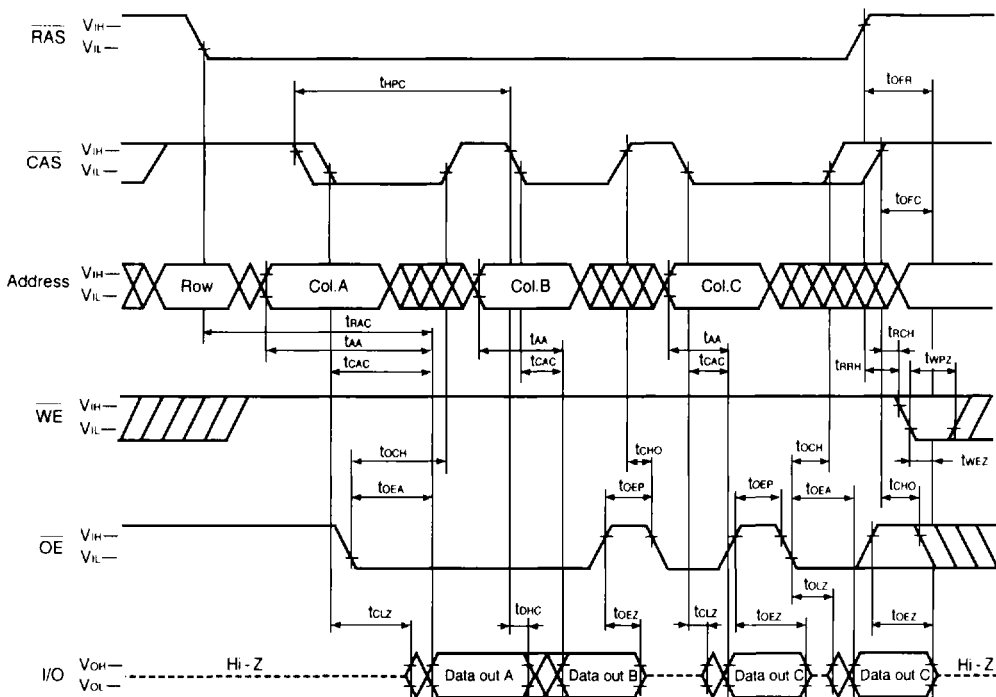
Cautions when using the hyper page mode (EDO)

1. $\overline{\text{CAS}}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.
    (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of read cycle)
        $\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active
        t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.
        t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.
    (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)
        $\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive ····· t_{OEZ} is effective.
    (3) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)
        $\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{\text{CAS}}$ signal when controlling data output with the $\overline{\text{OE}}$ signal.
    (1) $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active ····· t_{CHO} is effective.
    (2) $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active ····· t_{OCH} is effective.

373

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution   Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	$t_{RAC} = 60$ ns		90	mA	1, 2, 3
			$t_{RC} = t_{RC(MIN.)}$, Io = 0 mA	$t_{RAC} = 70$ ns		80		
Standby current	μPD42S16165L	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, Io = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, Io = 0 mA			0.15		
	μPD4216165L		$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, Io = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, Io = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH(MIN.)}$	$t_{RAC} = 60$ ns		90	mA	1, 2, 3 ,4
			$t_{RC} = t_{RC(MIN.)}$, Io = 0 mA	$t_{RAC} = 70$ ns		80		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ cycling	$t_{RAC} = 60$ ns		110	mA	1, 2, 5
			$t_{HPC} = t_{HPC(MIN.)}$, Io = 0 mA	$t_{RAC} = 70$ ns		100		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	$t_{RAC} = 60$ ns		90	mA	1, 2
			$t_{RC} = t_{RC(MIN.)}$, Io = 0 mA	$t_{RAC} = 70$ ns		80		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the μPD42S16165L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : $t_{RC} = 31.3$ μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} Io = 0 mA	$t_{RAS} \leq 1$ μs		220	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S16165L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: $t_{RASS} = 5$ ms $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V Io = 0 mA			150	μA	2
Input leakage current		$I_{I(L)}$	$V_I = 0$ to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current		$I_{O(L)}$	$V_O = 0$ to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage		V_{OH}	Io = −2.0 mA		2.4		V	
Low level output voltage		V_{OL}	Io = +2.0 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.
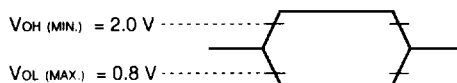
AC Characteristics (Recommended Operating Conditions unless otherwise noted)
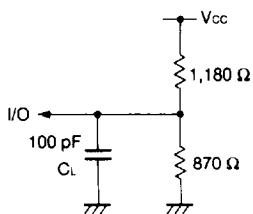
AC Characteristics Test Conditions

(1) Input timing specification

$V_{IH (MIN.)} = 2.0\ V$

$V_{IL (MAX.)} = 0.8\ V$

$t_T = 2\ ns$ $t_T = 2\ ns$
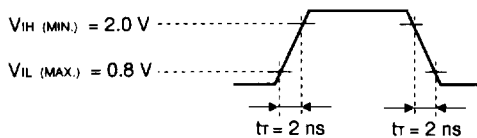
(2) Output timing specification

$V_{OH (MIN.)} = 2.0\ V$

$V_{OL (MAX.)} = 0.8\ V$

(3) Output load condition

Vcc

1,180 Ω

I/O

100 pF

C_L

870 Ω

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ precharge time		t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ precharge time		t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ pulse width		t_{RAS}	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time		t_{RSH}	10	–	12	–	ns	
$\overline{CAS}$ hold time		t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		t_{RCD}	14	45	14	52	ns	2
$\overline{RAS}$ to column address delay time		t_{RAD}	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		t_{CRP}	5	–	5	–	ns	3
Row address setup time		t_{ASR}	0	–	0	–	ns	
Row address hold time		t_{RAH}	10	–	10	–	ns	
Column address setup time		t_{ASC}	0	–	0	–	ns	
Column address hold time		t_{CAH}	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		t_{OES}	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		t_{CLZ}	0	–	0	–	ns	
$\overline{OE}$ to data setup time		t_{OLZ}	0	–	0	–	ns	
$\overline{OE}$ to data delay time		t_{OED}	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		t_{MRH}	0	–	0	–	ns	
Transition time (rise and fall)		t_T	1	50	1	50	ns	
Refresh time	µPD42S16165L	t_{REF}	–	128	–	128	ms	4
	µPD4216165L		–	64	–	64	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 µs.

   If 10 µs < t_{RAS} < 100 µs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \le t_{RAD\,(MAX.)}$ and $t_{RCD} \le t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \le t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD\,(MAX.)}$ and $t_{RCD\,(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \ge t_{RAD\,(MAX.)}$ and $t_{RCD} \ge t_{RCD\,(MAX.)}$ will not cause any operation problems.

3. $t_{CRP\,(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the µPD42S16165L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	17	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \le t_{RAD\,(MAX.)}$ and $t_{RCD} \le t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \le t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD\,(MAX.)}$ and $t_{RCD\,(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \ge t_{RAD\,(MAX.)}$ and $t_{RCD} \ge t_{RCD\,(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\,(MIN.)}$ or $t_{RRH\,(MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\,(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\,(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\,(MIN.)}$ and $t_{DH\,(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

| Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	tHPC	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	tRASP	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	tHCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	tCP	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	tACP	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	tCPWD	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35	–	40	–	ns	
Read modify write cycle time	tHPRWC	66	–	75	–	ns	
Data output hold time	tDHC	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5	–	5	–	ns	4
$\overline{OE}$ precharge time	tOEP	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	tWEZ	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	tWPZ	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	tOFR	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	tOFC	0	13	0	15	ns	3,4

Notes 1. tHPC (MIN.) is applied to $\overline{CAS}$ access.

   2. If tWCS ≥ tWCS (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If tRWD ≥ tRWD (MIN.), tCWD ≥ tCWD (MIN.), tAWD ≥ tAWD (MIN.) and tCPWD ≥ tCPWD (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

   3. tOFC (MAX.), tOFR (MAX.) and tWEZ (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to VOH or VOL.

   4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)

   $\overline{WE}$: inactive, $\overline{OE}$: active

   tOFC is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

   tOFR is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

   $\overline{WE}$, $\overline{OE}$: inactive ······ tOEZ is effective.

   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)

   $\overline{WE}$, $\overline{OE}$: active and either tRRH or tRCH must be met ······ tWEZ and tWPZ are effective.

   (4) $\overline{WE}$: inactive (in read cycle)

   $\overline{CAS}$: inactive, $\overline{OE}$: active ······ tCHO is effective.

   $\overline{CAS}$, $\overline{OE}$: active ······ tOCH is effective.

Refresh Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	µs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the µPD42S16165L.
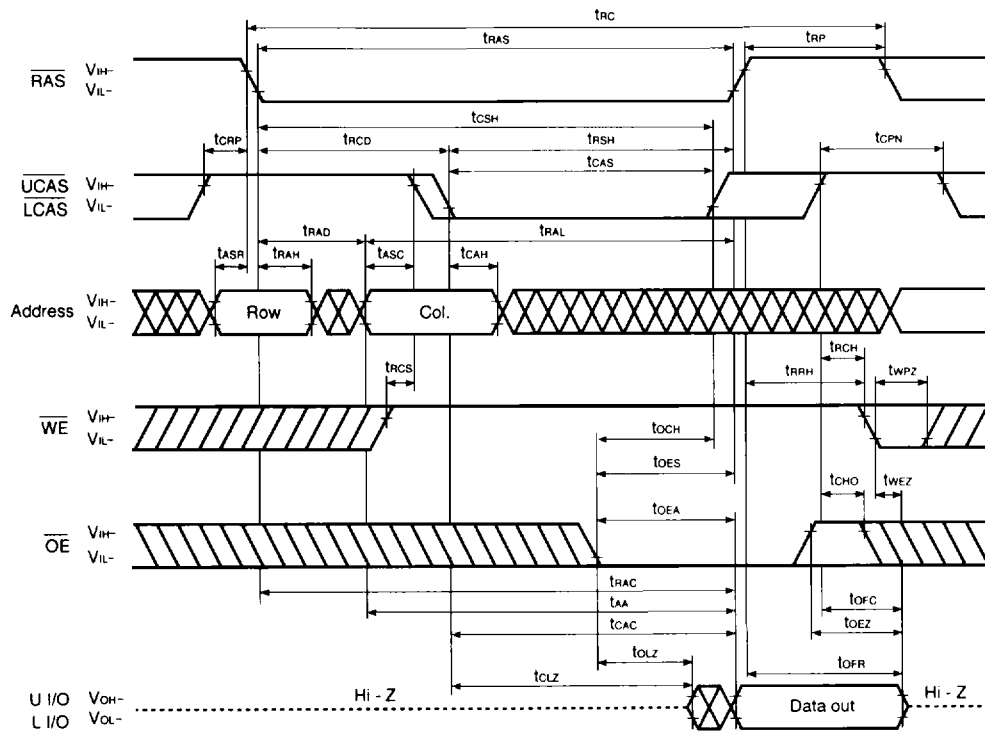
Read Cycle

Upper Byte Read Cycle
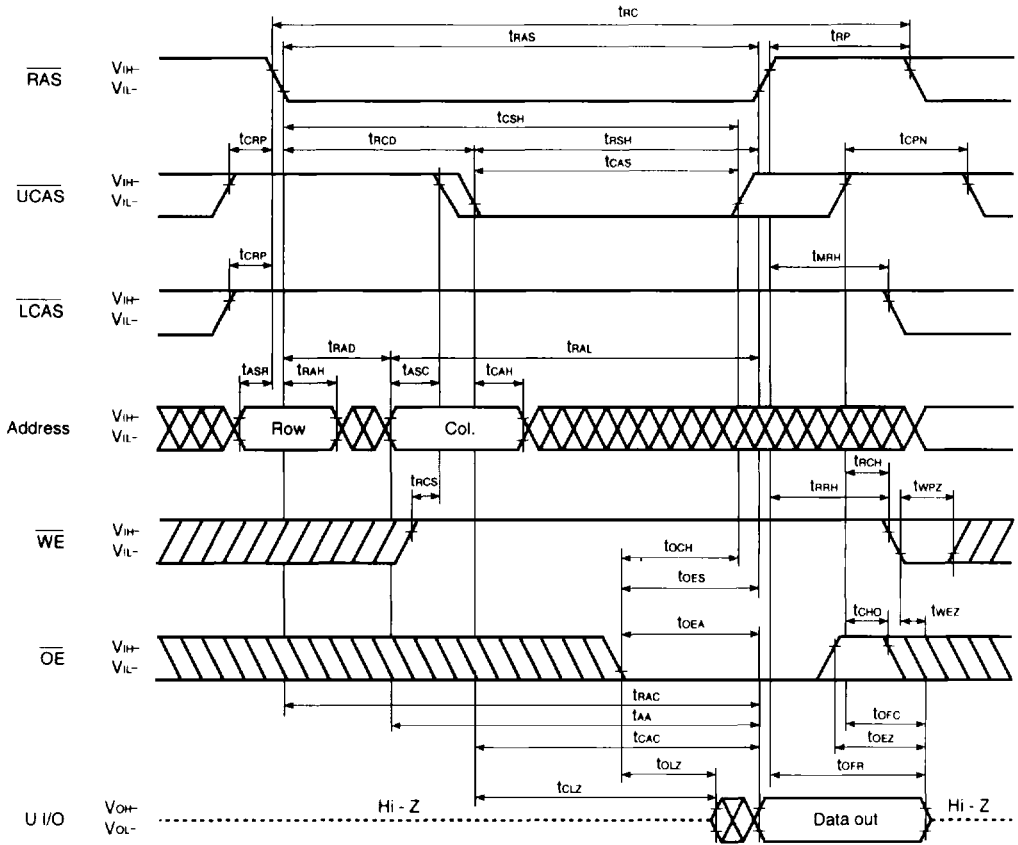
Remark L I/O: Hi-Z

Lower Byte Read Cycle
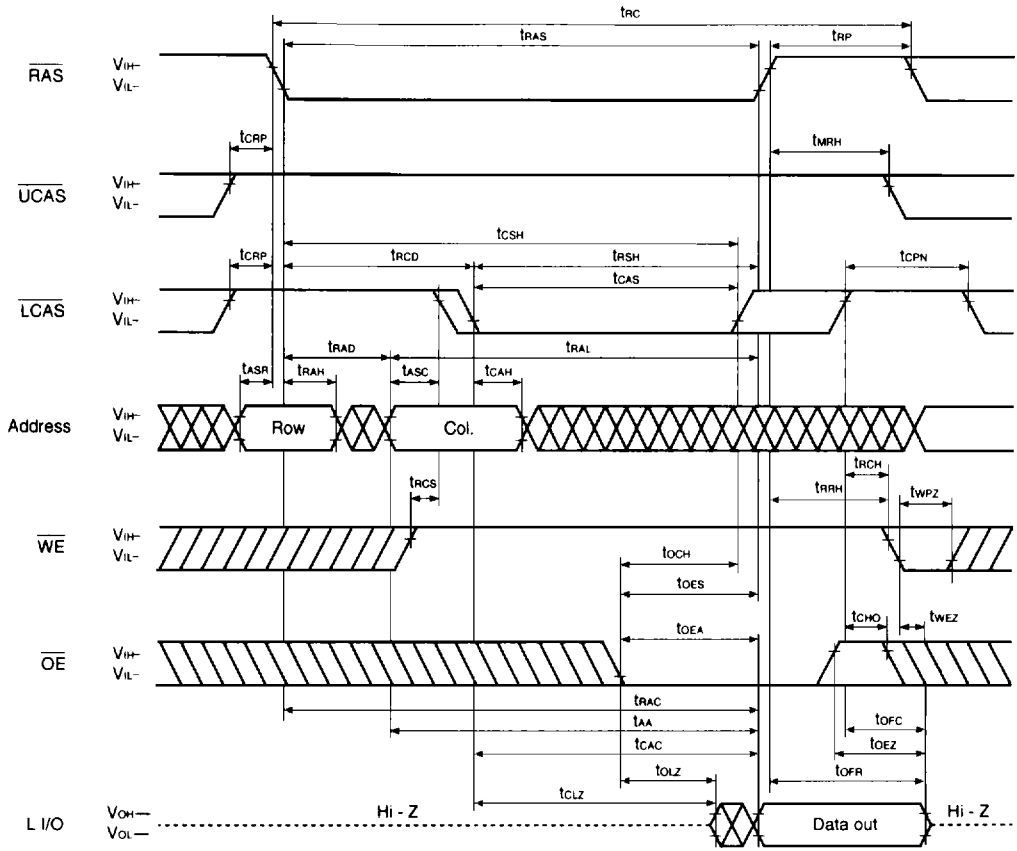
Remark U I/O: Hi-Z

Early Write Cycle
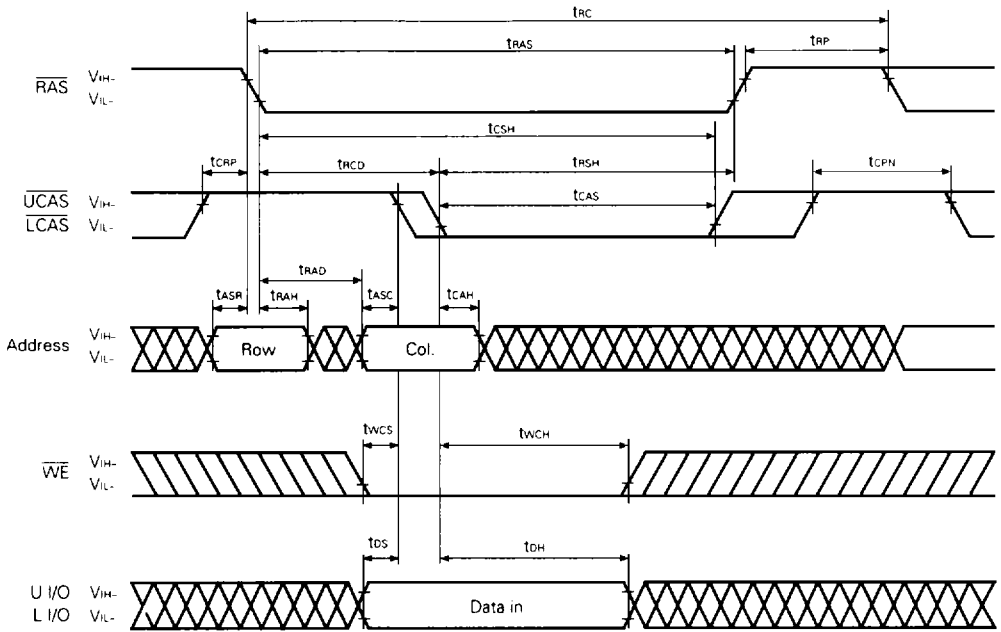
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle
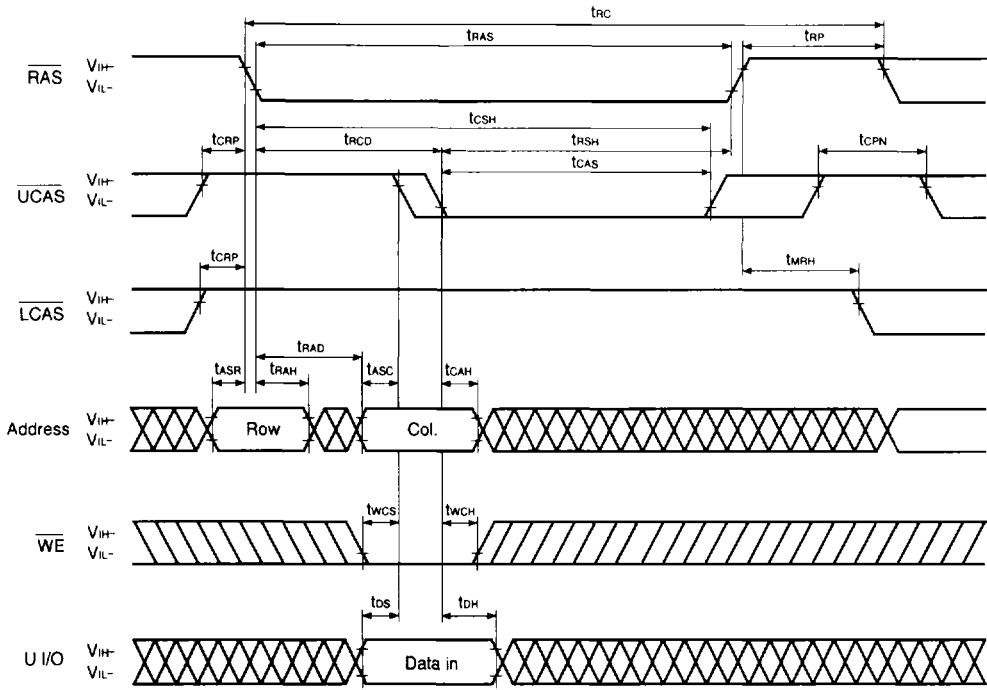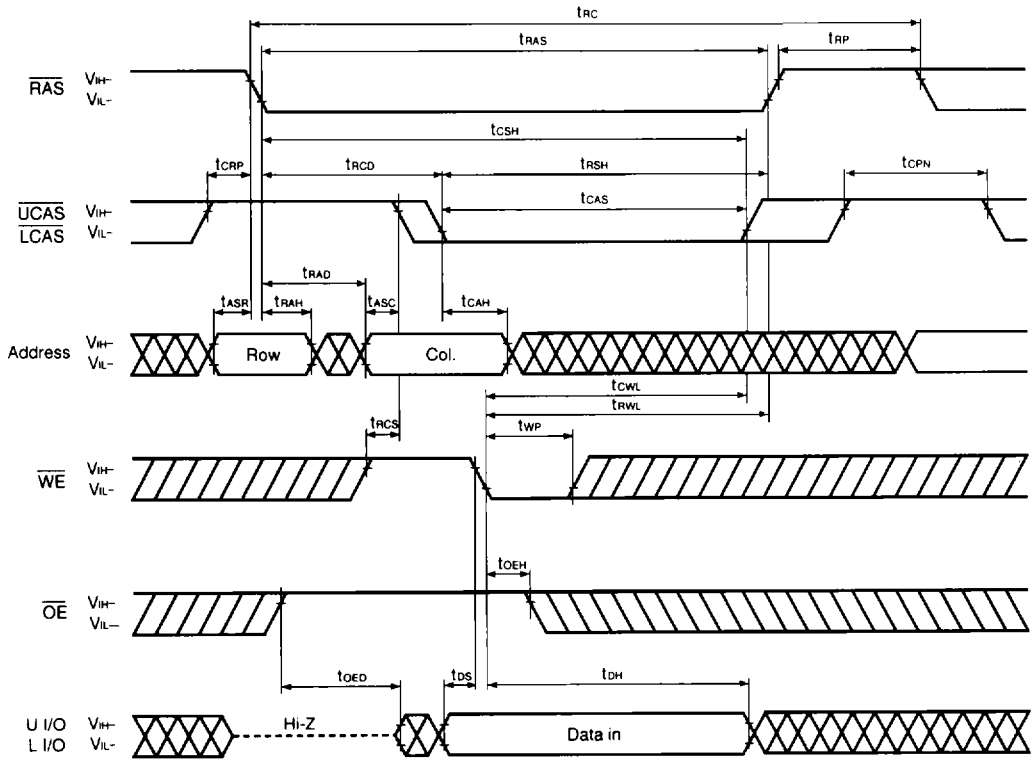

Remark $\overline{OE}$, L I/O: Don't care
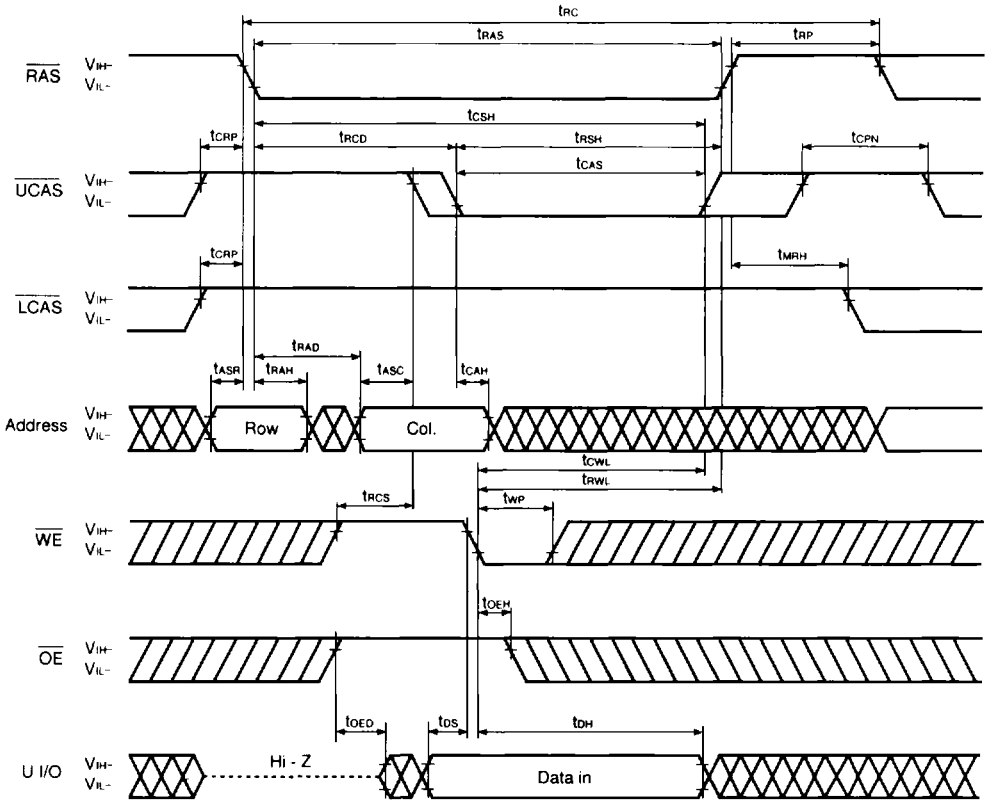
Lower Byte Early Write Cycle
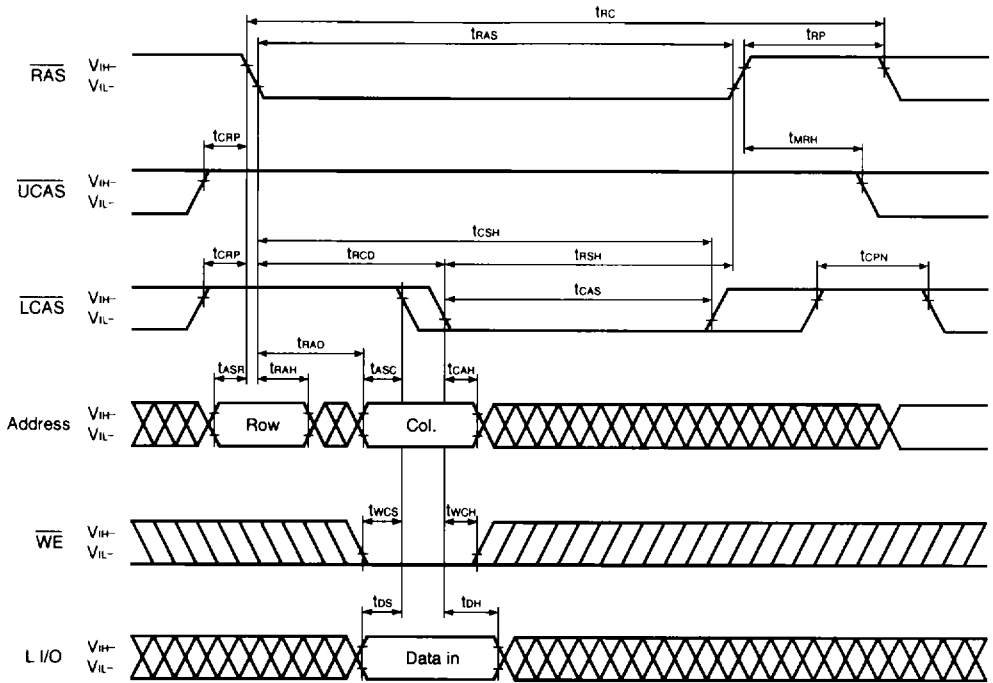
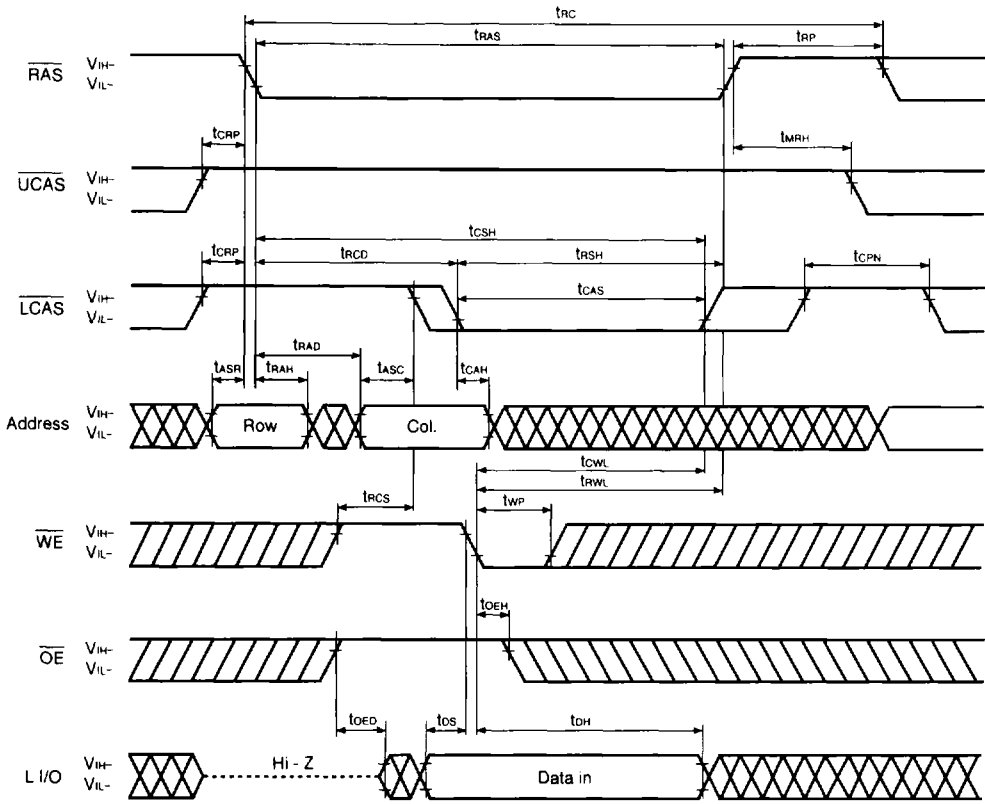**Remark** $\overline{OE}$, U I/O: Don't care
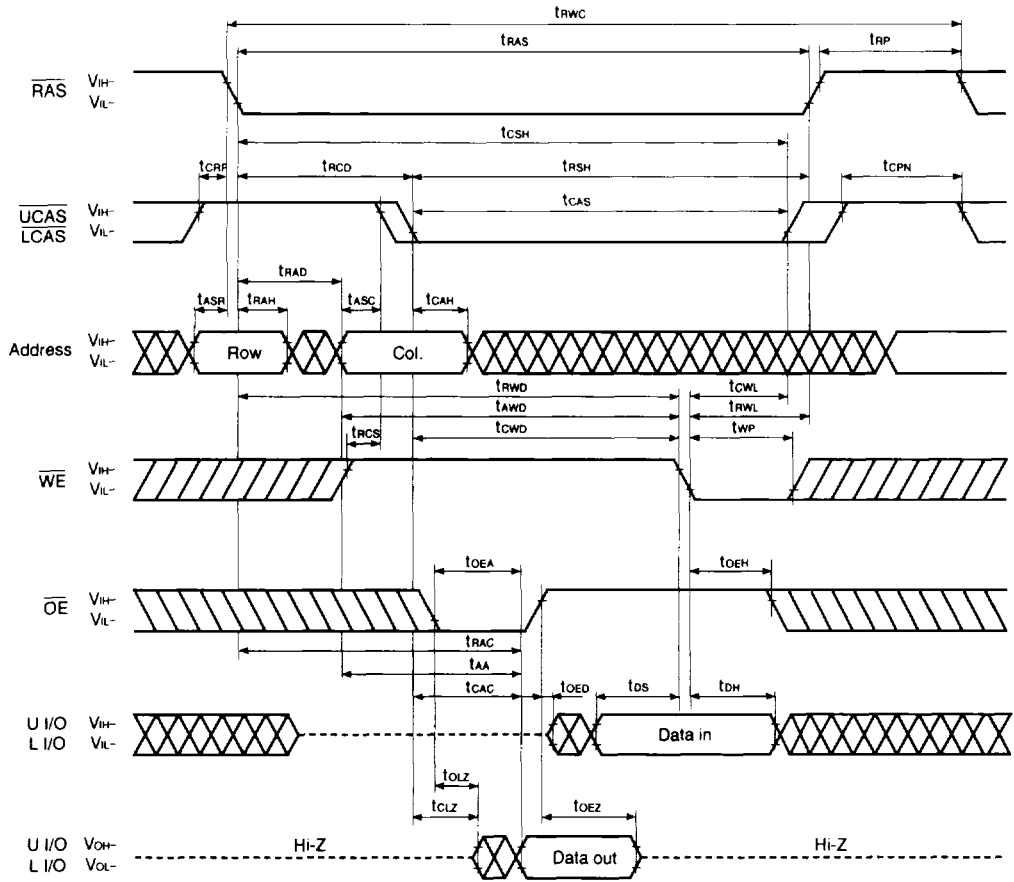
Late Write Cycle

Upper Byte Late Write Cycle

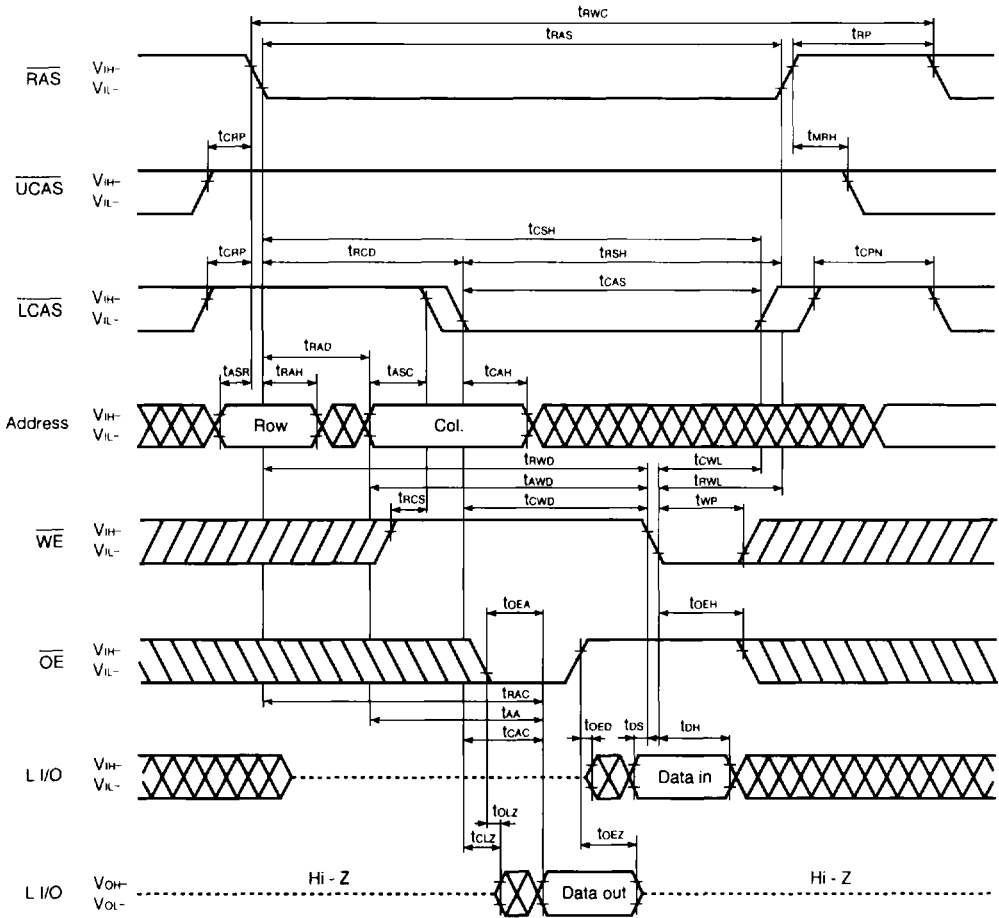**Remark** L I/O: Don't care

Lower Byte Late Write Cycle

Remark U I/O: Don't care

Read Modify Write Cycle

Upper Byte Read Modify Write Cycle

Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.
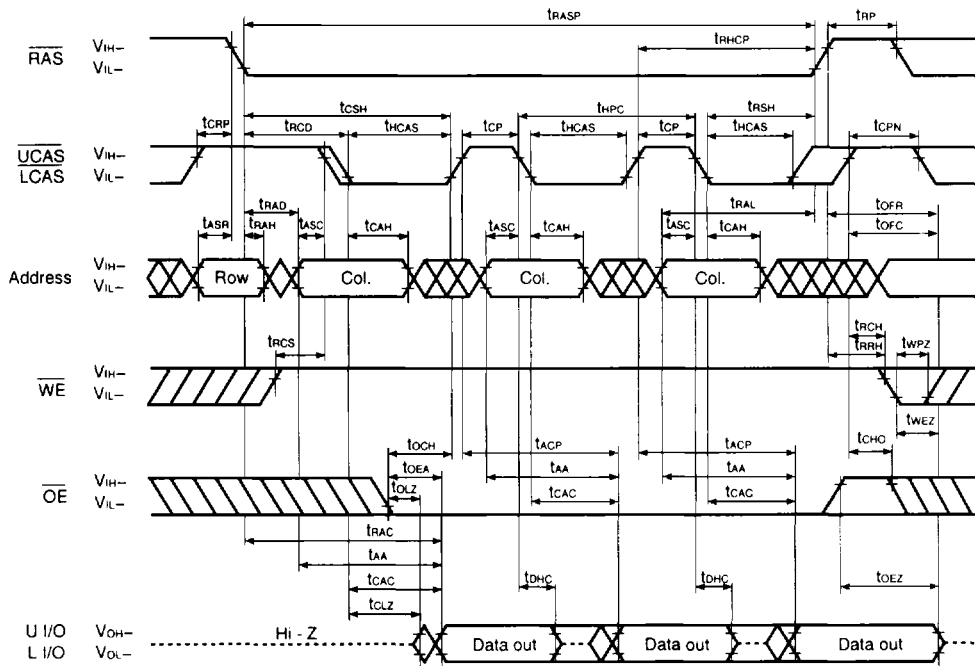
Lower Byte Read Modify Write Cycle


Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.
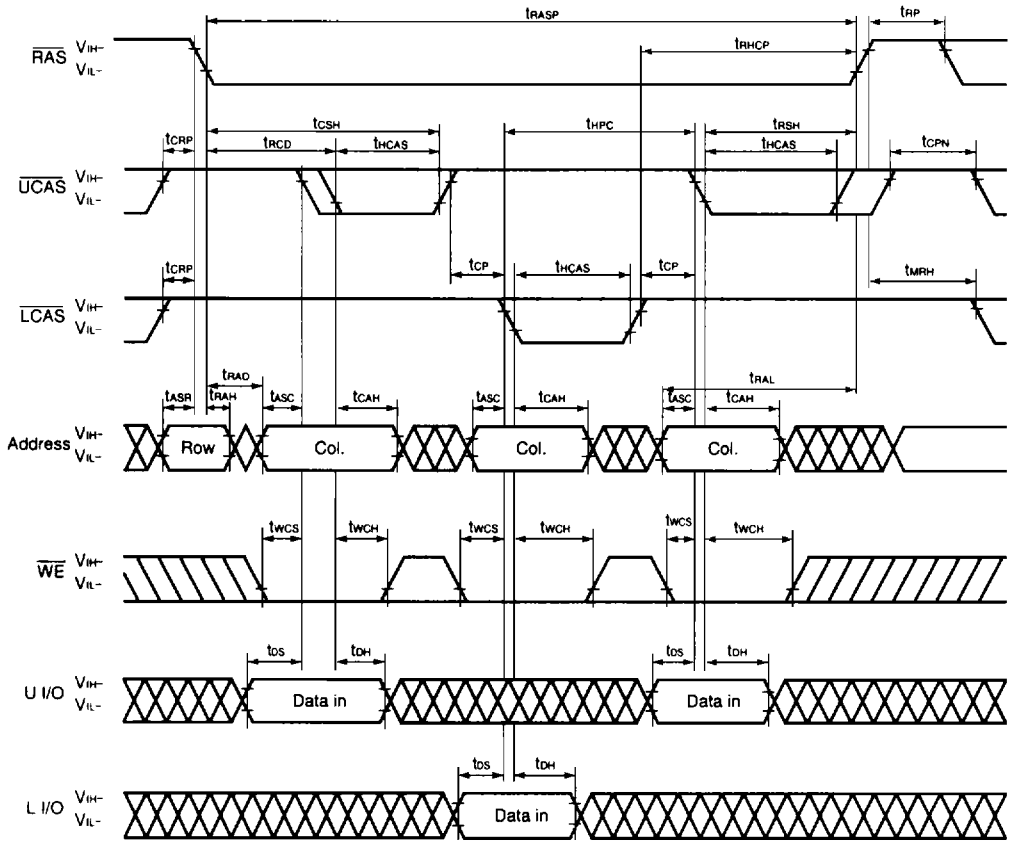
Hyper Page Mode (EDO) Read Cycle

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Byte Read Cycle

Remarks   1.   In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

           2.   This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.
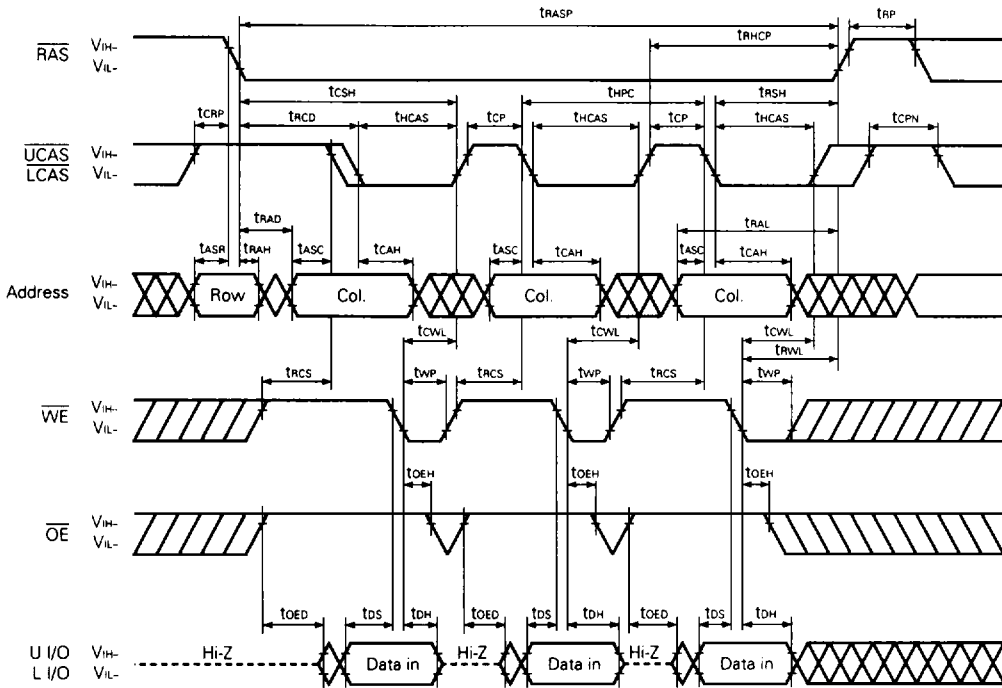
Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle (OE Control)

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Hyper Page Mode (EDO) Early Write Cycle
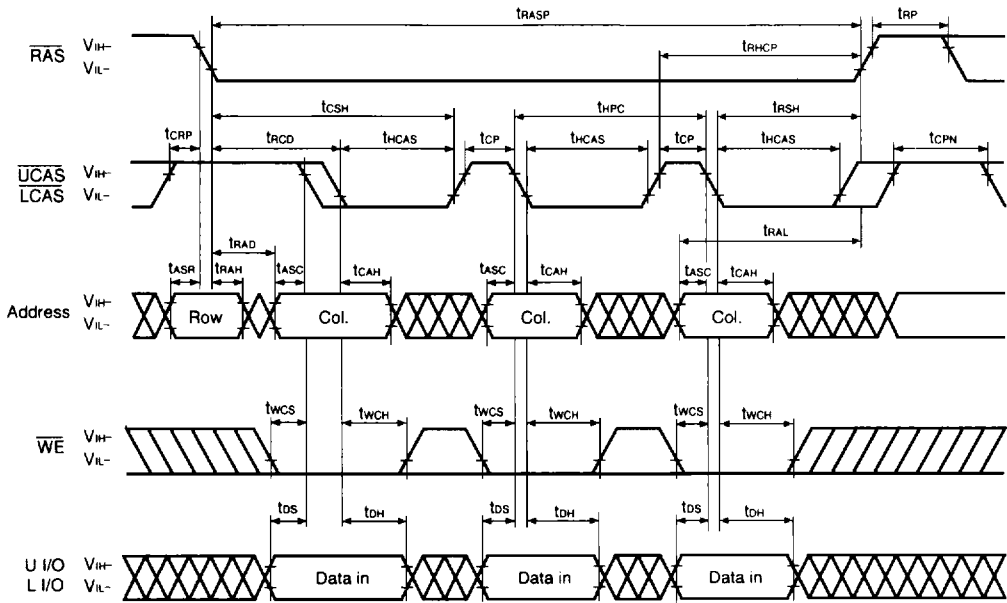
Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

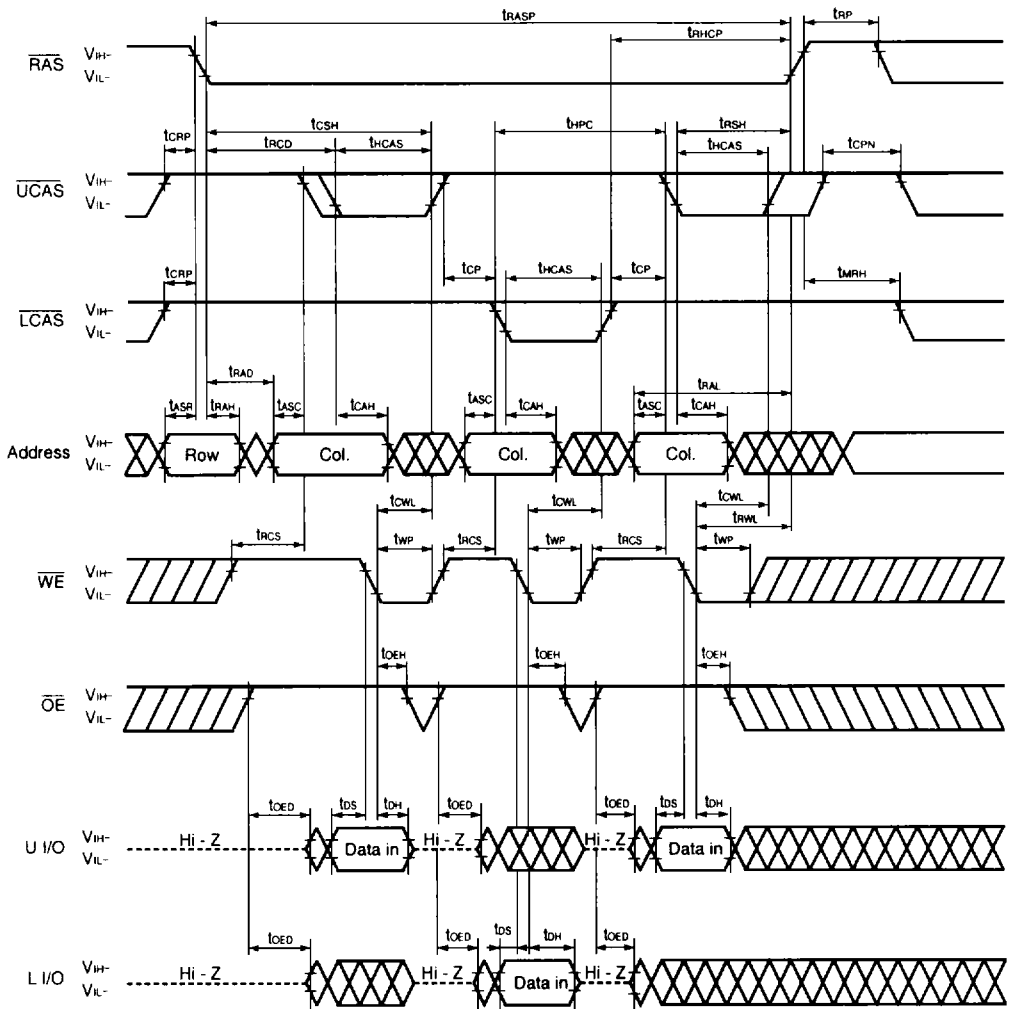**Hyper Page Mode (EDO) Byte Early Write Cycle**
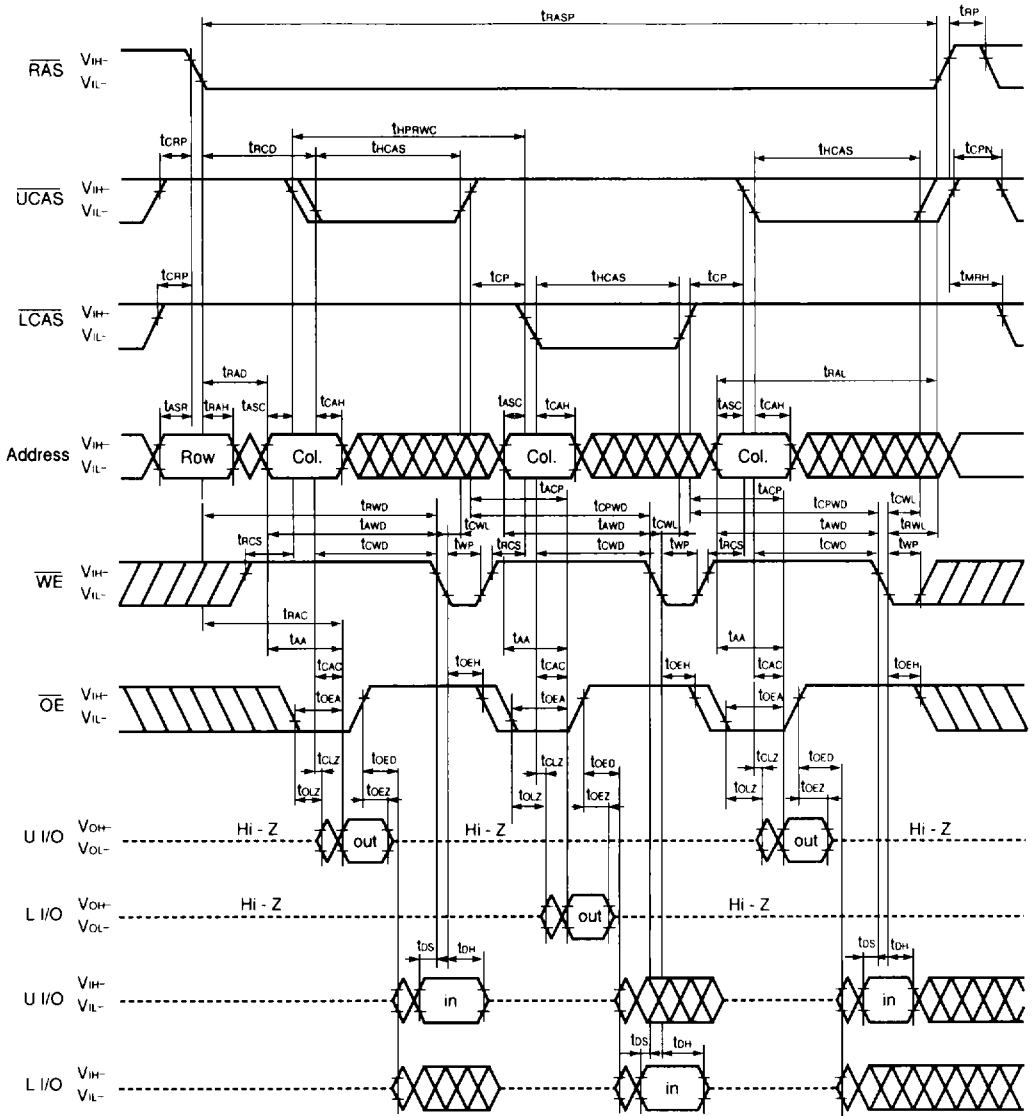

Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
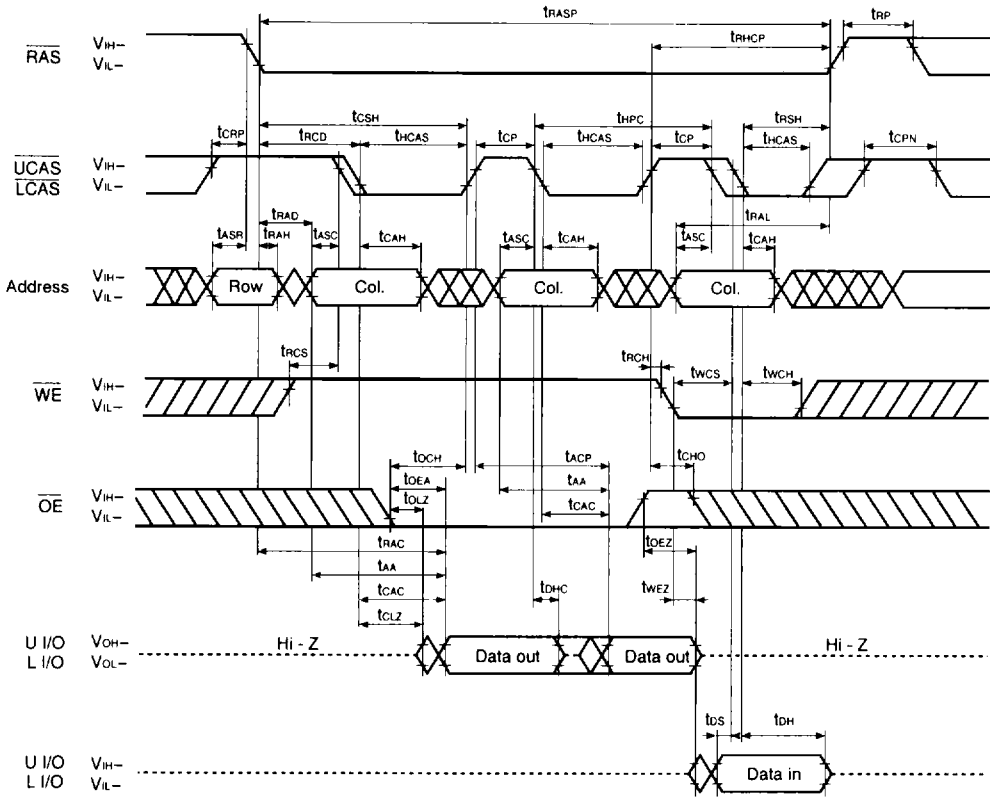
Hyper Page Mode (EDO) Byte Late Write Cycle

Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Modify Write Cycle

> **Remark**   In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Byte Read Modify Write Cycle

Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

        2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read and Write Cycle

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16165L)
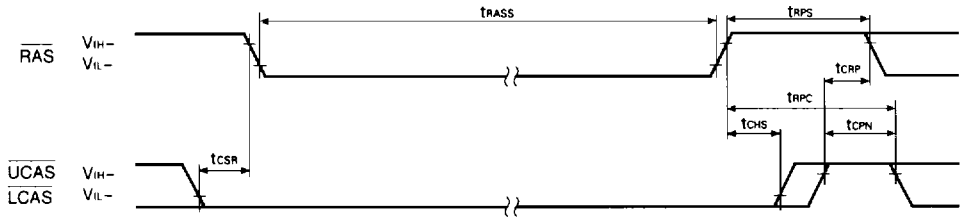
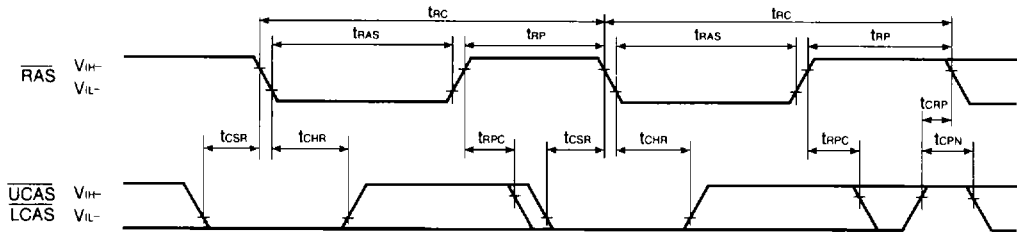**Remark** Address, $\overline{WE}$, $\overline{OE}$: Don't care   L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\,(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu$s), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu$s $< t_{RAS} < 100\ \mu$s, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (4,096/128 ms) should be met.

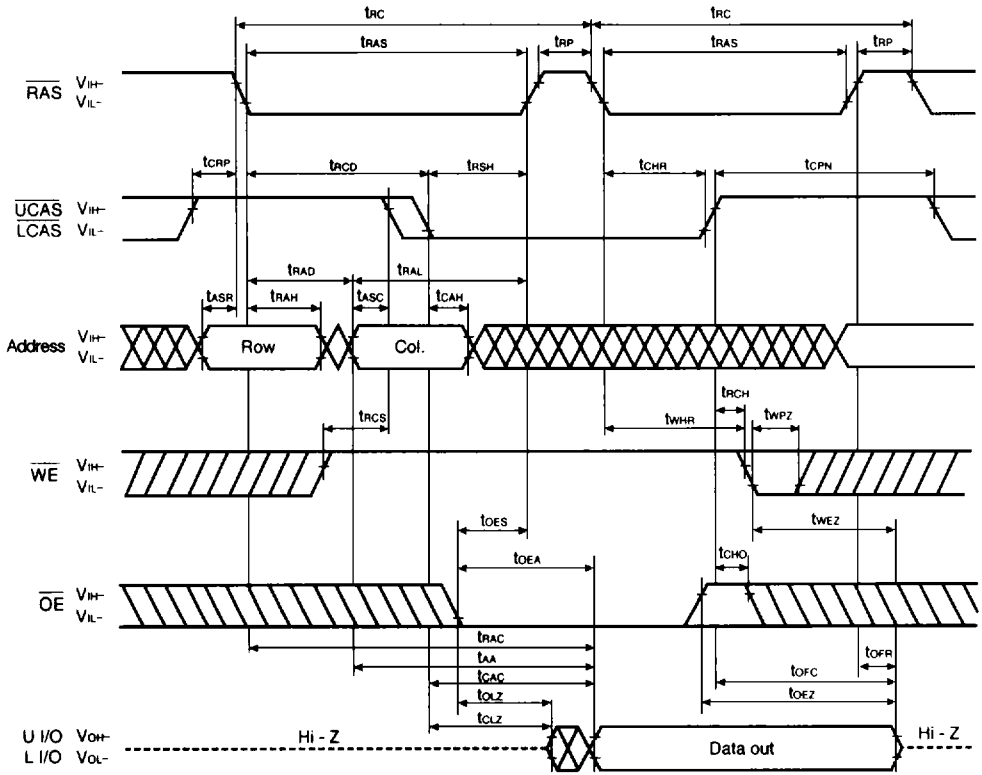For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care   L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle
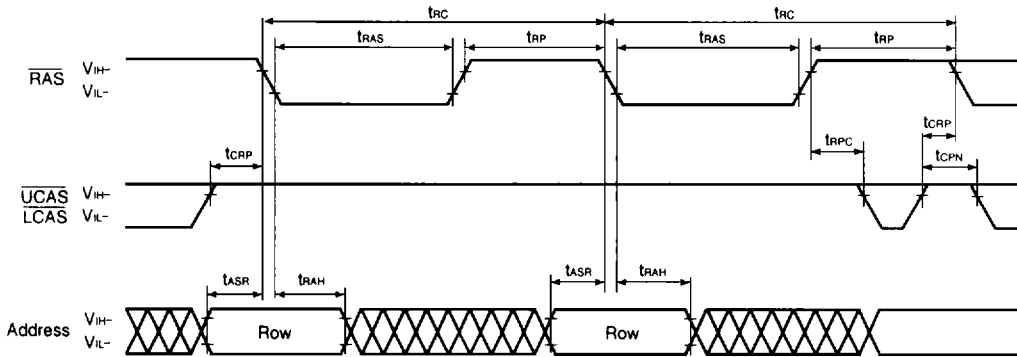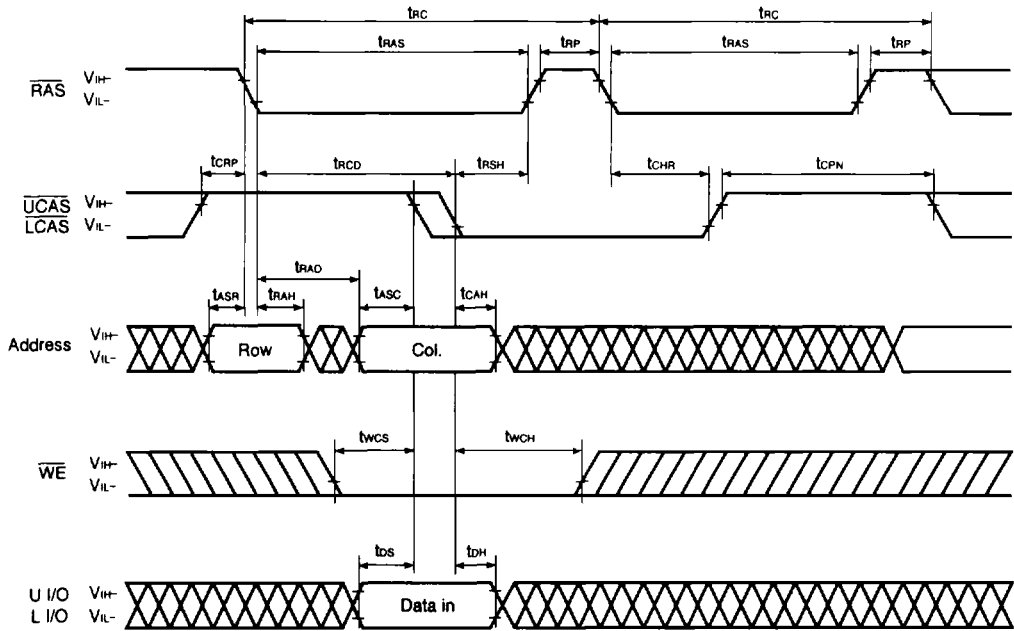

Remark $\overline{WE}$, $\overline{OE}$: Don't care   L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)

Hidden Refresh Cycle (Write)

Remark $\overline{OE}$: Don't care

Package Drawings

50PIN PLASTIC TSOP(II) (400 mil)
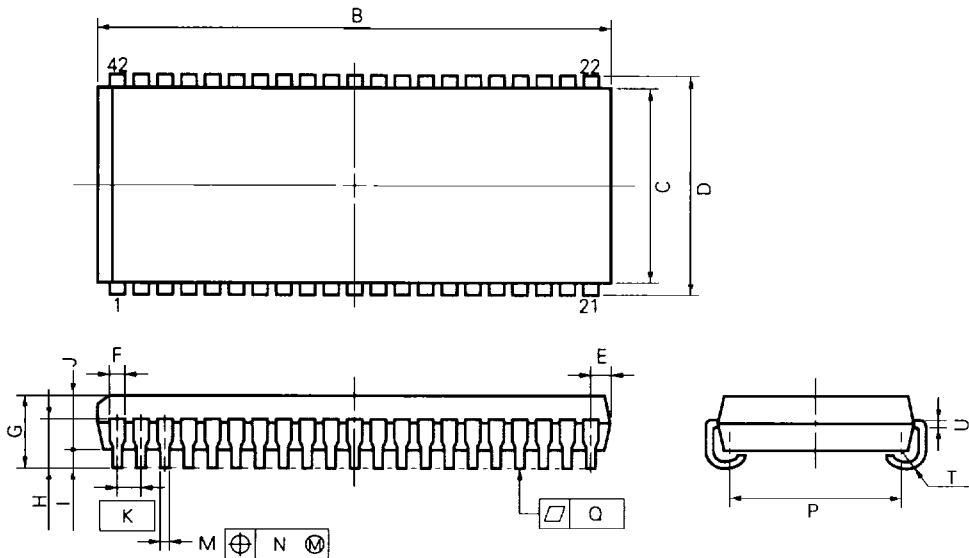

detail of lead end
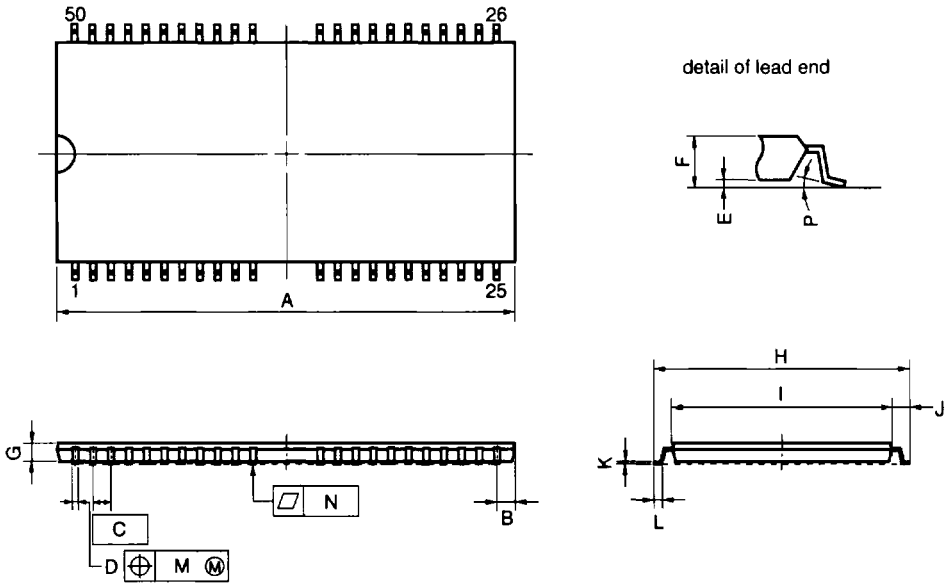
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)

P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

409

Recommended Soldering Conditions

The following conditions must be met for soldering conditions of the µPD42S16165L, 4216165L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

µPD42S16165LG5, 4216165LG5: 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^Note (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^Note (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

µPD42S16165LLE, 4216165LLE: 42-pin plastic SOJ (400 mil)

Please consult with our sales offices for soldering conditions of the µPD42S16165LLE, 4216165LLE.