MOTOROLA

Military 54LS273

Octal D Flip-Flop With Common Clear

ELECTRICALLY TESTED PER: MIL-M-38510/32501

The 54LS273 is a high-speed 8-Bit Register. The register consists of eight D type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset (CLEAR). This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

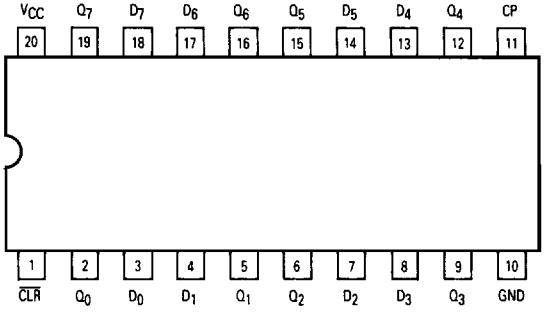
- 8-Bit High-Speed Register
- Parallel Register
- Common Clock and Master Reset
- Input Clamp Diodes Limit High-Speed Termination Effects

AVAILABLE AS:

1) JAN: JM38510/32501BXA
2) SMD: 7801001
3) 883C: 54LS273/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2
***Call Factory for latest update**

CONNECTION DIAGRAM



TRUTH TABLE

CLR	CP	D_n	Q_n
L	X	X	L
H	↑	H	H
H	↑	L	L

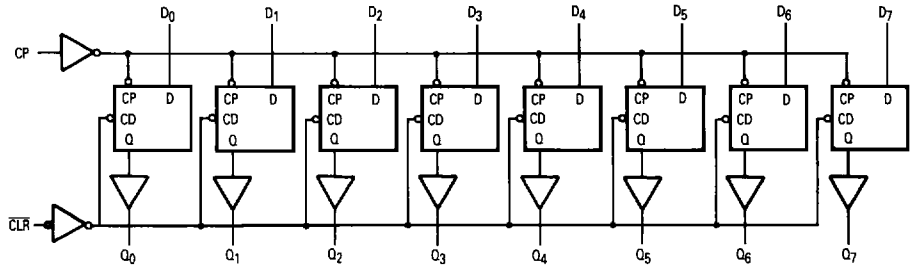
H = HIGH Logic Level
L = LOW Logic Level
X = Immaterial

PIN ASSIGNMENTS

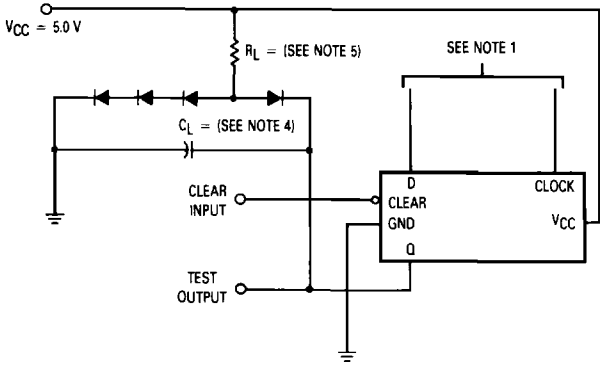
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{CLR}$	1	1	1	GND
Q_0	2	2	2	OPEN
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
Q_1	5	5	5	OPEN
D_2	6	6	6	OPEN
Q_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
Q_3	9	9	9	OPEN
GND	10	10	10	GND
CP	11	11	11	V_{CC}
Q_4	12	12	12	OPEN
D_4	13	13	13	V_{CC}
D_5	14	14	14	V_{CC}
Q_5	15	15	15	OPEN
Q_6	16	16	16	OPEN
D_6	17	17	17	V_{CC}
D_7	18	18	18	V_{CC}
Q_7	19	19	19	OPEN
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

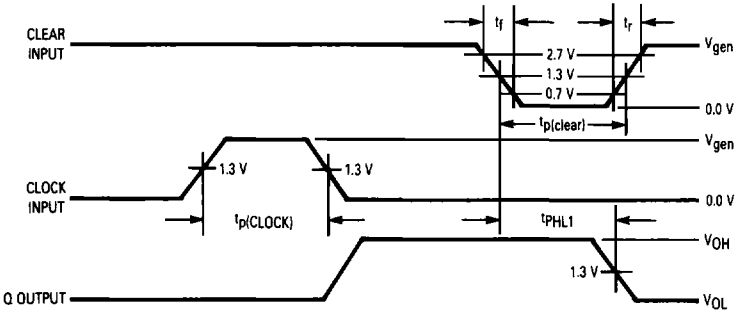
LOGIC DIAGRAM



AC TEST CIRCUIT



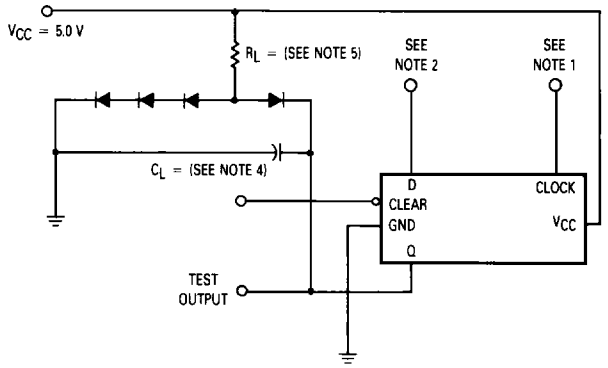
WAVEFORMS



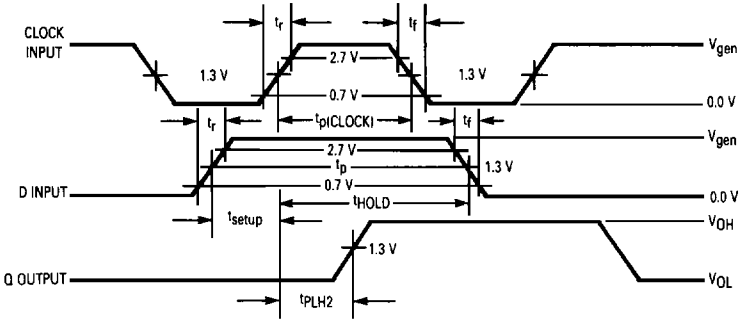
ASYNCHRONOUS SWITCHING

NOTES:
1. Clear input dominates regardless of the state of the clock or D inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear input pulse characteristics: V_{gen} = 3.0 V ± 0.2 V, $t_f \leq 6.0$ ns, $t_r \leq 15$ ns, $t_{p(clear)}$ = 20 ns and PRR ≤ 1.0 MHz.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 kΩ ± 5.0%.
6. Clock input pulse characteristics: $t_{p(clock)} \geq 20$ ns, V_{gen} = 3.0 V ± 0.2 V and PRR ≤ 1.0 MHz.
7. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

AC TEST CIRCUIT



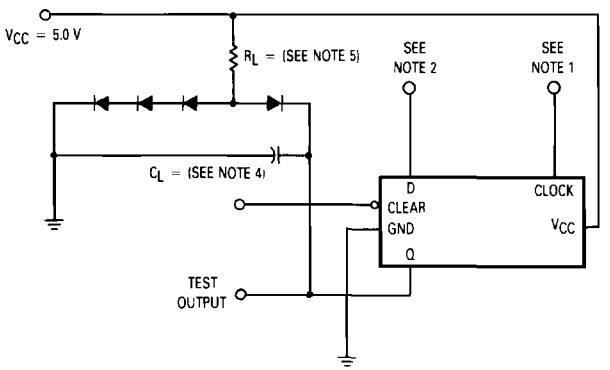
WAVEFORMS



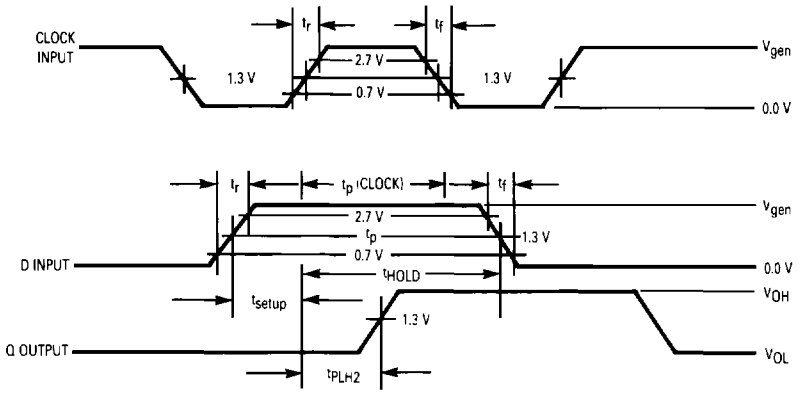
NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3.0 V ± 0.2 V, $t_r \leq$ 15 ns, $t_f \leq$ 6.0 ns, $t_{p(clock)}$ = 30 ns and PRR ≤ 1.0 MHz. When testing f_{MAX}, PRR = (see table 1), $t_f = t_r \leq$ 6.0 ns.
2. D input has the following characteristics: V_{gen} = 3.0 V ± 0.2 V, $t_r \leq$ 15 ns, $t_f \leq$ 6.0 ns, t_{setup} = 20 ns, t_{hold} = 5.0 ns, t_p = 25 ns and PRR is 50% of the clock PRR. For f_{MAX}, $t_f = t_r \leq$ 6.0 ns.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 kΩ ± 5.0%.
6. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

AC TEST CIRCUIT

SYNCHRONOUS SWITCHING (HIGH-LEVEL DATA)



WAVEFORMS



NOTES:

1. Clock input pulse has the following characteristics: V_{gen} = 3.0 V ± 0.2 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{p(clock)}$ = 30 ns and PRR ≤ 1.0 MHz.
2. D input has the following characteristics: V_{gen} = 3.0 V ± 0.2 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_{setup} = 20 ns, t_{hold} = 5.0 ns, t_p = 25 ns and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 kΩ ± 5.0%.
6. Terminal condition (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

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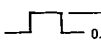
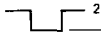
Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IN} = 2.0 V, other inputs are open, CLR = 2.0 V, CP = (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, other inputs are open, CLR = 2.0 V or 0.7 V, V_{IN} = 0.7 V, CP = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−105	−345	−105	−345	−105	−345	μA	V_{CC} = 5.5 V, $V_{IL(CLR)}$ = 0.4 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−160	−400	−160	−400	−160	−400	μA	V_{CC} = 4.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, CLR = 4.5 V, CP = (See Note 2).
I_{CC}	Power Supply Current		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), CP = (See Note 2).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:

1. 

2. 

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output CLR to Q_n	5.0	32 27	5.0	42 37	5.0	42 37	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output CP to Q_n	5.0	32 27	5.0	42 37	5.0	42 37	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output CP to Q_n	5.0	32 27	5.0	42 37	5.0	42 37	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25		25		25		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	30						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTE:
The limits specified for C_L = 15 pF are guaranteed, but not tested.

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