

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# HD74HC173

4-bit D-type Register (with 3-state outputs)



ADE-205-459 (Z)

1st. Edition

Sep. 2000

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## Description

The four D type Flip-Flops operate synchronously from a common clock. The 3-state outputs allow the device to be used in bus organized systems. The outputs are placed in the 3-stage mode when either of the output disable pins are in the logic high level.





The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic high level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Clearing is enabled by taking the clear input to a logic high level. The data outputs change state on the positive going edge of the clock.

## Features

- High Speed Operation:  $t_{pd}$  (Clock to Q) = 14 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

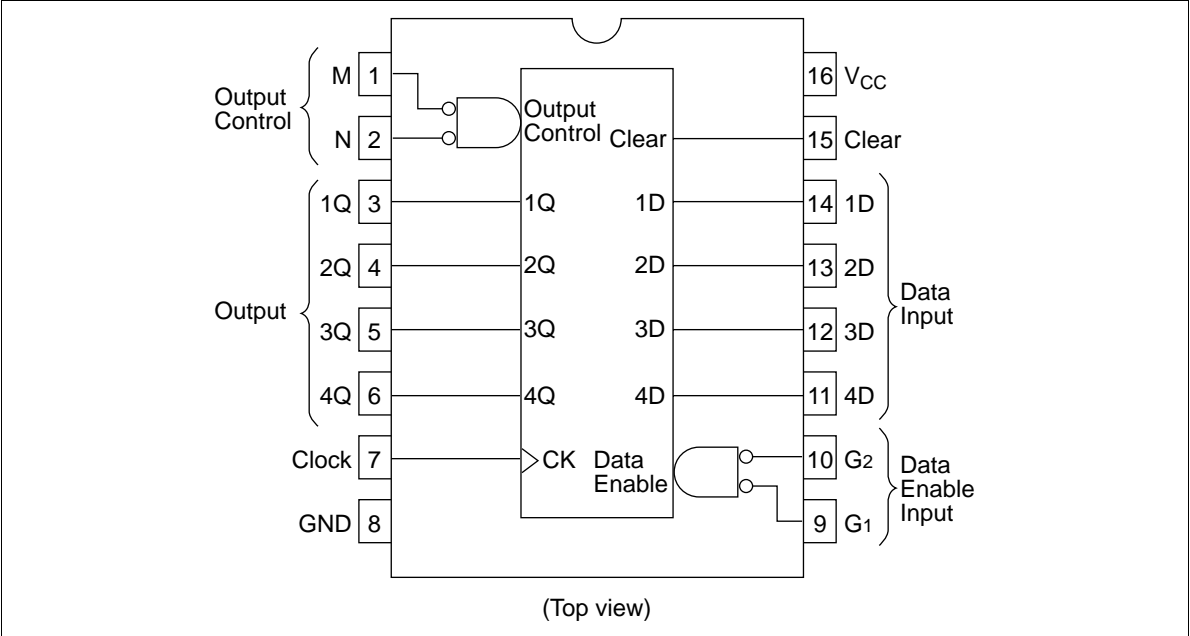
Function Table

Inputs

Clear	Clock	Data Enable		Data D	Output Q
		G <sub>1</sub>	G <sub>2</sub>		
H	X	X	X	X	L
L	L	X	X	X	Q <sub>0</sub>
L		H	X	X	Q <sub>0</sub>
L		X	H	X	Q <sub>0</sub>
L		L	L	L	L
L		L	L	H	H

Note: When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

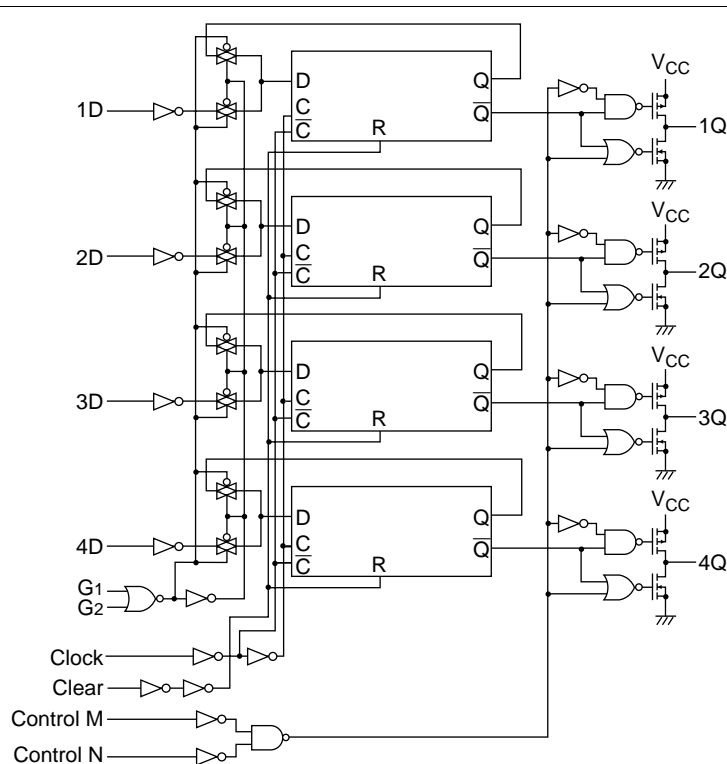
Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to +7.0	V
Input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC current drain per pin	$I_{OUT}$	$\pm 35$	mA
DC current drain per VCC, GND	$I_{CC}, I_{GND}$	$\pm 75$	mA
DC input diode current	$I_{IK}$	$\pm 20$	mA
DC output diode current	$I_{OK}$	$\pm 20$	mA
Power dissipation per package	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Block Diagram



## DC Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		
		6.0	5.68	—	—	5.63	—		
	V <sub>OL</sub>	2.0	—	0.0	0.1	—	0.1	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		
		6.0	—	—	0.26	—	0.33		
Off-state output current	I <sub>OZ</sub>	6.0	—	—	±0.5	—	±5.0	μA	Vin = V <sub>IH</sub> or V <sub>IL</sub> , Vout = V <sub>CC</sub> or GND
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	4.0	—	40	μA	Vin = V <sub>CC</sub> or GND, Iout = 0 μA

# HD74HC173

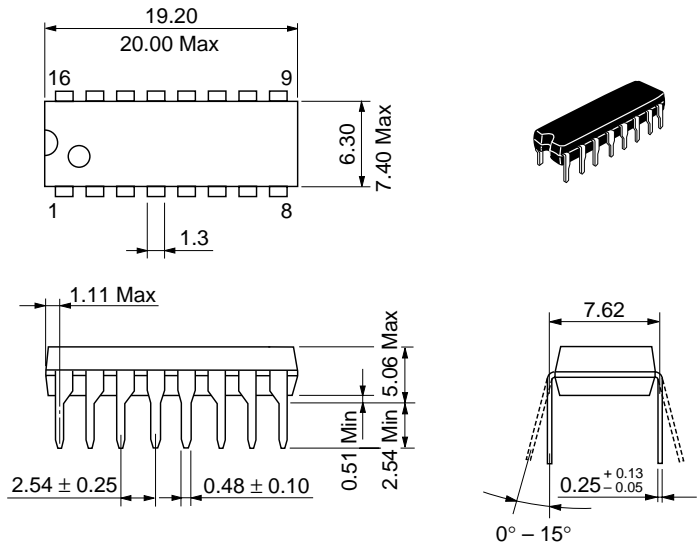
## AC Characteristics (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Item	Symbol	V <sub>cc</sub> (V)	Ta = 25°C			Ta = −40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f <sub>max</sub>	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t <sub>PLH</sub>	2.0	—	—	175	—	220	ns	Clock to Q
		4.5	—	14	35	—	44		
		6.0	—	—	30	—	37		
	t <sub>PHL</sub>	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Enable time	t <sub>ZH</sub>	2.0	—	—	150	—	190	ns	
		4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Disable time	t <sub>HZ</sub>	2.0	—	—	150	—	190	ns	
		4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t <sub>su</sub>	2.0	100	—	—	125	—	ns	
		4.5	20	4	—	25	—		
		6.0	17	—	—	21	—		
Removal time	t <sub>rem</sub>	2.0	90	—	—	115	—	ns	
		4.5	18	0	—	23	—		
		6.0	15	—	—	20	—		
Hold time	t <sub>h</sub>	2.0	5	—	—	5	—	ns	
		4.5	5	−2	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t <sub>w</sub>	2.0	80	—	—	100	—	ns	
		4.5	16	4	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t <sub>TLH</sub>	2.0	—	—	60	—	75	ns	
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	Cin	—	—	5	10	—	10	pF	



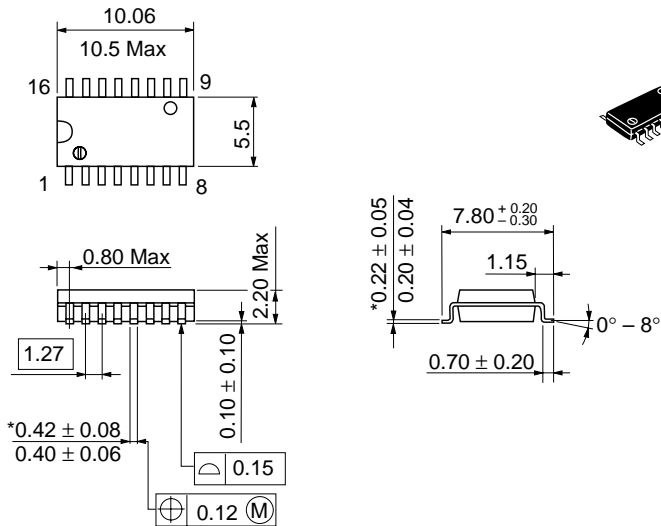
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

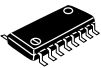
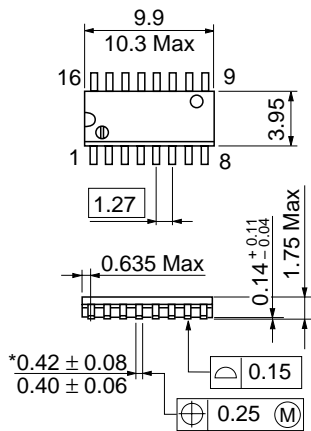
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	<a href="http://semiconductor.hitachi.com/">http://semiconductor.hitachi.com/</a>
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## For further information write to:

Hitachi Semiconductor  
(America) Inc.

179 East Tasman Drive,  
San Jose, CA 95134

Tel: <1> (408) 433-1990

Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic Components Group

Dornacher Straße 3  
D-85622 Feldkirchen, Munich

Germany

Tel: <49> (89) 9 9180-0

Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.

Whitebrook Park

Lower Cookham Road

Maidenhead

Berkshire SL6 8YA, United Kingdom

Tel: <44> (1628) 585000

Fax: <44> (1628) 585160

Hitachi Asia Ltd.

Hitachi Tower

16 Collyer Quay #20-00,

Singapore 049318

Tel: <65>-538-6533/538-8577

Fax: <65>-538-6933/538-3877

URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.

(Taipei Branch Office)

4/F, No. 167, Tun Hwa North Road,

Hung-Kuo Building,

Taipei (105), Taiwan

Tel: <886>-(2)-2718-3666

Fax: <886>-(2)-2718-8180

Telex: 23222 HAS-TP

URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.

Group III (Electronic Components)

7/F., North Tower,

World Finance Centre,

Harbour City, Canton Road

Tsim Sha Tsui, Kowloon,

Hong Kong

Tel: <852>-(2)-735-9218

Fax: <852>-(2)-730-0281

URL: <http://www.hitachi.com.hk>