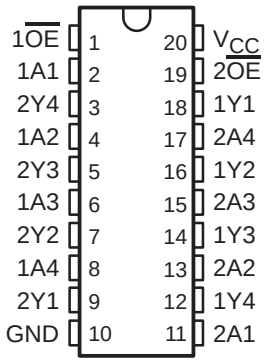
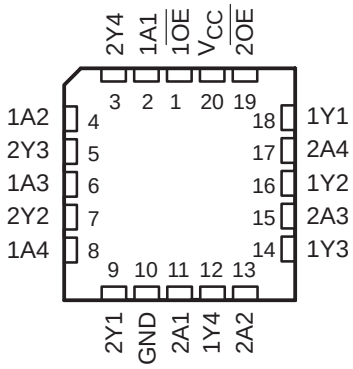
- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

SN54ABT2240A . . . J OR W PACKAGE
SN74ABT2240A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT2240A . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the ’ABT2241 and ’ABT2244A, these devices provide combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

These devices are organized as two 4-bit line drivers with separate $\overline{OE}$ inputs. When $\overline{OE}$ is low, the devices pass inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

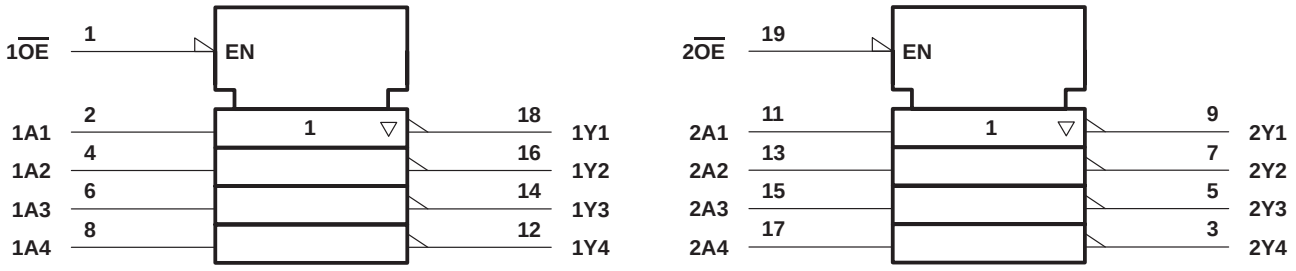
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT2240A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2240A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

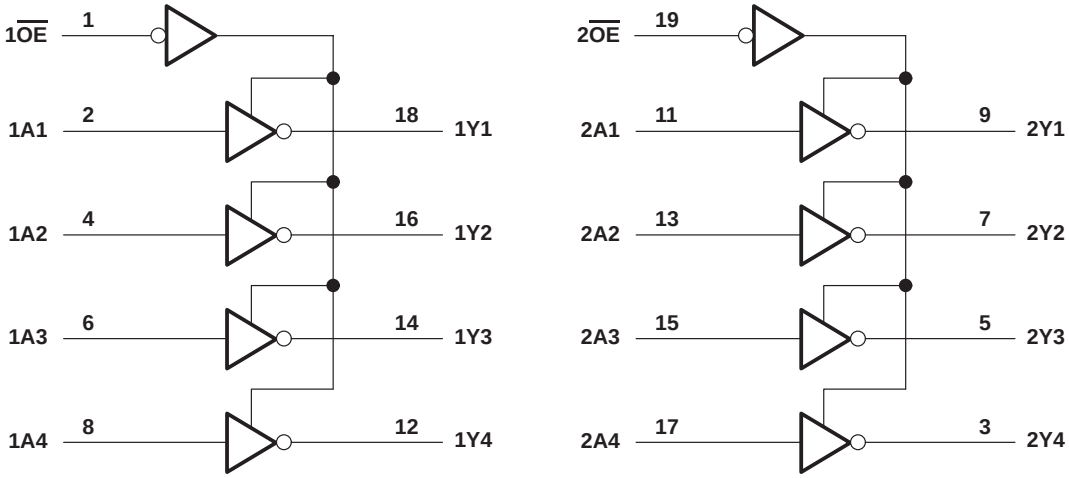
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†

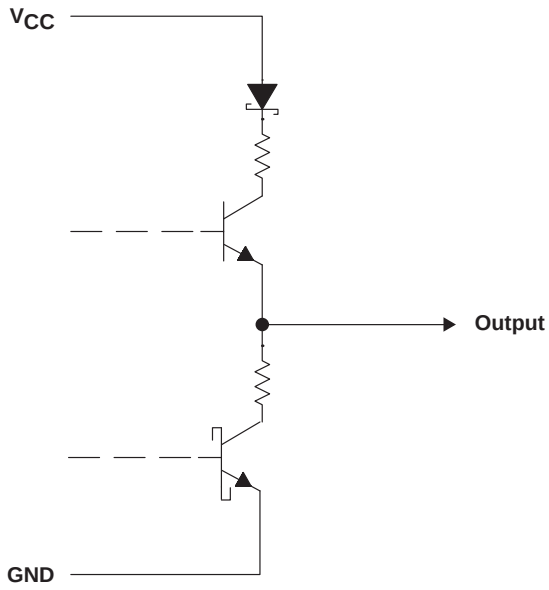


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 30 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT2240A		SN74ABT2240A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT2240A		SN74ABT2240A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
			I_{OH} = –32 mA	2*					2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	V
V_{hys}					100						mV
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			10*		10		10	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V			–10*		–10		–10	µA
I_{off}		V_{CC} = 0,	V_I or $V_O \le$ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}§	Data inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i		V_I = 2.5 V or 0.5 V			4						pF
C_o		V_O = 2.5 V or 0.5 V			7						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

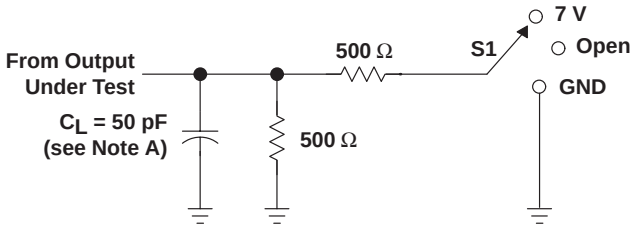
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT2240A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	3	4	1	5	ns
t_{PHL}			2.1	4.8	5.8	2.1	6.3	
t_{PZH}	$\overline{OE}$	Y	1.5	3.7	4.7	1.5	6.1	ns
t_{PZL}			1.7	6.5	7.6	1.7	8.8	
t_{PHZ}	$\overline{OE}$	Y	1.8	3.8	6.4	1.5	6.8	ns
t_{PLZ}			1	4.7	5.8	1	6.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

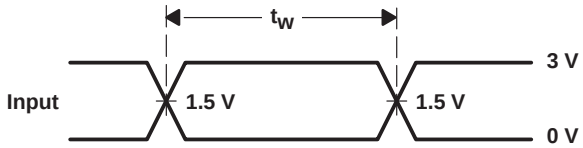
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT2240A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	3	4.1	1	4.8	ns
t_{PHL}			2.1	4.1	5.1	2.1	5.4	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.7	1.1	5.2	ns
t_{PZL}			1.7	4.5	6.4	1.7	6.8	
t_{PHZ}	$\overline{OE}$	Y	1.8	3.4	5.7	1.8	6.4	ns
t_{PLZ}			1.9	3.6	6	1.9	6.2	

PARAMETER MEASUREMENT INFORMATION

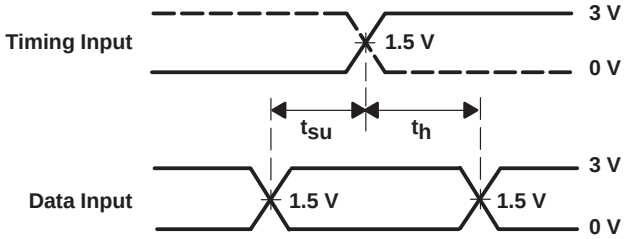


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

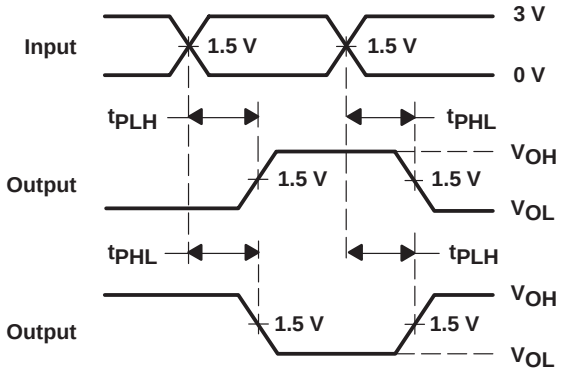
LOAD CIRCUIT



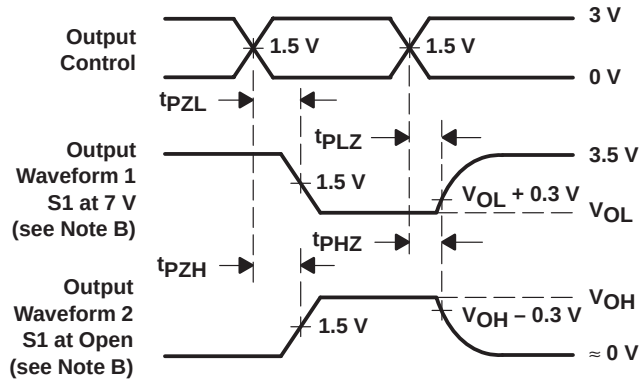
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN74ABT2240A, Octal Buffers And Line/MOS Drivers With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ABT2240A	SN74ABT2240A
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Outputs	8	8
Output Drive (mA)		-32/12
tpd max (ns)		6.3
Static Current		15.12
Logic	Inv	Inv

FEATURES

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- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC*-II *B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

DESCRIPTION

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These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'ABT2241 and 'ABT2244A, these devices provide combinations of inverting and noninverting outputs, symmetrical active-low output-enable (OE\) inputs, and complementary OE and OE\ inputs. These devices feature high fan-out and improved fan-in.

These devices are organized as two 4-bit line drivers with separate OE\ inputs. When OE\ is low, the devices pass inverted data from the A inputs to the Y outputs. When OE\ is high, the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT2240A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT2240A is characterized for operation from -40°C to 85°C.

Product Folder: SN74ABT2240A, Octal Buffers And Line/MOS Drivers With 3-State Outputs

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74abt2240a.pdf (106 KB,Rev.E) (Updated: 10/28/1998)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Advanced BiCMOS Technology (ABT) Logic Characterization Information (Rev. B) (SCBA008B - Updated: 06/01/1997)
- Advanced BiCMOS Technology (ABT) Logic Enables Optimal System Design (Rev. A) (SCBA001A - Updated: 03/01/1997)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices (Rev. A) (SCBA006A - Updated: 12/01/1996)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. C) (SCBA017C - Updated: 11/22/2002)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ABT2240ADBR	SSOP (DB)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT2240ADW	SOIC (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT2240ADWR	SOIC (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT2240ANSR	SOP (NS)	20		ACTIVE	View Product Content	Request Samples
SN74ABT2240APWR	TSSOP (PW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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Product Folder: SN74ABT2240A, Octal Buffers And Line/MOS Drivers With 3-State Outputs

DEVICE INFORMATION Updated Daily							TI INVENTORY STATUS As Of 09:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 09:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME	DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
SN74ABT2240ADBLE	OBSOLETE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors		
SN74ABT2240ADBR	ACTIVE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU | 0.26	2000	2000*	>10k | 08 May	4 WKS	Arrow | Americas	>1k	BUY NOW
										DigiKey | Americas	>1k	BUY NOW
SN74ABT2240ADW	ACTIVE	SOIC (DW) | 20	-40 TO 85	View Contents	1KU | 0.26	25	0*	3325 | 30 Apr	4 WKS	Insight | Americas	1k	BUY NOW
								>10k | 12 May		DigiKey | Americas	182	BUY NOW
SN74ABT2240ADWR	ACTIVE	SOIC (DW) | 20	-40 TO 85	View Contents	1KU | 0.26	2000	0*	1328 | 21 Apr	4 WKS	DigiKey | Americas	>1k	BUY NOW
								>10k | 12 May				
SN74ABT2240AN	ACTIVE	PDIP (N) | 20	-40 TO 85	View Contents	1KU | 0.26	20	980*	13 | 21 Apr	4 WKS	EBV Electronik | Europe	420	BUY NOW
SN74ABT2240ANSR	ACTIVE	SOP (NS) | 20		View Contents	1KU | 0.77	2000	0*	>10k | 12 May	4 WKS	DigiKey | Americas	897	BUY NOW
SN74ABT2240APW	ACTIVE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU | 0.49	70	0*	560 | 16 Apr	4 WKS	Arrow | Americas	>1k	BUY NOW
								38 | 21 Apr				
								>10k | 08 May				
SN74ABT2240APWLE	OBSOLETE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors		
SN74ABT2240APWR	ACTIVE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU | 0.26	2000	2000*	530 | 21 Apr	4 WKS	DigiKey | Americas	>1k	BUY NOW
								>10k | 08 May				

Table Data Updated on: 4/17/2003